SECTION 23. ELECTRICAL CHARACTERISTICS

23.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to V_{CC}+0.3	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Note: Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

23.2 DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = −20 to +75°C, unless otherwise noted)

Symbol	Item	Min	Typ	Max	Unit	Condition
V_{IH1}	Input High Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$	V_{CC}−0.6	–	V_{CC}+0.3	V	
V_{IH2}	Input High Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$	2.0	–	V_{CC}+0.3	V	
V_{IL1}	Input Low Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$	−0.3	–	0.6	V	
V_{IL2}	Input Low Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$	−0.3	–	0.8	V	
V_{OH}	Output High Voltage All outputs	2.4	–	–	V	I_{OH} = −200 μA
		V_{CC}−1.2	–	–		I_{OH} = −20 μA
V_{OL}	Output Low Voltage All Outputs	–	–	0.45	V	I_{OL} = 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL, $\overline{RESET}$	–	–	1.0	μA	Vin=0.5 to V_{CC} − 0.5 V
I_{TL}	Three State Leakage Current	–	–	1.0	μA	Vin=0.5 to V_{CC} − 0.5 V
I_{CC} (Note)	Power Dissipation (Normal Operation)	–	20	40	mA	f = 4 MHz
		–	25	50		f = 6 MHz
		–	30	60		f = 8 MHz
	Power Dissipation (System Stop Mode)	–	5	10	mA	f = 4 MHz
		–	6.3	12.5		f = 6 MHz
		–	7.5	15		f = 8 MHz
Cp	Pin Capacitance $\overline{RESET}$	–	–	120	pF	Vin=0V, f=1 MHz
	Except $\overline{RESET}$			20		Ta=25°C

Note: V_{IHmin} = V_{CC} − 1.0 V, V_{ILmax} = 0.8 V (all output terminals are at no load.)

Symbol	Item		Min	Typ	Max	Unit	Condition
V_{IHP}	Input High-Level Voltage		2.2	–	V_{CC} + 0.3	V	
V_{ILP}	Input Low-Level Voltage		−0.3	–	0.8	V	
V_{OHP}	Output High-Level Voltage		2.4	–	–	V	I_{OH} = −200 μA
			V_{CC} − 1.2	–	–		I_{OH} = −20 μA
V_{OLP}	Output Low-Level Voltage		–	–	0.45	V	* I_{OL} = 2.2 mA
			–	–	1.0		** I_{OL} = 10 mA
V_{in}	Analog Comparator Input Level Voltage	High level	V_{ref} + 0.1	–	–	V	
		Low level	–	–	V_{ref} − 0.1		
V_{ref}		V_{TH}	0	–	V_{CC} × 0.8	V	
I_{ILP}	Input Leak Current		–	–	1.0	μA	V_{in} = 0.5 to V_{CC} − 0.5

Note: *: Port A-F
**: Port F only

23.3 AC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = −20 to +75°C, unless otherwise noted)

Symbol	Item		HD647180X-4 Min	HD647180X-4 Max	HD647180X-6 Min	HD647180X-6 Max	HD647180X-8 Min	HD647180X-8 Max	Unit
t_{cyc}	Clock Cycle Time		250	2000	162	2000	125	2000	ns
t_{CHW}	Clock High Pulse Width		110	–	65	–	50	–	ns
t_{CLW}	Clock Low Pulse Width		110	–	65	–	50	–	ns
t_{cf}	Clock Fall Time		–	15	–	15	–	15	ns
t_{cr}	Clock Rise Time		–	15	–	15	–	15	ns
t_{AD}	Address Delay Time		–	110	–	90	–	80	ns
t_{AS}	Address Set-up Time ($\overline{ME}$ or $\overline{IOE}$ ↓)		50	–	30	–	20	–	ns
t_{MED1}	$\overline{ME}$ Delay Time 1		–	85	–	60	–	50	ns
t_{RDD1}	$\overline{RD}$ Delay Time 1	$\overline{IOC}$=1	–	85	–	60	–	50	ns
		$\overline{IOC}$=0	–	85	–	65	–	60	
t_{LD1}	$\overline{LIR}$ Delay Time 1		–	100	–	80	–	70 (Note)	ns
t_{AH}	Address Hold Time 1 ($\overline{ME}$, $\overline{IOE}$, $\overline{RD}$ or $\overline{WR}$ ↑)		80	–	35	–	20	–	ns
t_{MED2}	$\overline{ME}$ Delay Time 2		–	85	–	60	–	50	ns
t_{RDD2}	$\overline{RD}$ Delay Time 2		–	85	–	60	–	50	ns
t_{LD2}	$\overline{LIR}$ Delay Time 2		–	100	–	80	–	70 (Note)	ns
t_{DRS}	Data Read Set-up Time		50	–	40	–	30	–	ns
t_{DRH}	Data Read Hold Time		0	–	0	–	0	–	ns
t_{STD1}	ST Delay Time 1		–	110	–	90	–	70	ns
t_{STD2}	ST Delay Time 2		–	110	–	90	–	70	ns
t_{WS}	$\overline{WAIT}$ Set-up Time		80	–	40	–	40	–	ns
t_{WH}	$\overline{WAIT}$ Hold Time		70	–	40	–	40	–	ns
t_{WDZ}	Write Data Floating Delay Time		–	100	–	95	–	70	ns
t_{WRD1}	$\overline{WR}$ Delay Time 1		–	90	–	65	–	60	ns
t_{WDD}	Write Data Delay Time		–	110	–	90	–	80	ns
t_{WDS}	Write Data Set-up Time ($\overline{WR}$ ↓)		60	–	40	–	20	–	ns
t_{WRD2}	$\overline{WR}$ Delay Time 2		–	90	–	80	–	60	ns
t_{WRP}	$\overline{WR}$ Pulse Width		280	–	170	–	130	–	ns

Note: For a loading capacitance of less than or equal to 40 picofarads and operating temperature from 0 to 50 degrees, substract 10 nanoseconds from the value given in the maximum columns.

Symbol	Item		HD647180X-4 Min	HD647180X-4 Max	HD647180X-6 Min	HD647180X-6 Max	HD647180X-8 Min	HD647180X-8 Max	Unit
t_{WDH}	Write Data Hold Time ($\overline{WR}$ ↑)		60	—	40	—	15	—	ns
t_{IOD1}	$\overline{IOE}$ Delay Time 1	$\overline{IOC}$=1	—	85	—	60	—	50	ns
		$\overline{IOC}$=0	—	85	—	65	—	60	
t_{IOD2}	$\overline{IOE}$ Delay Time 2		—	85	—	60	—	50	ns
t_{IOD3}	$\overline{IOE}$ Delay Time 3 ($\overline{LIR}$ ↓)		540	—	340	—	250	—	ns
t_{INTS}	$\overline{INT}$ Set-up Time (ϕ ↓)		80	—	40	—	40	—	ns
t_{INTH}	$\overline{INT}$ Hold Time (ϕ ↓)		70	—	40	—	40	—	ns
t_{NMIW}	$\overline{NMI}$ Pulse Width		120	—	120	—	100	—	ns
t_{BRS}	$\overline{BUSREQ}$ Set-up Time (ϕ ↓)		80	—	40	—	40	—	ns
t_{BRH}	$\overline{BUSREQ}$ Hold Time (ϕ ↓)		70	—	40	—	40	—	ns
t_{BAD1}	$\overline{BUSACK}$ Delay Time 1		—	100	—	95	—	70	ns
t_{BAD2}	$\overline{BUSACK}$ Delay Time 2		—	100	—	95	—	70	ns
t_{BZD}	Bus Floating Delay Time		—	130	—	125	—	90	ns
t_{MEWH}	$\overline{ME}$ Pulse Width (HIGH)		200	—	110	—	90	—	ns
t_{MEWL}	$\overline{ME}$ Pulse Width (LOW)		210	—	125	—	100	—	ns
t_{RFD1}	$\overline{REF}$ Delay Time 1		—	110	—	90	—	80	ns
t_{RFD2}	$\overline{REF}$ Delay Time 2		—	110	—	90	—	80	ns
t_{HAD1}	$\overline{HALT}$ Delay Time 1		—	110	—	90	—	80	ns
t_{HAD2}	$\overline{HALT}$ Delay Time 2		—	110	—	90	—	80	ns
t_{DRQS}	$\overline{DREQi}$ Set-up Time		80	—	40	—	40	—	ns
t_{DRQH}	$\overline{DREQi}$ Hold Time		70	—	40	—	40	—	ns
t_{TED1}	$\overline{TENDi}$ Delay Time 1		—	85	—	70	—	60	ns
t_{TED2}	$\overline{TENDi}$ Delay Time 2		—	85	—	70	—	60	ns
t_{ED1}	Enable Delay Time 1		—	100	—	95	—	70	ns
t_{ED2}	Enable Delay Time 2		—	100	—	95	—	70	ns
P_{WEH}	E Pulse Width (HIGH)		150	—	75	—	65	—	ns
P_{WEL}	E Pulse Width (LOW)		300	—	180	—	130	—	ns

		HD647180X-4		HD647180X-6		HD647180X-8		
Symbol	Item	Min	Max	Min	Max	Min	Max	Unit
t_{Er}	Enable Rise Time	—	25	—	20	—	20	ns
t_{Ef}	Enable Fall Time	—	25	—	20	—	20	ns
t_{TOD}	Timer Output Delay Time	—	300	—	300	—	200	ns
t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	200	—	200	—	200	ns
t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5tcyc + 300	—	7.5tcyc + 300	—	7.5tcyc + 200	ns
t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	1	—	tcyc
t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	1	—	tcyc
t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	1	—	tcyc
t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	1	—	tcyc
t_{RES}	$\overline{\text{RESET}}$ Set-up Time	120	—	120	—	100	—	ns
t_{REH}	$\overline{\text{RESET}}$ Hold Time	80	—	80	—	70	—	ns
t_{OSC}	Oscillator Stabilization Time	—	20	—	20	—	20	ms
t_{EXr}	External Clock Rise Time (EXTAL)	—	25	—	25	—	25	ns
t_{EXf}	External Clock Fall Time (EXTAL)	—	25	—	25	—	25	ns
t_{Rr}	$\overline{\text{RESET}}$ Rise Time	—	50	—	50	—	50	ms
t_{Rf}	$\overline{\text{RESET}}$ Fall Time	—	50	—	50	—	50	ms
t_{Ir}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	—	100	—	100	—	100	ns
t_{If}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	—	100	—	100	—	100	ns
t_{PWD}	Port Data Output Delay Time	—	110	—	90	—	80	ns
t_{PDSU}	Port Data Input Setup Time	80	—	50	—	50	—	ns
t_{PDH}	Port Data Input Hold Time	60	—	40	—	40	—	ns

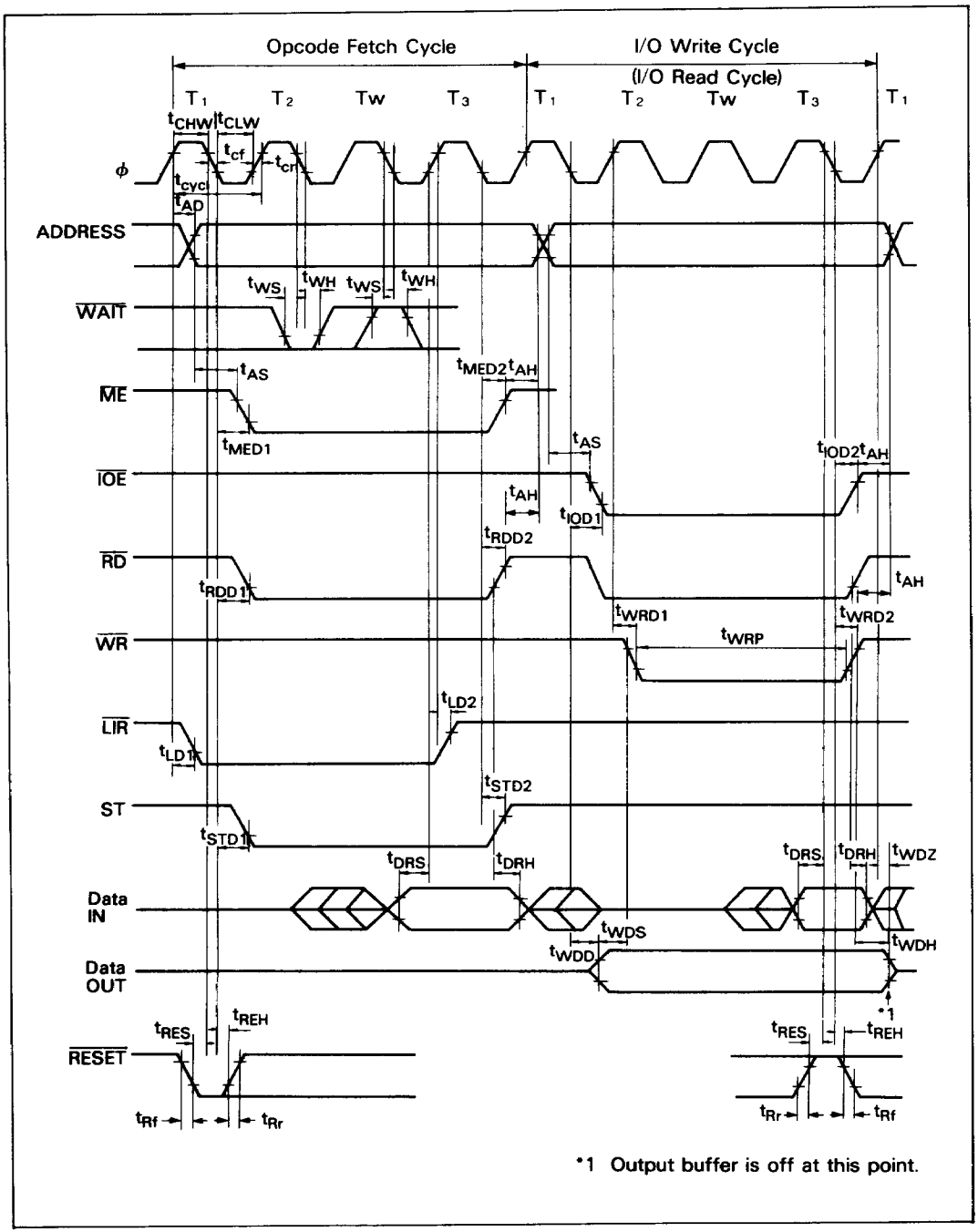

Figure 23-1. CPU Timing (Opcode Fetch Cycle, I/O Write Cycle, I/O Read Cycle)

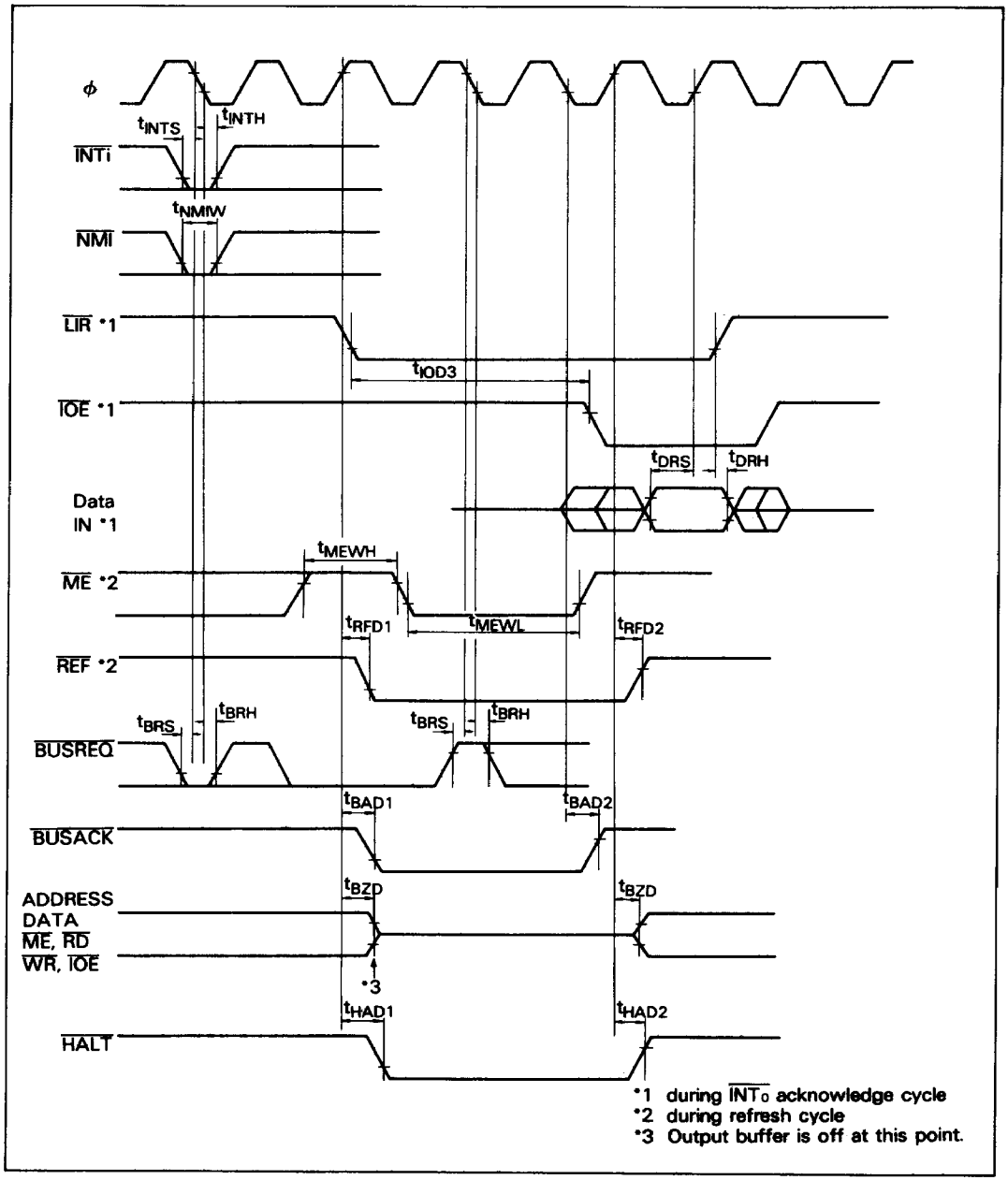

Figure 23-2. CPU Timing ($\overline{INT_0}$ Acknowledge Cycle, Refresh Cycle, Bus Release Mode, Halt Mode, Sleep Mode, System Stop Mode)

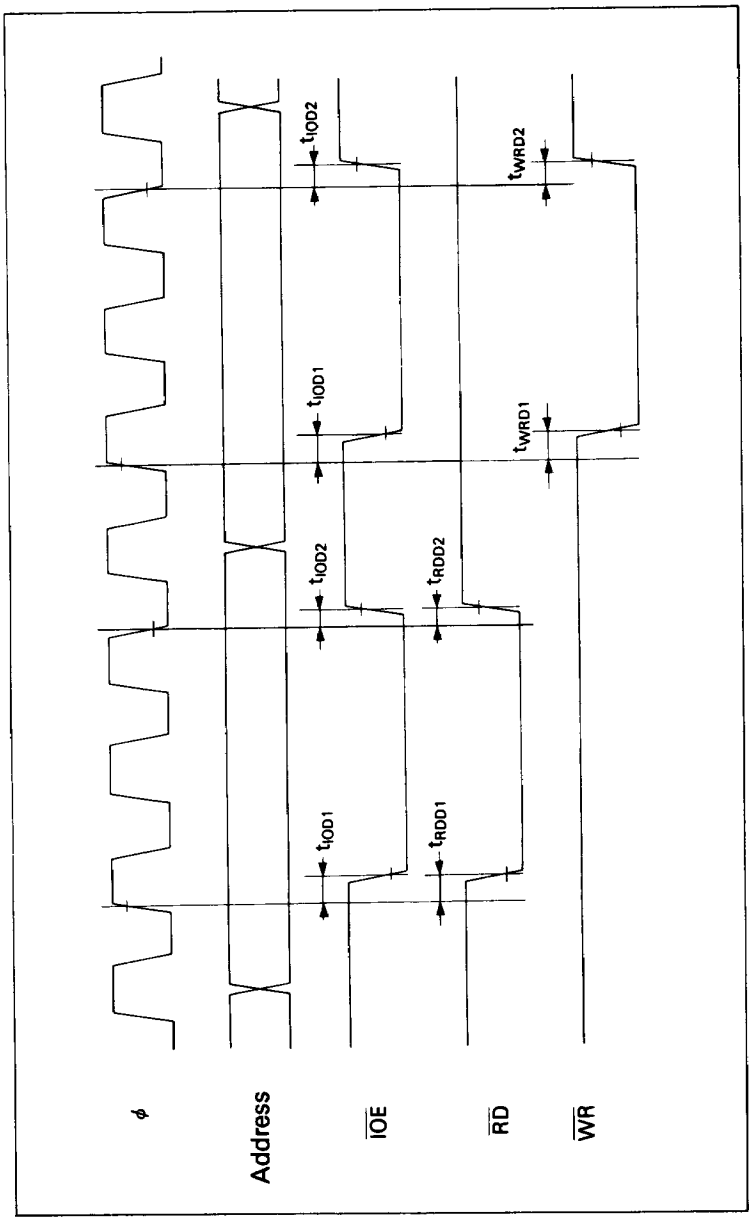

Figure 23-3. CPU Timing ($\overline{IOC}$ = 0)

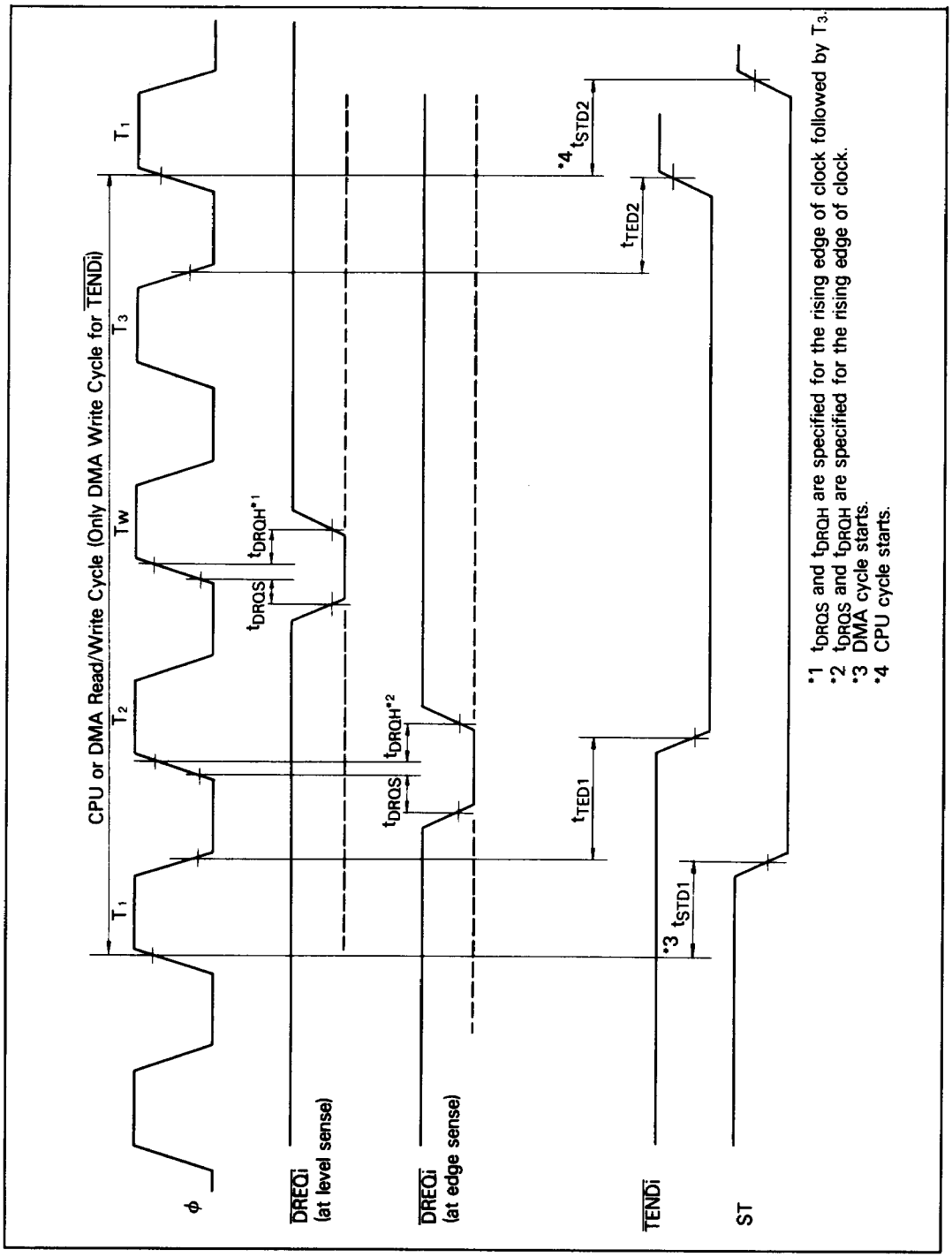

Figure 23-4. DMA Control Signals

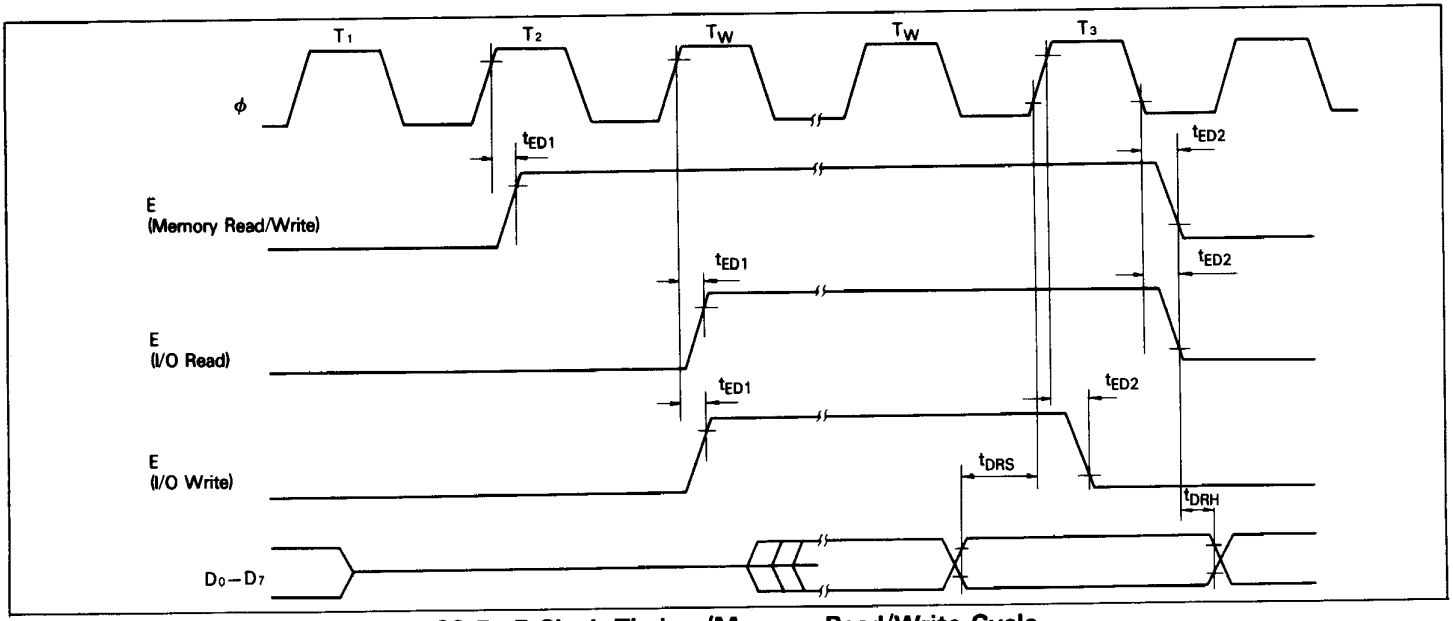

Figure 23-5. E Clock Timing (Memory Read/Write Cycle, I/O Read/Write Cycle)

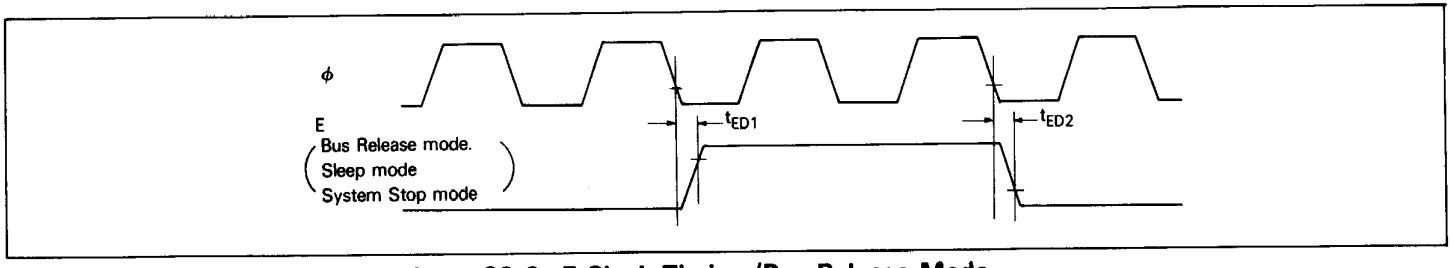

Figure 23-6. E Clock Timing (Bus Release Mode, Sleep Mode, System Stop Mode)

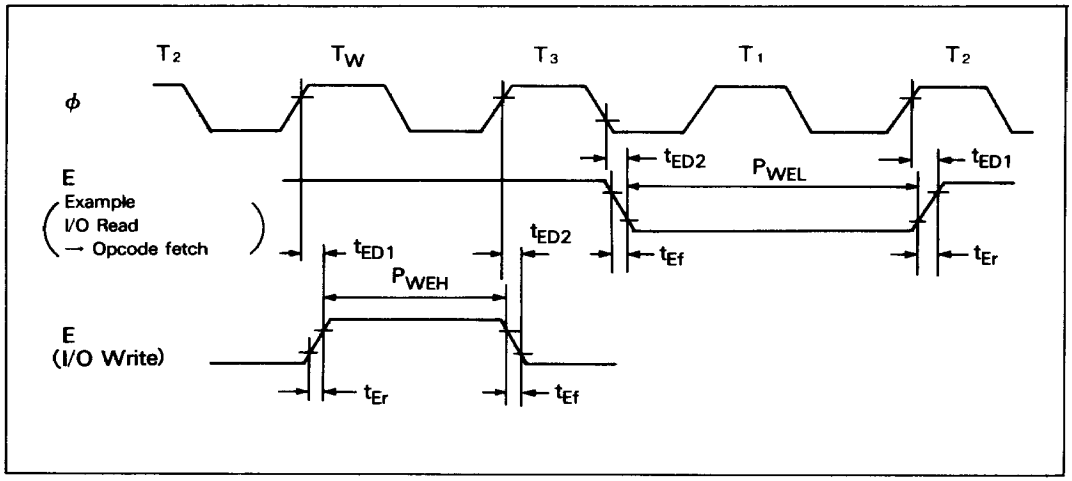

Figure 23-7. E Clock Timing (Minimum Timing Example of P_{WEL} and P_{WEH})

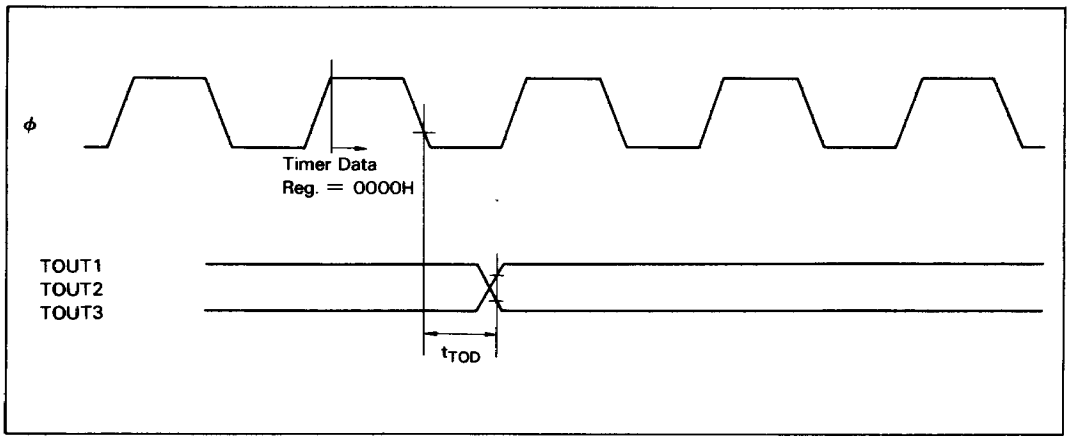

Figure 23-8. Timer Output Timing

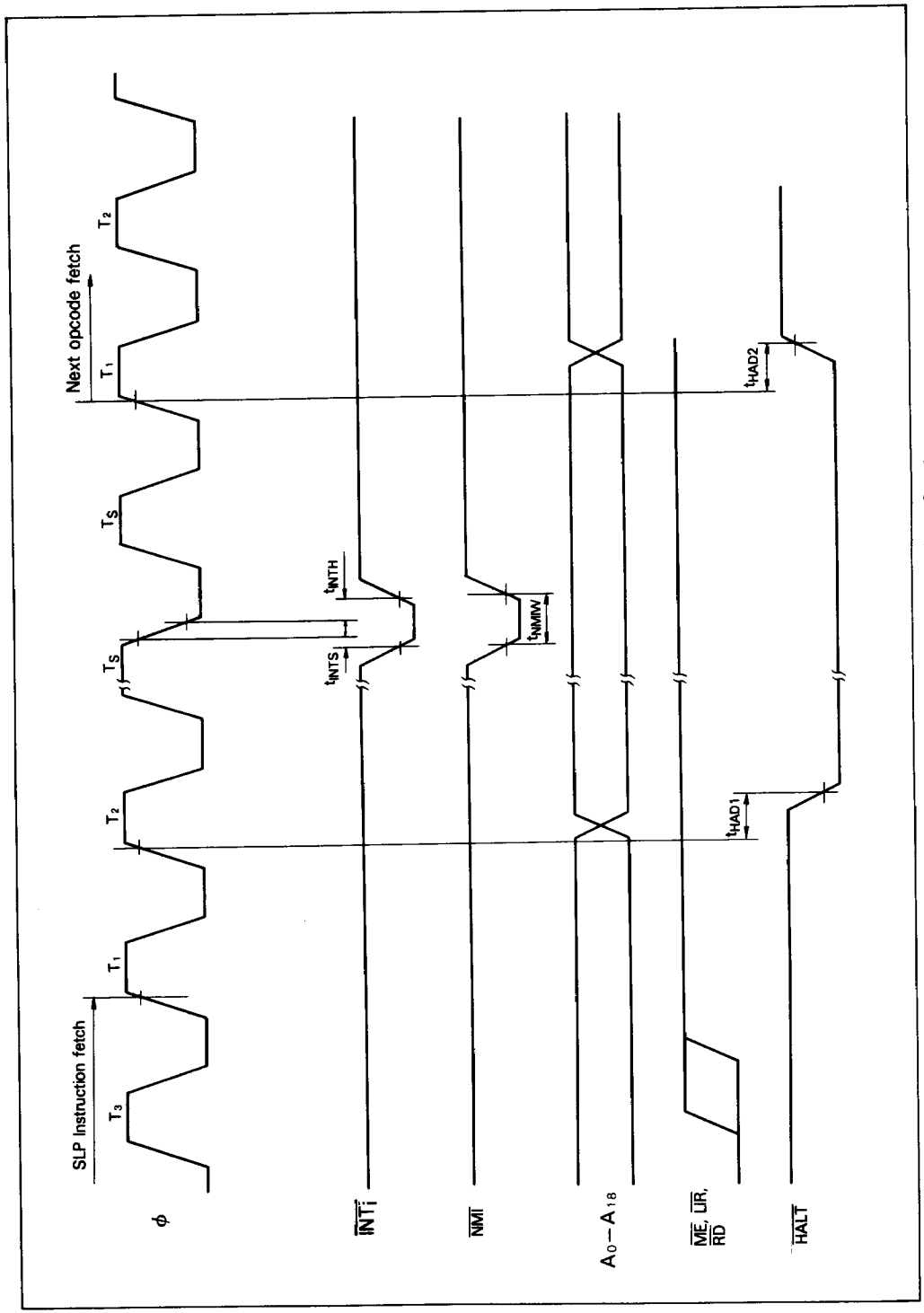

Figure 23-9. SLP Execution Cycle

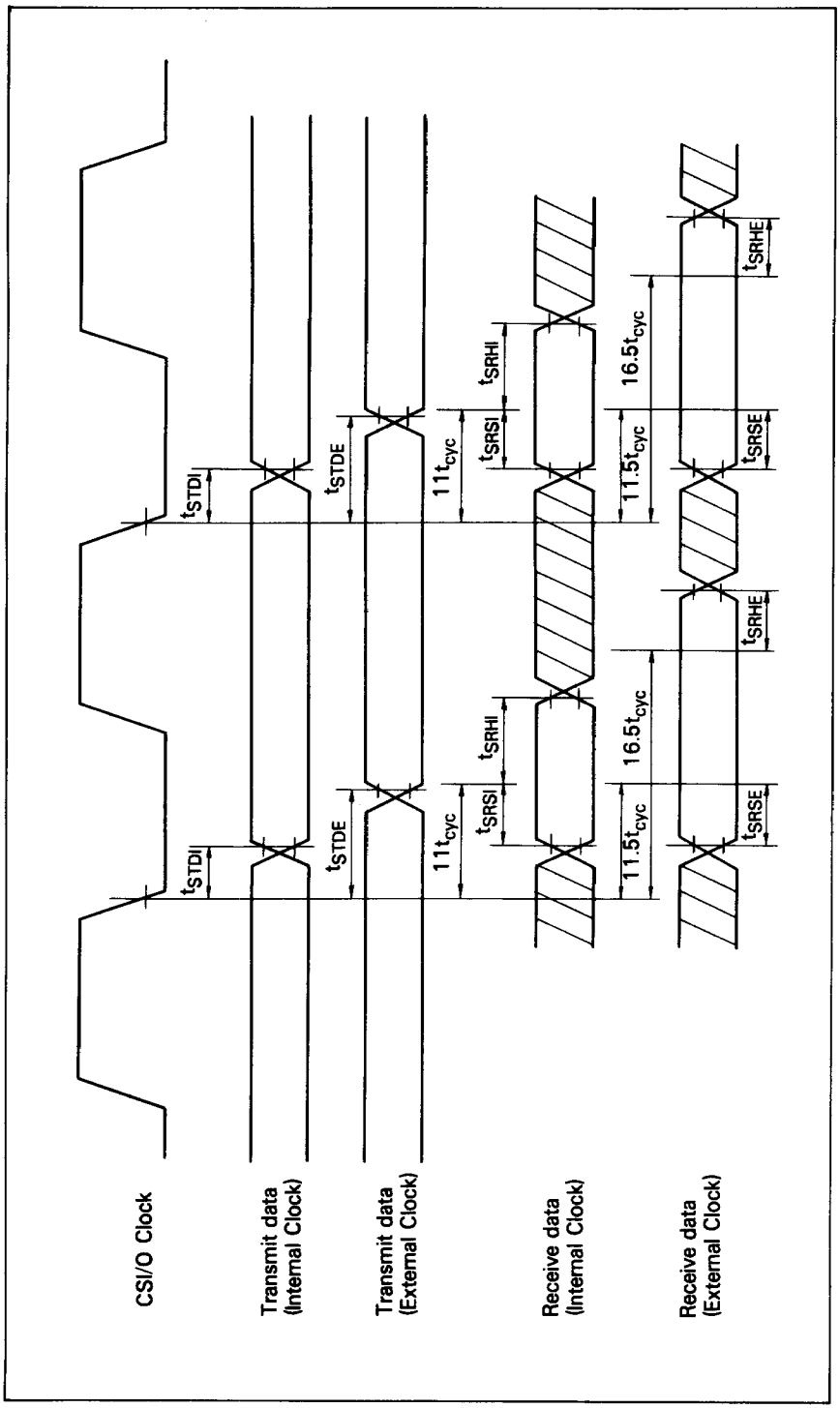

Figure 23-10. CSI/O Receive/Transmit Timing

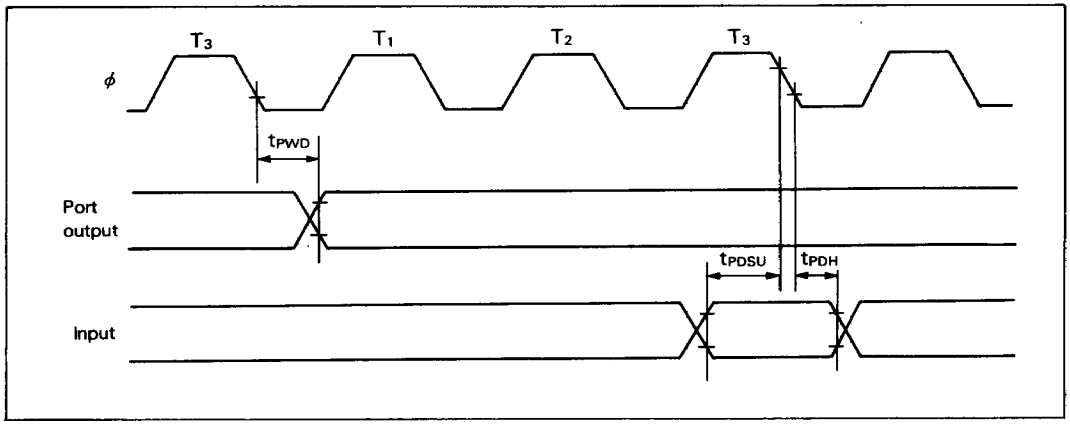

Figure 23-11. Port Input and Output Timing

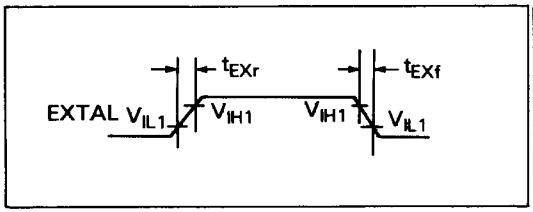

Figure 23-12. External Clock Rise Time and Fall Time

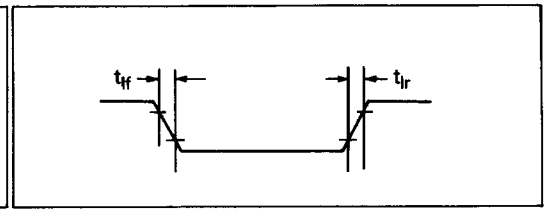

Figure 23-13. Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)

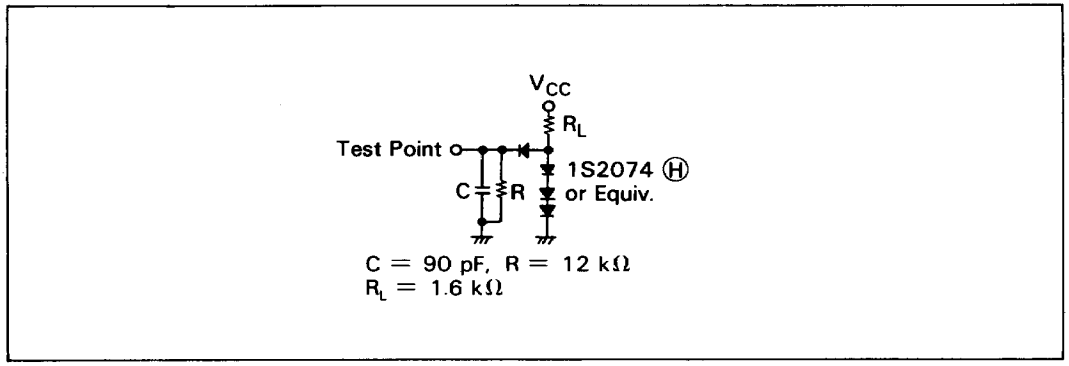

Figure 23-14. Bus Timing Test Load (TTL Load)

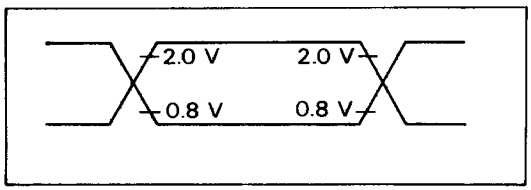

Figure 23-15. Reference Level (Input)

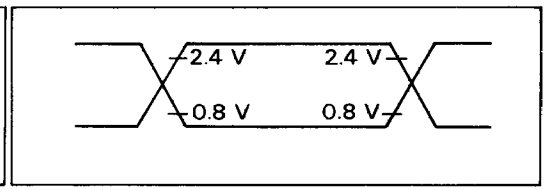

Figure 23-16. Reference Level (Output)