CS-541

Read Data Processor

Description

The CS-541 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals. The circuit will handle data rates up to 15 Megabits/sec.

In read mode the CS-541 provides amplification and qualification of head preamplifier outputs. Pulse qualification is achieved using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry.

The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

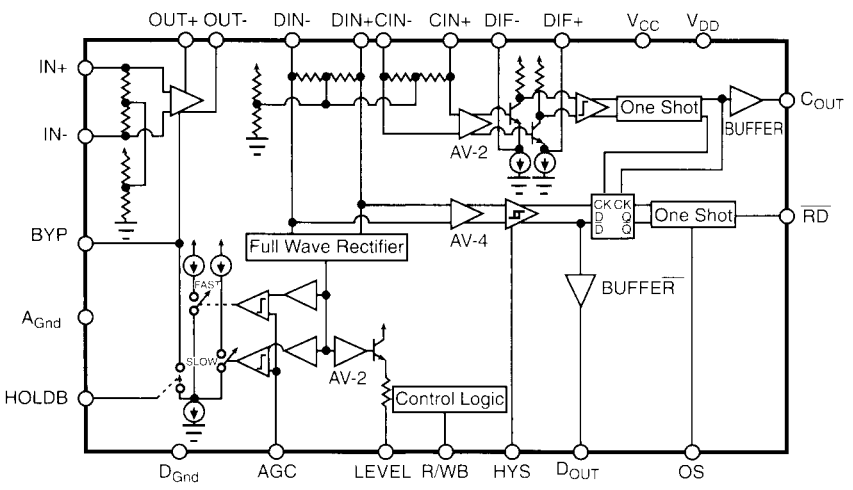
In write mode the circuitry is disabled and the AGC gain stage input impedance switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition.

The CS-541 requires +5V and +12V power supplies and is available in a 24 pin DIP, 24 pin SO and a 28 pin PLCC.

Absolute Maximum Ratings

5V Supply Voltage, V_{CC} 6V
12V Supply Voltage, V_{DD} 14V
Storage Temperature ..... -65°C to 150°C
Lead Temperature ..... 260°C
R/W, IN+, IN-, HOLS ..... -0.3V to V_{CC} + 0.3V
RD ..... -0.3V to V_{CC} + 0.3V or +12mA
All others ..... -0.3V to V_{CC} + 0.3V
*Operation above these rating may cause permanent damage to device.

Block Diagram

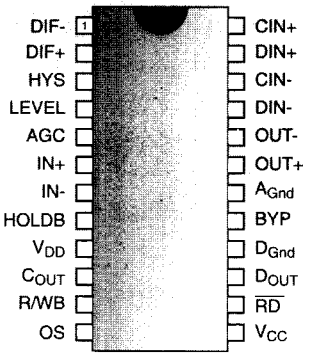


Features

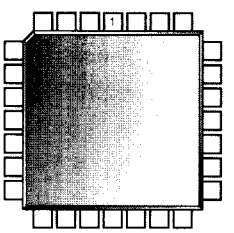
- **Level Qualification Supports High Resolution MFM and RLL Encoded Data Retrieval**
- **Wide Bandwidth AGC Input Amplifier**
- **Supports Data Rates Up to 15 Megabits/sec**
- **Standard 12V ± 10% and 5V ± 10% Supplies**
- **Supports Embedded Servo Pattern Decoding**
- **Write to Read Transient Suppression**
- **Fast and Slow AGC Attack Regions for Fast Transient Recovery**

Package Options

24-Pin PDIP, SO



28-Lead PLCC



CSC™ CHERRY SEMICONDUCTOR

Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Fax (401)885-5786
Telex WUI 6817157

Electrical Characteristics: $4.5V \le V_{CC} \le 5.5V$, $10.8V \le V_{DD} \le 13.2V$, $25°C \le T_J \le +135°C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Supply					
I_{CC}-V_{CC} Supply Current	Outputs unloaded	–	–	14	mA
I_{DD}-V_{DD} Supply Current	Outputs unloaded	–	–	70	mA
■ Logic Signals					
VIL-Input Low Voltage		-0.3	–	0.8	V
VIH-Input High Voltage		2.0	–	–	V
IIL-Input Low Current	VIL = 0.4V	0.0	–	-0.4	mA
IIH-Input High Current	VIL = 2.4V	–	–	100	µA
VOL-Output Low Voltage	IOL = 4.0mA	–	–	0.4	V
VOH-Output High Voltage	IOH = -400µA	2.4	–	–	V
■ Mode Control					
Read to Write Transition Time		–	–	1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2	–	3.0	µs
Read to Hold Transition Time		–	–	1.0	µs
■ Write Mode					
Common Mode Input Impedance (both sides)	R/WB Pin = low	–	250	–	Ω
■ Read Mode					
AGC Amplifier Unless otherwise specified IN+ and IN- are AC coupled, OUT+ and OUT- are loaded differentially with 600Ω and each side is loaded with >10pF to GND, a 2000pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.					
Differential Input Resistance	V(IN+ - IN-) = 100mVpp @ 2.5MHz		5		kΩ
Differential Input Capacitance	V(IN+ - IN-) = 100MVpp @ 2.5MHz			10	pF
Common Mode Input Impedance (both sides)	R/WB pin high R/WB pin low		1.8 0.25		kΩ kΩ
Gain Range	1.0Vpp ≤ V(OUT+ – OUT-) = 2.5Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/√Hz
Bandwidth	Gain set to maximum -3dB point	30			MHz
Maximum Output Voltage Swing		3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND	±3.2			mA
Output Resistance		13		34	Ω
Output Capacitance				15	pF
(Din+ – DIN-) Input Voltage Swing VS AGC Input Level	30mVpp ≤ V(IN+ – IN-) ≤ 550mVpp 0.5Vpp≤ V(DIN+ – DIN-) ≤ 1.5Vpp	0.37		0.56	Vpp/V
(Din+ – DIN-) Input Voltage Swing Variation	30mVpp V(IN+ – IN-) ≤ 550mVpp AGC Fixed, over suply & temp.			8	%
Gain Decay time (T_D) 2.5MHz, V_{OUT} to 90% of final value Fig. 1A	V_{IN} = 300mVpp- > 150mVpp at		50		µs

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Read Mode (continued)					
Gain Attack Time (T_A)	From Write to Read transition to V_{OUT} at 110% of final value V_{IN} = 400mVpp @ 2.5MHz. Fig. 1B		4		µs
Fast AGC Capacitor Charge Current	V(DIN+ = DIN-) = 1.6V V(AGC) = 2.2V	1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+ - DIN-)}{V(DIN+ - DIN-) \text{ Final}}$		1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode Hold Mode	 -0.2	 4.5 	 +0.2	 µA µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100mVpp @ 5MHz, gain at max.	40			dB
PSRR (Input Referred)	VCC or VDD = 100mVpp @ 5MHz, gain at max	30			dB
■ Hysteresis Comparator					
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ - DIN-) = 100mVpp@2.5MHz	5		11	kΩ
Differential Input Capacitance	V(DIN+ - DIN-) = 100mVpp@2.5MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		kΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5kΩ across DIN+, DIN-			10	mV
Peak Hysteresis Voltage vs. HYS pin voltage (input referred)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16		0.25	V/V V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Level Pin Output Voltage vs. V(DIN+ – DIN-)	0.6 < | V (DIN+ – DIN-) | < 1.3Vpp 10kΩ from LEVEL pin to GND	1.5		2.5	V/Vpp
LEVEL Pin Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5mA		180		Ω
D_{OUT} Pin Output Low Voltage	0.0 ≤ I0L ≤ 0.5mA	V_{DD}-4.0		V_{DD} -2.8	V
D_{OUT} Pin Output High Voltage	0.0 ≤ I0H ≤ 0.5mA	V_{DD} -2.5		V_{DD} -1.8	V
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-)=100mVpp @ 2.5MHz	5.8		11.0	kΩ
Differential Input Capacitance	V(CIN+ – CIN-)=100mVpp @ 2.5MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		kΩ
Voltage Gain From CIN+/- to DIF+/-	R(DIF+ to DIF-) = 2kΩ	1.7		2.2	V/V
DIF+ to DIF- Pin current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF = AC coupled			10.0	mV

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Hysteresis Comparator					
C_{OUT} Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5mA		V_{DD} -3.0		V
C_{OUT} Pin Output Pulse Voltage, V(high) - V(low)	0.0 ≤ IOH ≤ 0.5mA		+0.4		V
C_{OUT} Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5mA		30		ns

Output Data Characteristics (Ref. Fig. 2) Unless otherwise specified V(CIN+ - CIN-) = V(DIN+ - DIN-) = 1.0Vpp AC coupled since wave at 2.5MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65pF, V (Hys) = 1.8DC, a 60pF capacitor is connected between OS and V_{CC}, RD- is loaded with a 4kΩ resistor to V_{CC} and a 10pF capacitor to GND.

D-Flip-Flop Set Up Time (TD1)	Min. delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ - DIF-) reaching a peak	0	–	–	ns
Propogation Delay (TD3)		–	–	110	ns
Output Data Pulse Width Variation	TD5 = 670 COS, 50 pF ≤ COS ≤ 200pF	–	–	±15	%
Logic Skew TD3 – TD4		–	–	3	ns
Output Rise Time	VOH = 2.4V	–	–	14	ns
Output Fall Time	VOL = 0.4V	–	–	18	ns

Package Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
24L PDIP, 24L SO	28L PLCC		
13	15	V_{CC}	5 volt power supply.
9	10	V_{DD}	12 volt power supply.
18	21	A_{Gnd}	Analog and Digital ground pins.
16	19	D_{Gnd}	Analog and Digital ground pins.
11	12	R/WB	TTL compatible read/write control pin.
6	7	IN+	Analog signal input pins.
7	8	IN-	Analog signal input pins.
19	22	OUT+	AGC Amplifier output pins.
20	23	OUT-	AGC Amplifier output pins.
17	20	BYP	The AGC timing capacitor is tied between this pin and AGND.
8	9	HOLD B	TTl compatible pin that holds the AGC gain when pulled low.
5	6	AGC	Reference input voltage level for the AGC circuit.
23	27	DIN+	Analog input to the hysteresis comparator.
21	24	DIN-	Analog input to the hysteresis comparator.
3	3	HYS	Hysteresis level setting input to the hysteresis comparator.
4	5	LEVEL	Provides rectified signal level for input to the hysteresis comparator.
15	18	D_{OUT}	Buffered test point for monitoring the flip-flop D input
24	28	CIN+	Analog input to the differentiator.
22	26	CIN-	Analog input to the differentiator.

Package Pin Description: continued

PACKAGE PIN #		PIN SYMBOL	FUNCTION
24L PDIP, 24L SO	28L PLCC		
2	2	DIF+	Pins for external differentiating network.
1	1	DIF-	Pins for external differentiating network.
10	11	C_{OUT}	Buffered test point for monitoring the clock input to the flip-flop.
12	13	OS	Connection for read output pulse width setting capacitor.
14	16	$\overline{RD}$	TTL compatible read output.

State Table

R/WB	HOLD B	FUNCTION
1	1	READ – Read amp on, AGC active, Digital section active.
1	0	HOLD – Read amp on, AGC gain held constant, Digital section active.
0	X	WRITE – AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced.

Timing Diagrams

Figure 1: AGC Timing Diagram

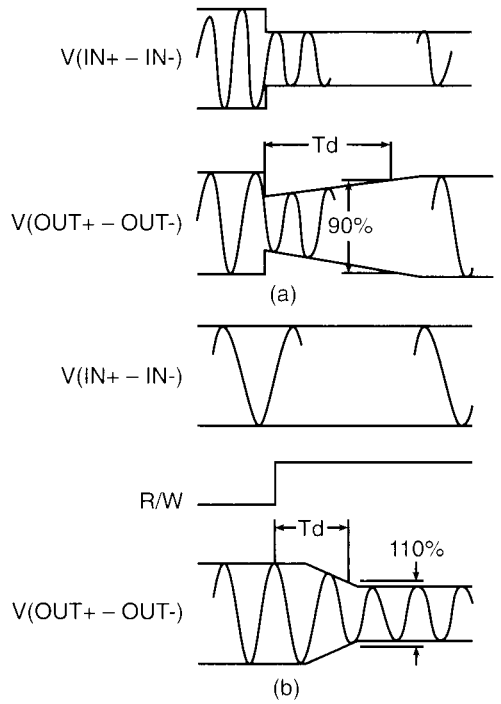
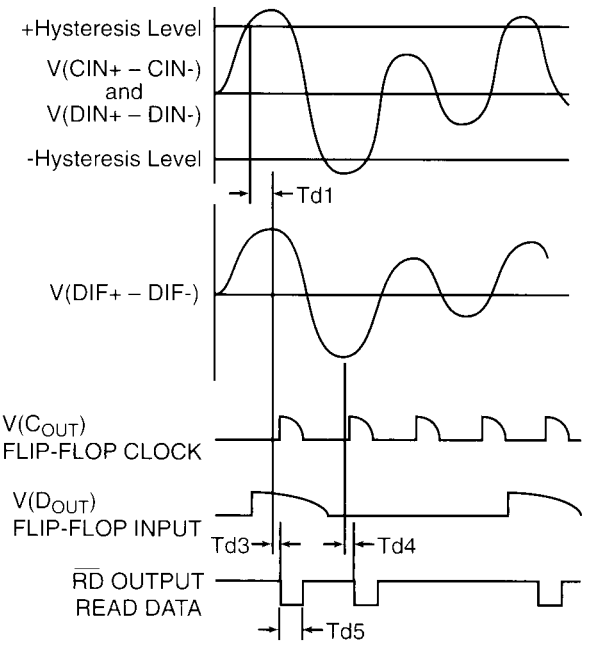
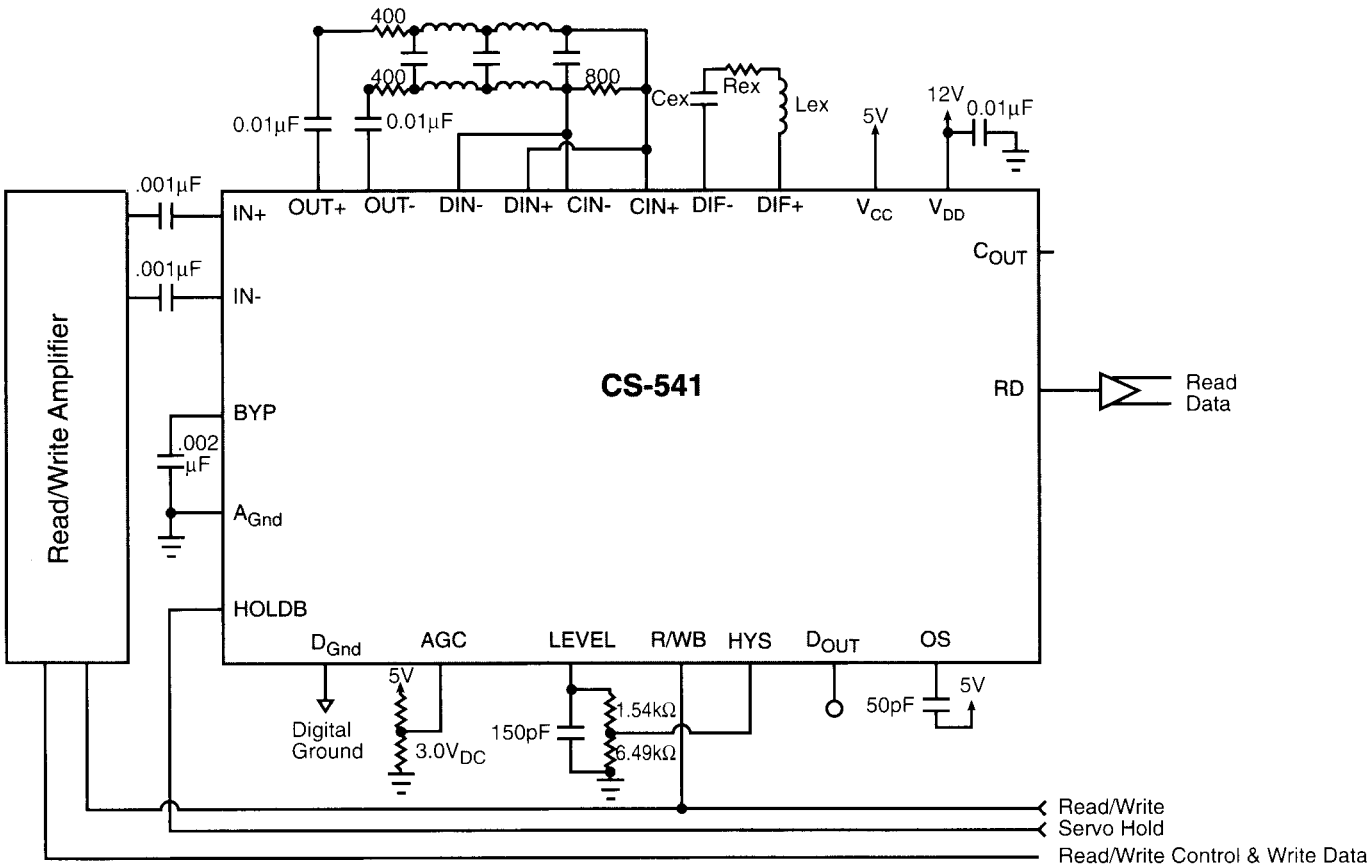


Figure 2: Timing Diagram



Applications Diagram



Note: Circuit traces for the 12V bypass capacitor and the AGC hold capacitor should be as short as possible with both capacitors returned to the Analog Ground pin.

Package Specification

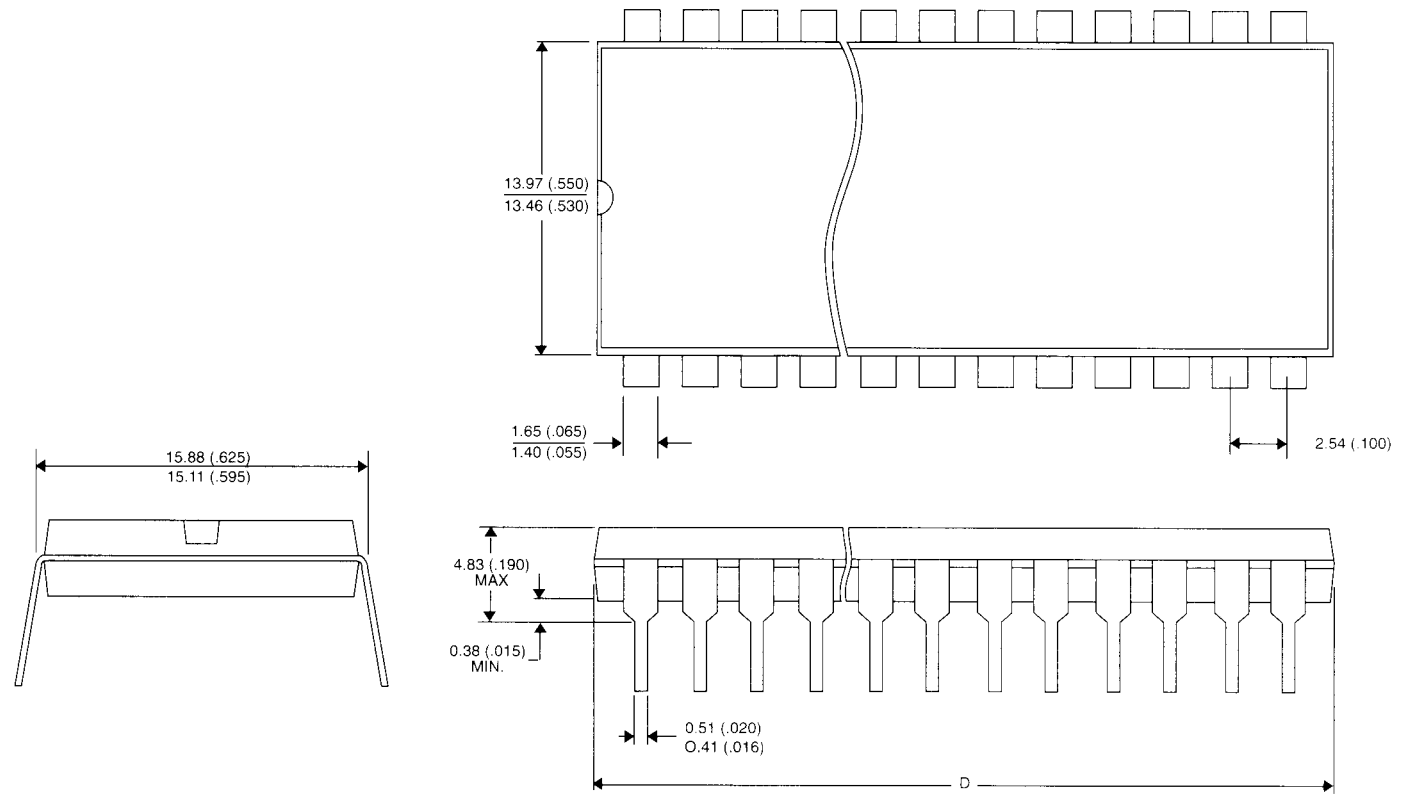
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
24L PDIP	31.88	31.62	1.255	1.245
28L PLCC (A)	12.57	12.32	.495	.485
28L PLCC (B)	11.53	11.43	.454	.450
24L SO	15.54	15.29	.612	.602

PACKAGE THERMAL DATA

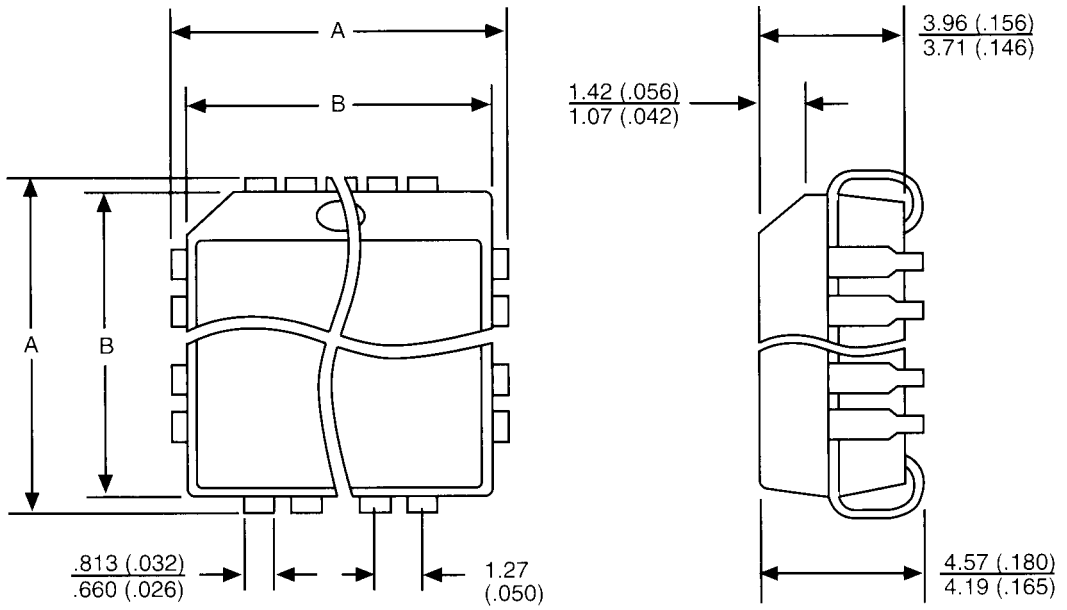
Thermal Data		24 L PDIP	28 L PLCC	24L SO	
$R\Theta_{JC}$	typ	55	18	16	°C/W
$R\Theta_{JA}$	typ	23	70	80	°C/W

24L PDIP

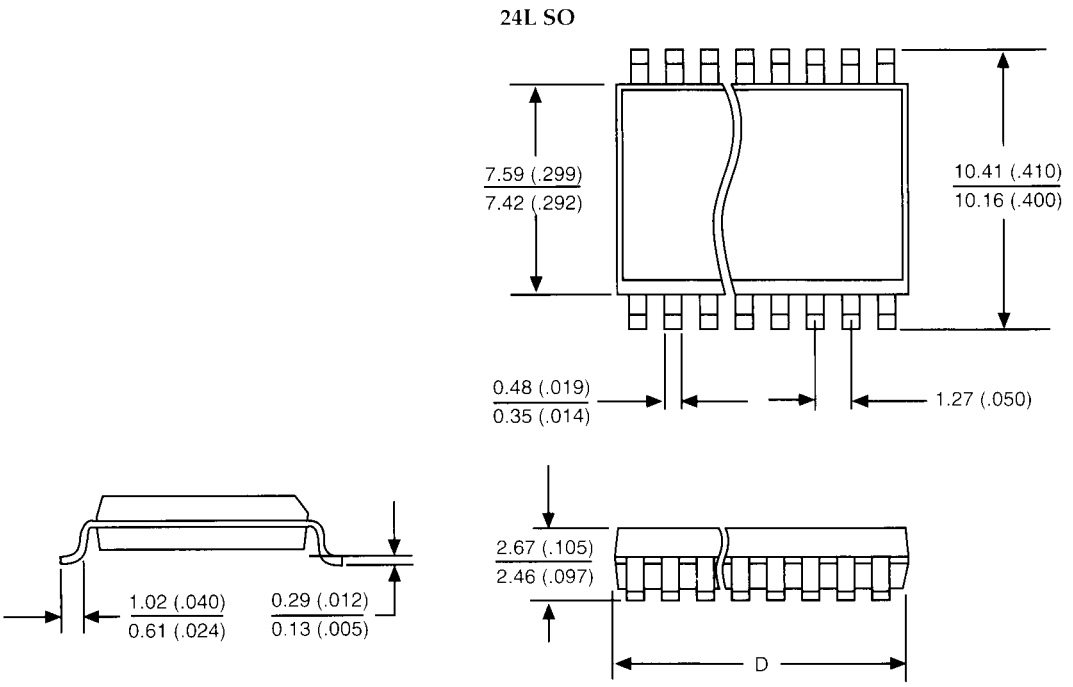


Package Specification: continued

28L PLCC



24L SO



Ordering Information

Part Number	Description
CS-541FN28	28 Lead PLCC
CS-541N24	24 Lead PDIP
CS-541D24	24 Lead SO

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Cherry Semiconductor Corporation
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Tel: (401)885-3600 Fax (401)885-5786
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