CMOS single-chip 8-bit microcontroller

87C654/87C654-16

ORDERING INFORMATION

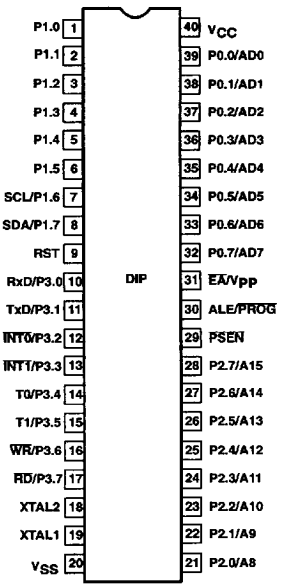
DESCRIPTION	ORDER CODE	PKG DESIGNATOR*
40-Pin Ceramic Dual In-line Package (DIP) with Quartz Window	87C654/BQA 87C654-16/BQA	GDIP1-T40
40-Pin Ceramic Dual In-line Package without Quartz Window	87C654/BQA OT[1] 87C654-16/BQA OT[1]	GDIP1-T40
Ceramic Quad Flat Pack with J-Bend leads and quartz window	87C654/BMA 87C654-16/BMA	GQCC1-J44
Ceramic Quad Flat Pack with J-Bend leads and without quartz window	87C654/BMA OT[1] 87C654-16/BMA OT[1]	GQCC1-J44

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

FEATURES

- 80C51 central processing unit
- 16k × 8 EPROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP PIN FUNCTIONS

DESCRIPTION

The 87C654/-16 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C654/-16 has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C654/-16 contains a 16k × 8 EPROM, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C654/-16 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

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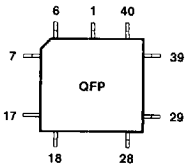
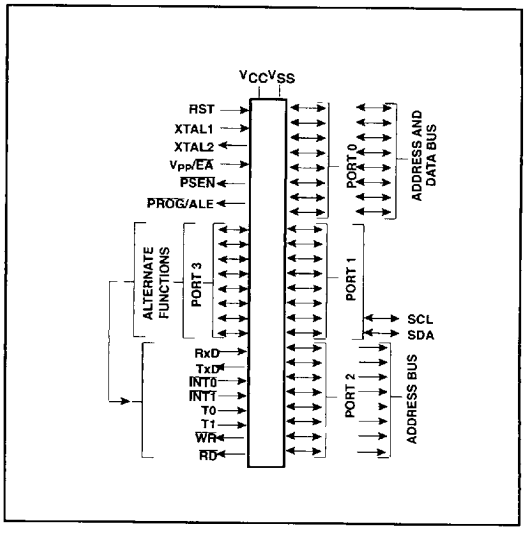
QFP PIN FUNCTIONS

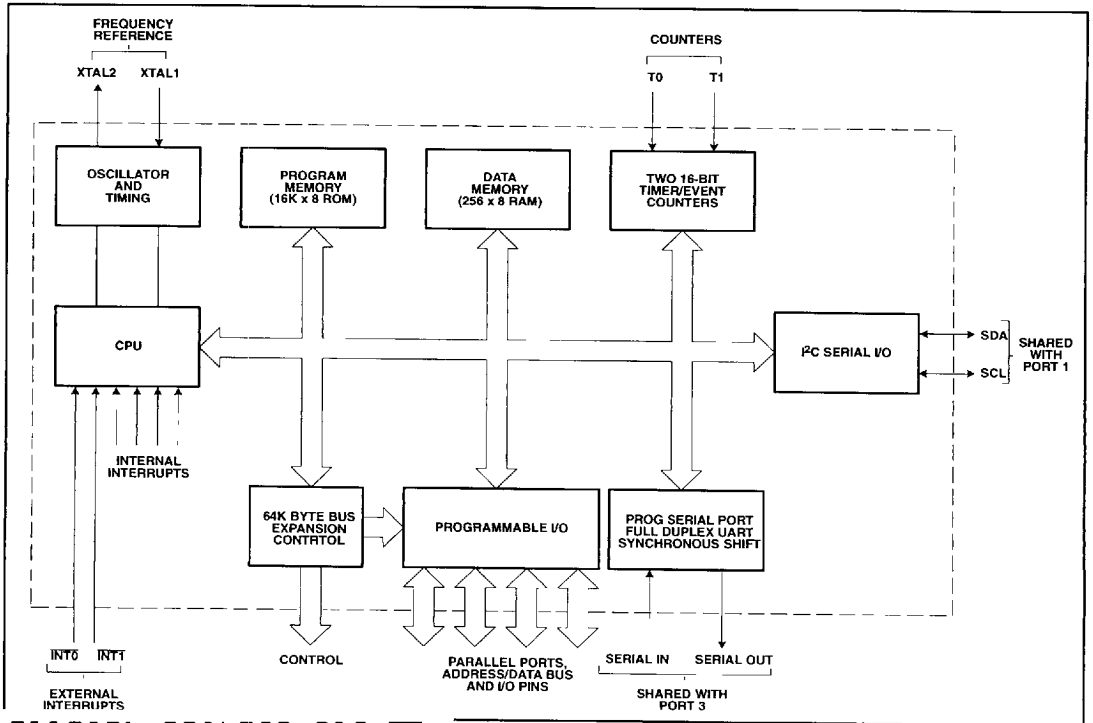


Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE/$\overline{PROG}$
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$/V_{PP}
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{CC}

LOGIC SYMBOL



BLOCK DIAGRAM



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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	QFP		
V_{SS}	20	22	I	**Ground:** 0V reference.
V_{CC}	40	44	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39-32	43-46	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C654. External pull-ups are required during program verification.
P1.0-P1.7	1-8	2-9	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
P1.6	7	8	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	8	9	I/O	**SDA:** I^2C-bus serial port data line.
P2.0-P2.7	21-28	24-31	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0-P3.7	10-17	11, 13-19	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	I	**RxD (P3.0):** Serial input port
	11	13	O	**TxD (P3.1):** Serial output port
	12	14	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	I	**T0 (P3.4):** Timer 0 external input
	15	17	I	**T1 (P3.5):** Timer 1 external input
	16	18	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	O	**Program Store Enable:** The read strobe to external program memory. When the 87C654 is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE: To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} - 0.5V, respectively.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Serial Control Register (S1CON) - See Table 2

S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2[2]	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC}			f_{OSC} DIVIDED BY
			6MHz	12MHz	16MHz[2]	
0	0	0	23	47	62.5	256[2]
0	0	1	27	54	71	224[2]
0	1	0	31 25	62 5	83.3	192[2]
0	1	1	37	75	100	160[2]
1	0	0	6.25	12.5	17	960
1	0	1	50	100	133[3]	120
1	1	0	100	200[3]	267[3]	60
1	1	1	0.25 < 31.25	0.5 < 62.5	0.67 < 83.3	96 × (256 - (reload value Timer 1)) (Reload value range: 0 - 254 in mode 2)

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ABSOLUTE MAXIMUM RATINGS[4, 5, 6]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	-65 to +150	°C
	Voltage on $\overline{EA}/V_{PP}$ to V_{SS} (87C654 only)	-0.5 to + 13	V
	Voltage on any other pin to V_{SS}	-0.5 to + 6.5	V
	Input, output current on any single pin	±5	mA
	Input, output current on any two pins	±10	mA
	Power dissipation (based on package heat transfer limitations, not device power consumption)	1	W

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –55°C to +125°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[7]	MAX	
V_{CC}	Supply voltage		4.5	4.5	5.5	V
I_{CC}	Power supply current:					
	Active mode @ 16MHz	See note 11		11.5	39	mA
	Idle mode @ 16MHz			1.3	7	mA
	Active mode @ 12MHz				35	mA
	Idle mode @ 12MHz				6	mA
	Power down mode			3.0	200	µA
Inputs						
V_{IL}	Input low voltage, except $\overline{EA}$, P1.6/SCL, P1.7/SDA		-0.5		$0.2V_{CC}$-0.25	V
V_{IL1}	Input low voltage to $\overline{EA}$		-0.5		$0.2V_{CC}$-0.45	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA[12]		-0.5		$0.3V_{CC}$	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA		$0.2V_{CC}$+1.1		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$+0.2		V_{CC}+0.5	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA[12]		$0.7V_{CC}$		6.0	V
$-I_{IL}$	Logical 0 input current, ports 1, 2, 3 except P1.6/SCL, P1.7/SDA	V_{IN} = 0.45V			-75	µA
$-I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	See note 10			-750	µA
I_{IL1}	Input leakage current, port 0, $\overline{EA}$	0.45V<V_I<V_{CC}	–10		10	µA
I_{IL2}	Input leakage current, P1.6/SCL, P1.7/SDA	0V<V_I<6V 0V<V_{CC}<5.5V	–10		10	µA
Outputs						
V_{OL}[8]	Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	V_{CC} = 4.5V; I_{OL} = 100µA I_{OL} = 1.6mA I_{OL} = 3.5mA			0.3 0.45 1.0	V V V
V_{OL1}[8]	Output low voltage, port 0, ALE, $\overline{PSEN}$	V_{CC} = 4.5V; I_{OL} = 200µA I_{OL} = 3.2mA I_{OL} = 7.0mA			0.3 0.45 1.0	V V V
V_{OL2}[8]	Output low voltage, P1.6/SCL, P1.7/SDA	I_{OL} = 3.0mA			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 (except P1.6 and P1.7)	V_{CC} = 4.5V; I_{OH} = –10µA I_{OH} = –30µA I_{OH} = –60µA	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V V V
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)[9]	V_{CC} = 4.5V; I_{OH} = –200µA I_{OH} = –3.2mA I_{OH} = –7.0mA	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V V V
R_{RST}	Internal reset pulldown resistor		50		225	kΩ
C_{IO}	Pin capacitance[16]	Test freq = 1MHz, T_{amb} = 25°C			10	pF

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AC ELECTRICAL CHARACTERISTICS[17]

T_{amb} = -55°C to +125°C, V_{CC} = 5V ±10%, V_{SS} = 0V[13, 14]

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	112		$2t_{CLCL}$-55		ns
t_{AVLL}	1	Address valid to ALE low	43		t_{CLCL}-40		ns
t_{LLAX}	1	Address hold after ALE low	33		t_{CLCL}-50		ns
t_{LLIV}	1	ALE low to valid instruction in		218		$4t_{CLCL}$-115	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	28		t_{CLCL}-55		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	190		$3t_{CLCL}$-50		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		130		$3t_{CLCL}$-120	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		58		t_{CLCL}-25	ns
t_{AVIV}	1	Address to valid instruction in		277		$5t_{CLCL}$-140	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		20		20	ns
Data Memory							
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		242		$5t_{CLCL}$-175	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		82		$2t_{CLCL}$-85	ns
t_{LLDV}	2, 3	ALE low to valid data in		497		$8t_{CLCL}$-170	ns
t_{AVDV}	2, 3	Address to valid data in		565		$9t_{CLCL}$-185	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	203		$4t_{CLCL}$-130		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	33		t_{CLCL}-50		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	33		t_{CLCL}-50		ns
t_{QVWH}	2, 3	Data valid to WR high	433		$7t_{CLCL}$-150		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
External Clock							
t_{CHCX}	4	High time[16]	20		20		ns
t_{CLCX}	4	Low time[16]	20		20		ns
t_{CLCH}	4	Rise time[16]		20		20	ns
t_{CHCL}	4	Fall time[16]		20		20	ns
Shift Register[15]							
t_{XLXL}	5	Serial port clock cycle time[16]	1.0		$12t_{CLCL}$		µs
t_{QVXH}	5	Output data setup to clock rising edge[16]	700		$10t_{CLCL}$-133		ns
t_{XHQX}	5	Output data hold after clock rising edge[16]	50		$2t_{CLCL}$-117		ns
t_{XHDX}	5	Input data hold after clock rising edge[16]	0		0		ns
t_{XHDV}	5	Clock rising edge to input data valid[16]		700		$10t_{CLCL}$-133	ns

NOTES: on following page

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NOTES:
1. Erase characteristics do not apply for one time programming (OT).
2. The CR2 control bit is only implemented on the 16MHz version.
3. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.
4. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
5. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
6. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
7. Typical ratings are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
8. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
9. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
10. Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
11. See Figures 8 through 11 for I_{CC} test conditions.
12. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
13. Parameters are valid over operating temperature range unless otherwise specified.
14. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
15. The shift register has been characterized for the 87C654 only.
16. These values are characterized but not 100% production tested.
17. AC parameters at the maximum rated frequency.

AC SYMBOL DESIGNATIONS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples:

t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

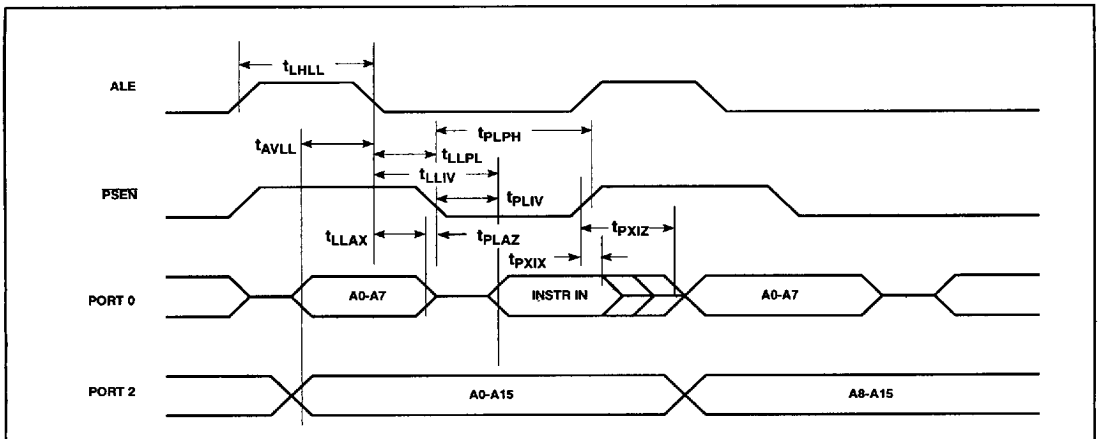

Figure 1. External Program Memory Read Cycle

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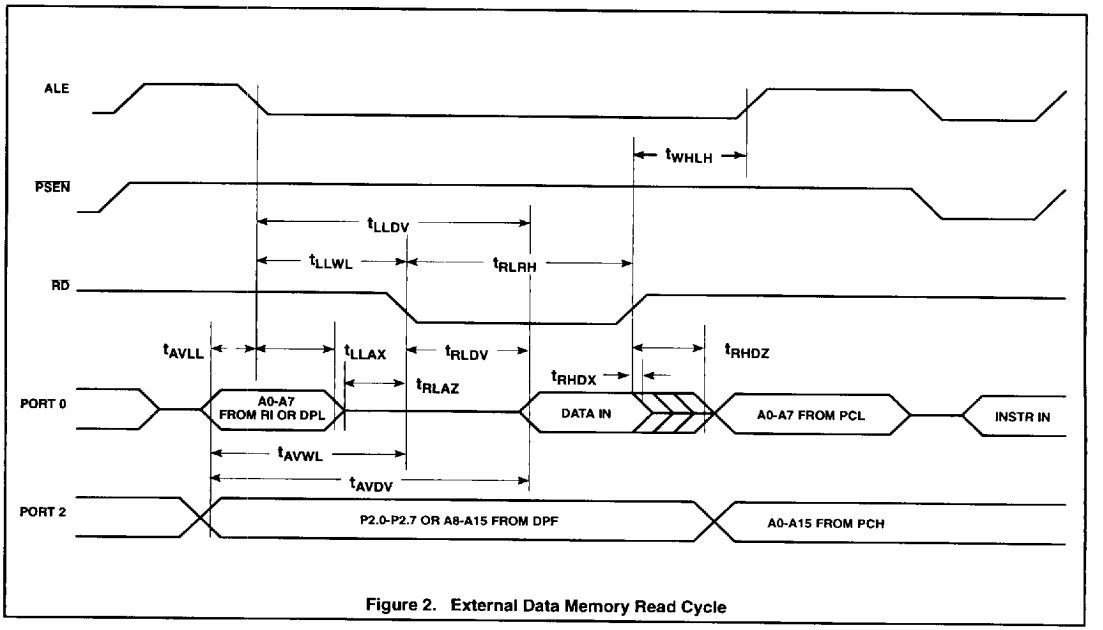

Figure 2. External Data Memory Read Cycle

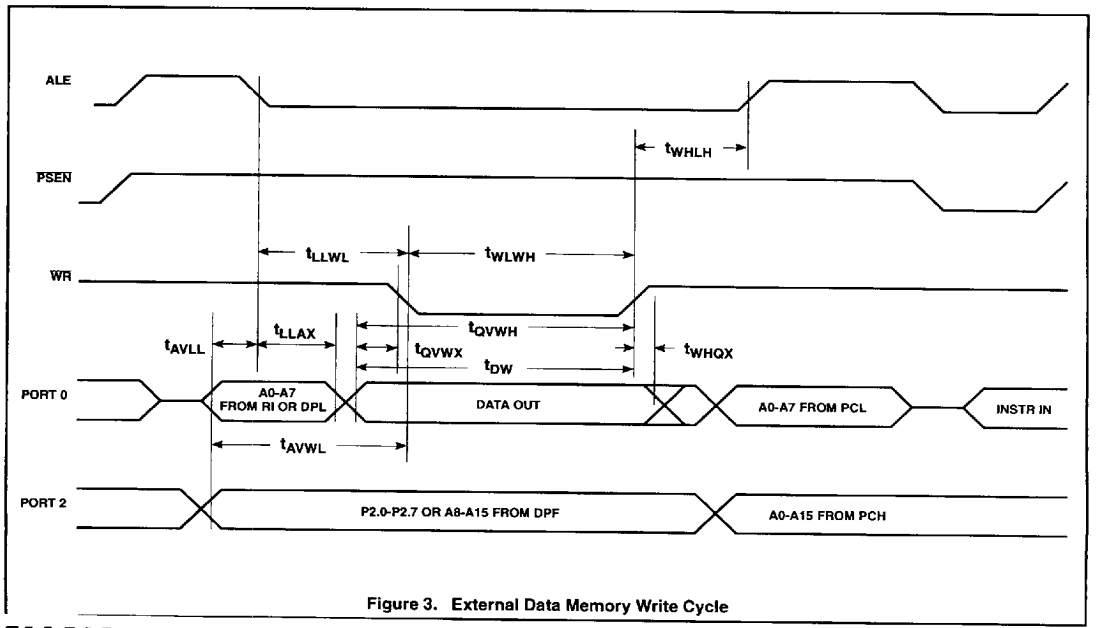

Figure 3. External Data Memory Write Cycle

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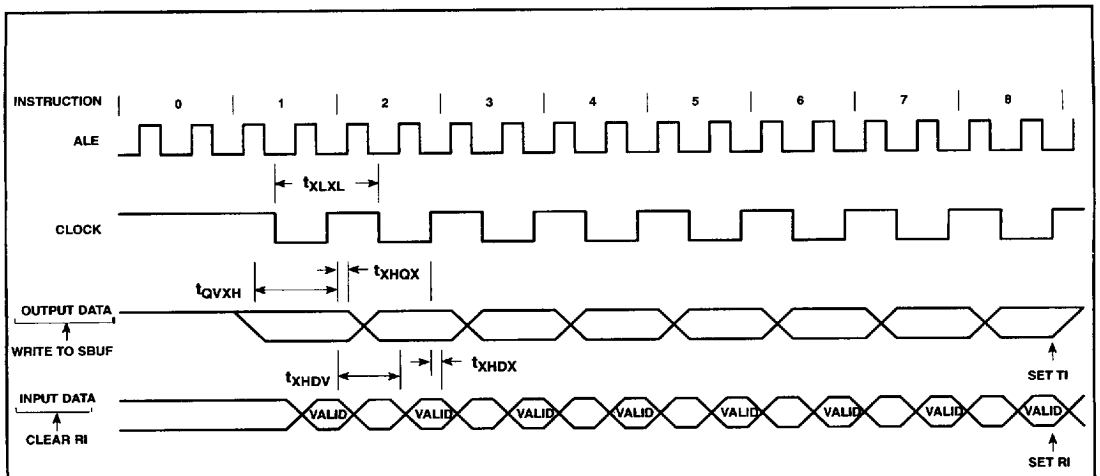


Figure 4. Shift Register Mode Timing

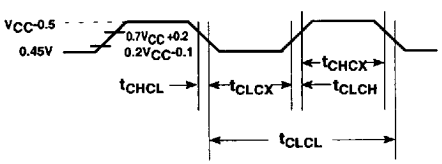
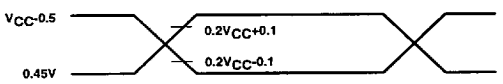
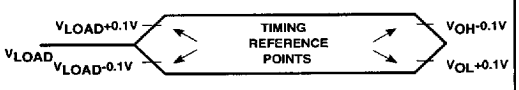


Figure 5. External Clock Drive



NOTE:
AC INPUTS DURING TESTING ARE DRIVEN AT V_{CC}-0 5 FOR A LOGIC '1' AND 0 45V FOR A LOGIC '0' TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN FOR A LOGIC '1' AND V_{IL} MAX FOR A LOGIC '0'

Figure 6. AC Testing Input/Output



NOTE:
FOR TIMING PURPOSES, A PORT IS NO LONGER FLOATING WHEN A 100MV CHANGE FROM LOAD VOLTAGE OCCURS AND BEGINS TO FLOAT WHEN A 100mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS $I_{OH}/I_{OL} \geq \pm$ 20mA

Figure 7. Float Waveform

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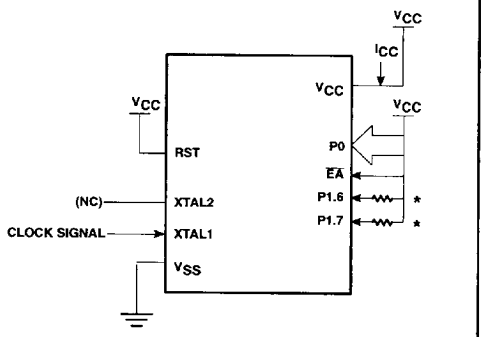
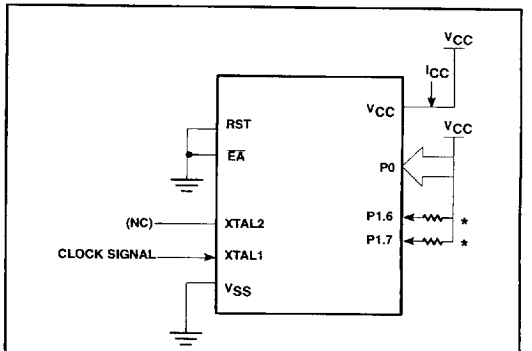


* NOTE:
Ports 1.6 and 1.7 should be connected to V_{CC} through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_{OL1} specification

Figure 8. I_{CC} Test Condition, Active Mode
All other pins are disconnected



* NOTE:
Ports 1.6 and 1.7 should be connected to V_{CC} through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_{OL1} specification

Figure 9. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

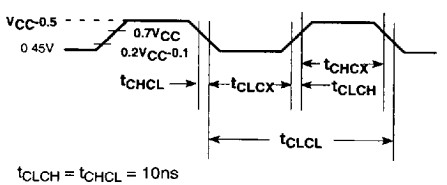


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

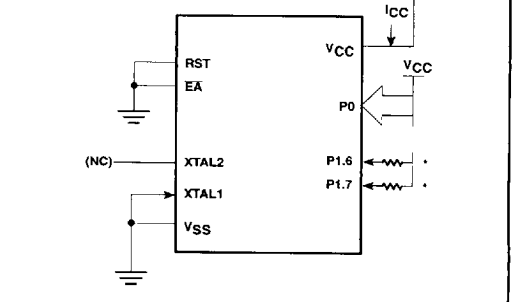


Figure 11. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

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EPROM CHARACTERISTICS

The 87C654/-16 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C654 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C654 manufactured by Philips Components.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 12 and 13. Figure 14 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 12. Note that the 87C654 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 12. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 13.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 14. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = 99H indicates 87C654

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
'0' = Valid low for that pin, '1' = valid high for that pin.
V_{PP} = 12.75V ±0.25V.
V_{CC} = 5V±10% during programming and verification.
* ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

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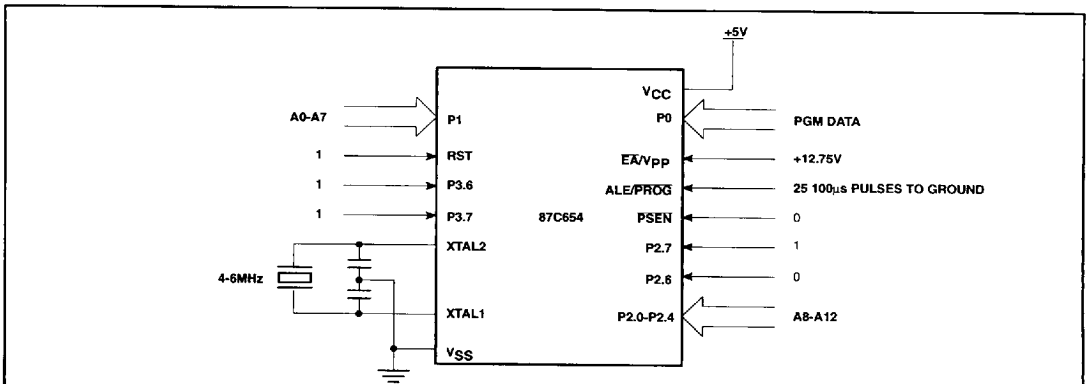

Figure 12. Programming Configuration

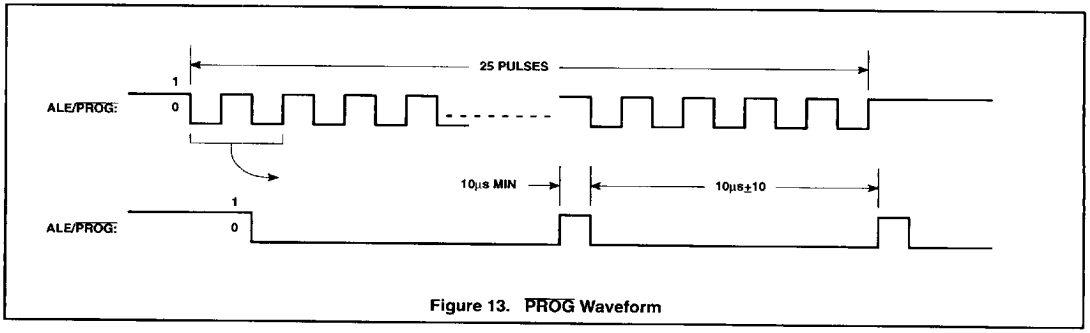

Figure 13. PROG Waveform

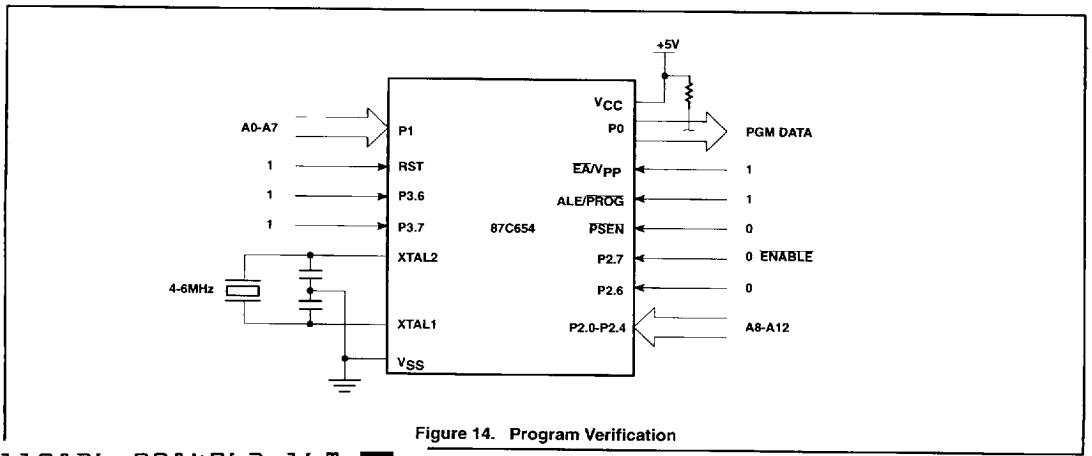

Figure 14. Program Verification

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 15)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 (ENABLE) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

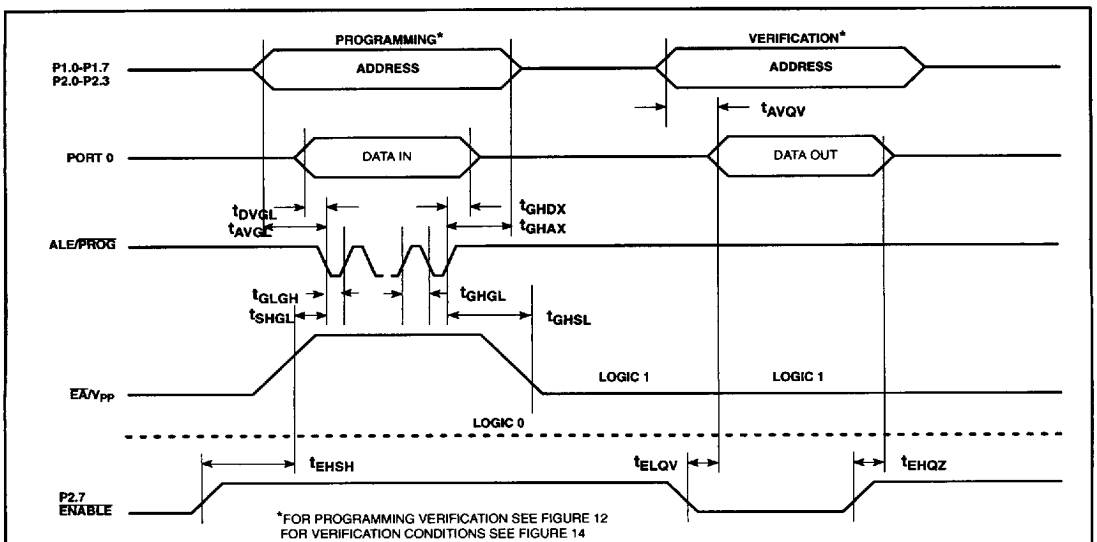

Figure 15. EPROM Programming and Verification

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

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