Military 54ALS163

Synchronous 4-Bit Binary Counter (With Synchronous Clear)

ELECTRICALLY TESTED PER:
MPG54ALS163

The ALS163 is a high-speed 4-bit synchronous counter. It is edge-triggered, synchronously presetable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The ALS163 can count modulo 16 (binary).

The ALS163 has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

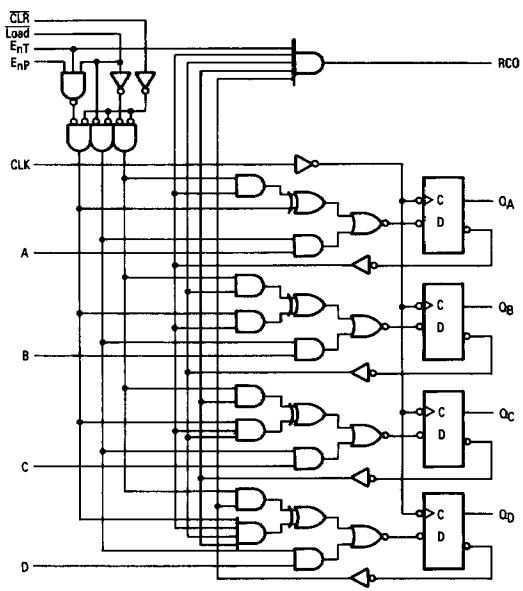
- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Typical Count Rate of 35 MHz

AVAILABLE AS:

1) JAN: N/A
2) SMD: N/A
3) 883C: 54ALS163/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{CLR}$	1	1	2	GND
CLK	2	2	3	V_{CC}
A	3	3	4	V_{CC}
B	4	4	5	V_{CC}
C	5	5	7	V_{CC}
D	6	6	8	V_{CC}
E_{nP}	7	7	9	V_{CC}
GND	8	8	10	GND
$\overline{Load}$	9	9	12	V_{CC}
E_{nT}	10	10	13	V_{CC}
Q_D	11	11	14	OPEN
Q_C	12	12	15	OPEN
Q_B	13	13	17	OPEN
Q_A	14	14	18	OPEN
RCO	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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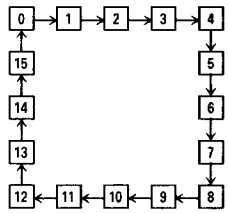
PIN NAMES	
Load	Parallel Enable (Active LOW)
A – D	Parallel Inputs (Data Inputs)
E_{nP}	Count Enable Parallel Input
E_{nT}	Count Enable Trickle Input
CLK	Clock (Active HIGH Going Edge) Input
CLR	Master Reset (Active LOW) Input
$Q_A - Q_D$	Parallel Outputs
RCO	Terminal Count (Ripple Carry) Output

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = $E_{nP} \cdot E_{nT} \cdot$ Load

RCO for ALS163 = $E_{nT} \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$

Preset = $\overline{\text{Load}} \cdot$ CLK + (rising clock edge)

Reset = $\overline{\text{SR}} \cdot$ CLK + (rising clock edge)

FUNCTIONAL DESCRIPTION

The ALS163 is a 4-bit synchronous counter with a synchronous Parallel Enable (Load) feature. The counter consists of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of the clock input (CLK). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

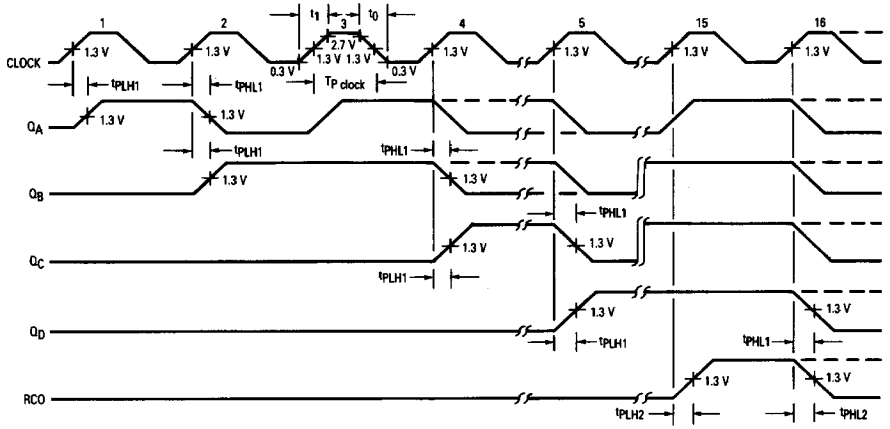
Three control inputs — Parallel Enable ($\overline{\text{Load}}$), Count Enable Parallel (E_{nP}) and Count Enable Trickle (E_{nT}) — select the mode of operation as shown in the table below. The Count Mode is enabled when the E_{nP}, E_{nT}, and $\overline{\text{Load}}$ inputs are HIGH. When the $\overline{\text{Load}}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the E_{nP} or E_{nT} can be used to inhibit the count sequence. With the $\overline{\text{Load}}$ held HIGH, a LOW on either the E_{nP} or E_{nT} inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs ($E_{nP} \cdot E_{nT}$) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (RCO) output is HIGH when the Counter Enable Trickle (E_{nT}) input is HIGH while the counter is in its maximum count state (HLLH for BCD counters, HHHH for Binary counters). Note that RCO is fully decoded and will, therefore, be HIGH only for one count state.

The ALS163 can count modulo 16 following a binary sequence. It can generate a RCO when the E_{nT} input is HIGH while the counter is in the state 15 (HHHH). From this state it can increment to state 0 (LLLL).

The active LOW Synchronous Reset ($\overline{\text{SR}}$) input of the ALS163 acts as an edge-triggered control input, overriding E_{nT}, E_{nP} and $\overline{\text{Load}}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

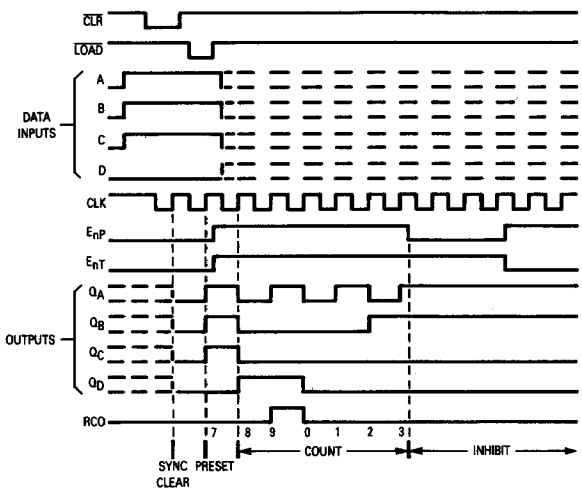
SWITCHING TIME WAVEFORM 1



SYNCHRONOUS TRUTH TABLE

Outputs at time t_n									Outputs at time t_{n+1}				
CLK	E_{nP}	E_{nT}	$\overline{Load}$	A	B	C	D	$\overline{CLR}$	Q_A	Q_B	Q_C	Q_D	Carry Output (RCO)
CP	L	X	H	X	X	X	X	H	NC	NC	NC	NC	NC
CP	X	L	H	X	X	X	X	H	NC	NC	NC	NC	L
CP	H	H	H	X	X	X	X	H	Previous count pulse 1 (Note 1)				H if count = 15 L if count < 15
CP	X	H	L	X	X	X	X	H	A	B	C	D	H if count = 15 L if count < 15
CP	X	L	L	X	X	X	X	H	A	B	C	D	L
CP	X	X	X	X	X	X	X	L	L	L	L	L	L

TYPICAL OPERATIONAL SEQUENCE

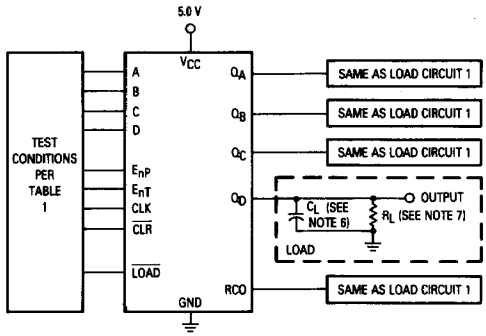


UP COUNT SEQUENCE TABLE

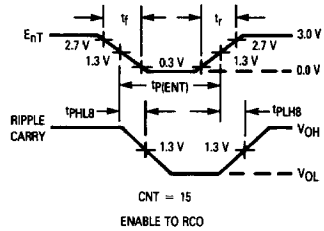
Q_A (LSB)	Q_B	Q_C	Q_D (MSB)
L	L	L	L
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	H

NOTES:
1. See up count sequence table.
2. L = V_{IL} for inputs, V_{OL} for outputs.
3. H = V_{IH} for inputs, V_{OH} for outputs.
4. X = V_{IH} or V_{IL}.
5. CP = Clock pulse.
6. NC = No change.
7. RCO = Carry output.
8. E_{nT} = Enable T.
9. E_{nP} = Enable P.

TEST CIRCUIT

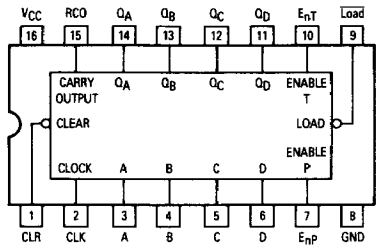


SWITCHING TIME WAVEFORM 2



NOTES:
1. Clock input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{p\,(clock)} = 20$ ns and PRR ≤ 1.0 MHz.
2. Clear input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{p\,(clear)} = 20$ ns.
3. For f_{MAX}, the clock input pulse are as follows:
   $t_r = t_f = 3.0 \pm 1.5$ ns, for 25°C, $t_{p\,(clock)} = 15$ ns, PRR = 30 MHz,
   for −55/125°C, $t_{p\,(clock)} = 20$ ns and PRR = 25 MHz.
4. Enable input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{setup} = 30$ ns, $t_{hold} = 0$ ns and
   $t_{p\,(enable)} = 30$ ns.
5. Inputs not under test are at ground.
6. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
7. $R_L = 499\ \Omega \pm 1.0\%$.

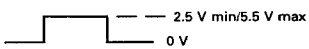
CONNECTION DIAGRAM



Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logic "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −400 μA, $\overline{CLR}$ = 2.0 V, E_{nP} = 2.0 V, CLK = (See Note 1), V_{IH} = 2.0 V, E_{nT} = 2.0 V, $\overline{Load}$ = 0.8 V.
V_{OL}	Logic "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.8 V, $\overline{Load}$ = 0.8 V, CLK = (See Note 1), $\overline{CLR}$ = 2.0 V, E_{nP} = 2.0 V, E_{nT} = 2.0 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		40		40		40	μA	CLK, $\overline{Load}$, E_{nT}: V_{CC} = 5.5 V, V_{IH} = 2.7 V (other inputs are open).
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V (other inputs are open).
I_{IHH}	Logical "1" Input Current		200		200		200	μA	CLK, $\overline{Load}$, E_{nT}: V_{CC} = 5.5 V, V_{IHH} = 7.0 V (other inputs are open).
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V (other inputs are open).
I_O	Output Short Circuit Current	−30	−112	−30	−112	−30	−112	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{Load}$ = GND, V_{OUT} = 2.25 V, CLK = (See Note 1).
I_{IL}	Logical "0" Input Current	0	−200	0	−200	0	−200	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open).
I_{CC}	Power Supply Current Off		25		25		25	mA	V_{CC} = 5.5 V, V_{IN} = GND or 5.5 V (all inputs), $\overline{Load}$ = GND, $\overline{CLR}$ & $E_{nT/P}$ = 5.5 V, CLK = (See Notes 1,3).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

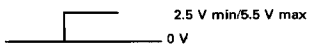
NOTES:

1. Apply one clock pulse prior to test as follows:



2. Method 3011 shall be used, except the output voltage shall be as specified herein, and the output current shall be operating rather than short circuit current. The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit current I_{OS}.

3. Apply one clock pulse prior to test as follows:



Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CLK to Qn	6.0	18	6.0	20	6.0	20	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output CLK to Qn	4.0	15	4.0	18	4.0	18	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output CLK to RCO	7.0	23	7.0	25	7.0	25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CLK to RCO	8.0	26	8.0	30	8.0	30	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL8}	Propagation Delay /Data-Output E_{nT} to RCO	4.0	13	4.0	16	4.0	16	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH8}	Propagation Delay /Data-Output E_{nT} to RCO	5.0	17	5.0	20	5.0	20	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
f_{MAX}	Maximum Clock Frequency	30		25		25		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

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