MOTOROLA

4-Bit Arithmetic Logic Unit/Function Generator

Military 10581

ELECTRICALLY TESTED PER:
MPG 10581

The 10581 is a high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple-through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the 10579, full-carry look-ahead, as a second order look ahead block, the 10581 provides high speed arithmetic operations on very long words.

- 600 mW typ/pkg (No load)
- t_{pd} (typ): A1 to F = 6.5 ns
  C_n to C_{n+4} = 3.1 ns
  A1 to P_G = 5.0 ns
  A1 to G_G = 4.5 ns
  A1 to C_{n+4} = 5.0 ns

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883C: 10581/BXAJC
X = CASE OUTLINE AS FOLLOWS:

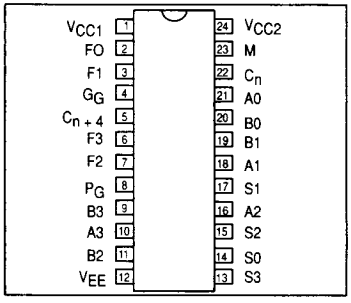
PACKAGE: CERDIP: K
CERFLAT: J
LCC: 3

The letter "M" appears before the slash on LCC.

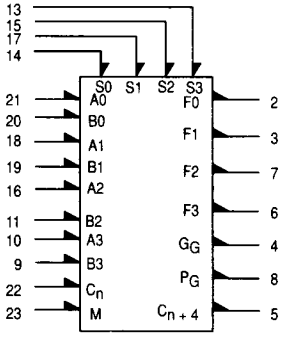
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	7	2	GND
F0	2	8	3	51 Ω to V_{TT}
F1	3	9	4	51 Ω to V_{TT}
G_G	4	10	5	51 Ω to V_{TT}
C_{n+4}	5	11	6	51 Ω to V_{TT}
F3	6	12	7	51 Ω to V_{TT}
F2	7	13	9	51 Ω to V_{TT}
P_G	8	14	10	51 Ω to V_{TT}
B3	9	15	11	50 Ω to V_{EE}
A3	10	16	12	GND
B2	11	17	13	50 Ω to V_{EE}
V_{EE}	12	18	14	V_{EE}
S3	13	19	16	50 Ω to V_{EE}
S0	14	20	17	GND
S2	15	21	18	50 Ω to V_{EE}
A2	16	22	19	GND
S1	17	23	20	GND
A1	18	24	21	50 Ω to V_{EE}
B1	19	1	23	V_{EE}
B0	20	2	24	50 Ω to V_{EE}
A0	21	3	25	GND
C_n	22	4	26	50 Ω to V_{EE}
M	23	5	27	GND
V_{CC2}	24	6	28	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN



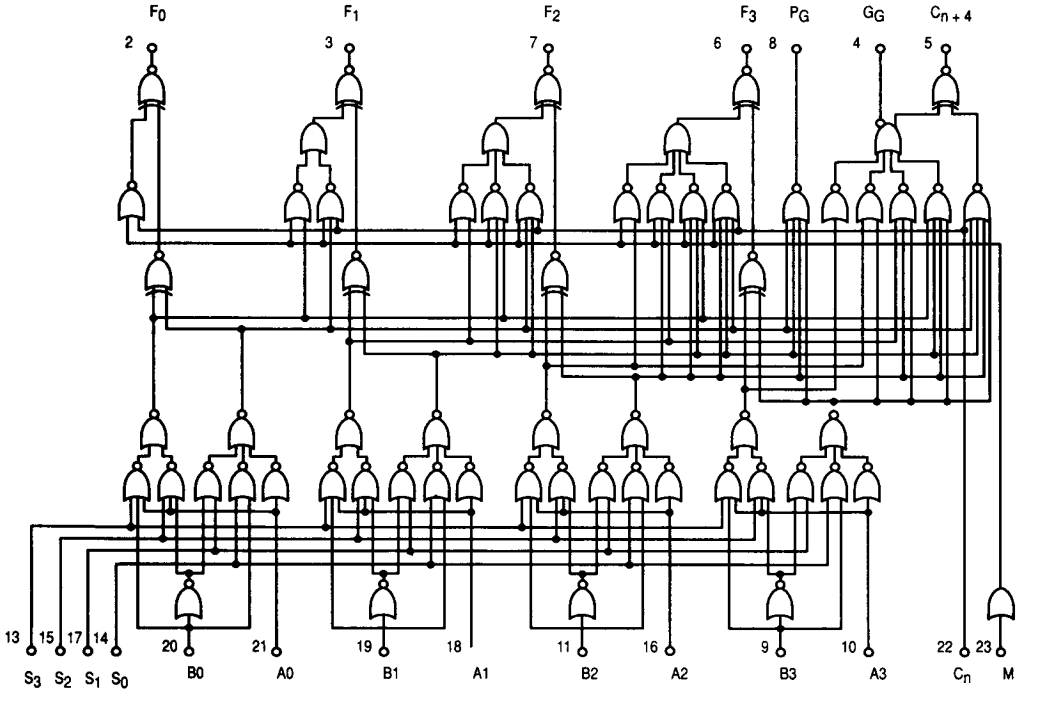
LOGIC DIAGRAM

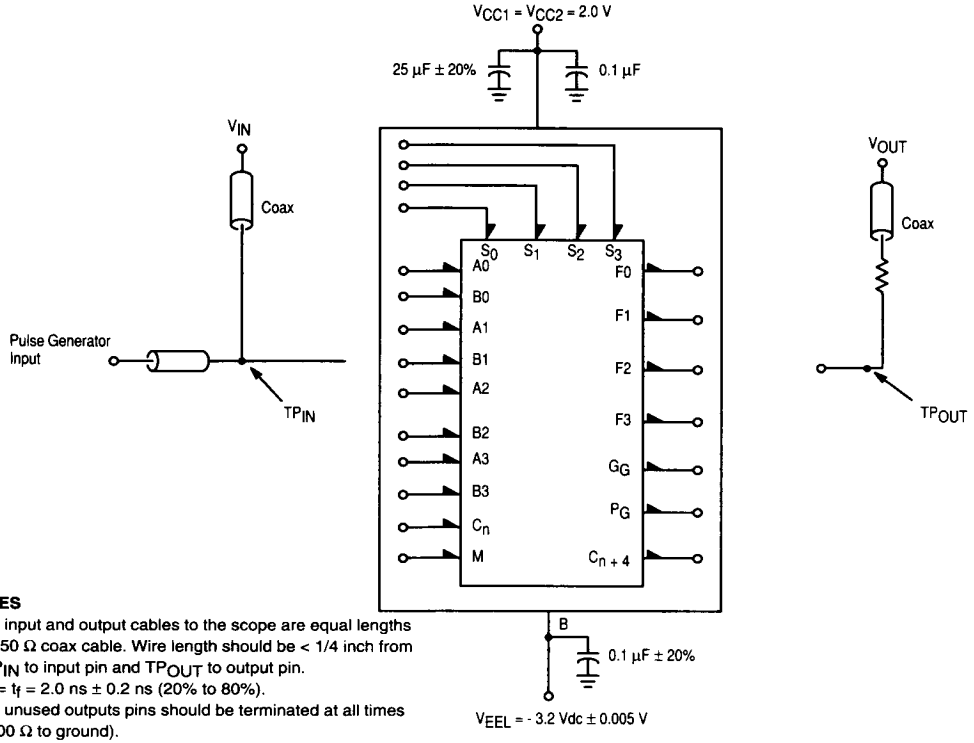


Arithmetic/Logic Functions

Function Select				Logic Function M is High C = D. C.	Arithmetic Operation M is Low C_n is low
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \bullet B$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	$F = A \otimes B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \bullet B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \bullet \overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = minus 1

Logic Diagram





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%).
3. All unused outputs pins should be terminated at all times (100 Ω to ground).
4. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.

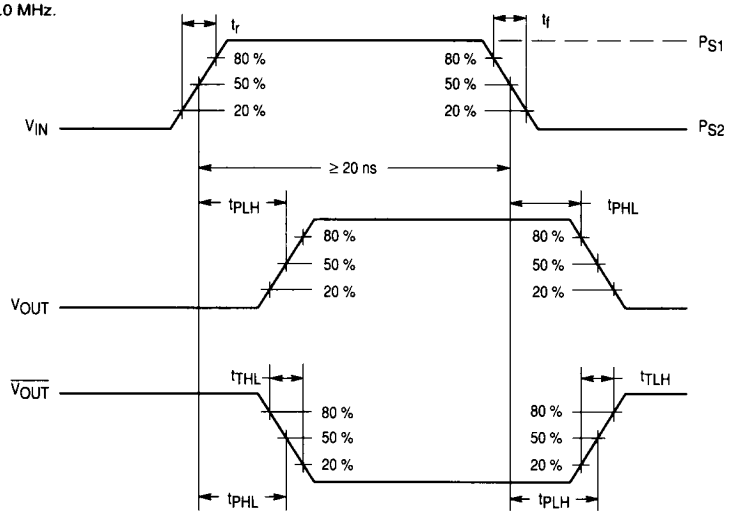


Figure 1. Switching Test Circuit and Waveforms

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.850	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.820	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = -55 °C	-0.88	-1.920	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	9 - 11 16 - 23	13 - 15			12	1, 24	2 - 8
V_{OL1}	Low Output Voltage	– 1.85	– 1.620	– 1.82	– 1.545	– 1.92	– 1.655	V	9 - 11, 14, 16 18, 19, 21 - 23	9, 10, 13, 15 16, 17, 19, 21			12	1, 24	2, 3, 5 - 8
V_{OLA}	Low Output Voltage	– 1.98	– 1.60	– 1.88	– 1.525	– 2.10	– 1.635	V		9 - 11, 13 - 23	14, 15	9 – 11 16 – 23	12	1, 24	2 - 8
V_{OHA}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	9 - 11, 13 16 - 23	13 - 23	16 - 23	13 - 15 22, 23	12	1, 24	2 - 8
V_{OL2}	Low Output Voltage	– 1.99	– 1.620	– 1.88	– 1.545	– 2.10	– 1.655	V	11, 14, 16, 18 20, 22, 23	9, 10, 13, 15 17, 19, 21			12	1, 24	4
I_{IH1}	Input Current High		200		340		340	µA	13, 23				12	1, 24	13, 23
I_{IH2}	Input Current High		220		375		375	µA	10, 16, 18 21				12	1, 24	10, 16, 18 21
I_{IH3}	Input Current High		245		415		415	µA	9, 11 19, 20				12	1, 24	9, 11, 19, 20
I_{IH4}	Input Current High		265		450		450	µA	14, 15, 17				12	1, 24	14, 15, 17
I_{IH5}	Input Current High		290		495		495	µA	22				12	1, 24	22
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		9 - 11 13 - 23			12	1, 24	9 - 11 , 13 - 23
I_{EE}	Power Supply Current	– 145		– 160		– 160		mA	9 - 11, 16 18 - 21				12	1, 24	12

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	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	1.0	3.0	0.8	3.1	0.9	3.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{C_n}$ to $\overline{C_{n+4}}$	1.1	5.0	0.9	5.1	1.0	5.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.3	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{C_n}$ to $\overline{F}$	2.0	7.0	2.0	7.1	1.9	7.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{F}$	3.0	10	2.8	10.2	2.9	10.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	3.5	1.0	3.6	0.9	3.5	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{P_G}$	2.0	6.5	1.8	6.5	1.8	6.6	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{G_G}$	2.0	7.0	2.0	7.1	1.9	7.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.0	3.0	0.9	3.1	0.9	3.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{C_{n+4}}$	2.0	7.0	1.9	7.5	2.0	7.1	ns	"	"	"	"	"	"

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		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{F}$	3.0	11	2.7	11.2	2.9	11.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	3.5	0.9	3.5	1.0	3.5	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{P_G}$	2.0	7.5	1.6	7.6	1.8	7.6	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.0	1.0	5.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{G_G}$	2.0	8.0	2.0	8.1	1.9	8.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.0	3.0	0.9	3.0	0.9	3.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{C_{n+4}}$	2.0	8.0	1.9	8.5	1.9	8.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{M}$ to $\overline{F}$	3.0	10	2.8	10.2	2.3	10.3	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{F}$	3.0	10	2.6	10.2	2.7	10.2	ns	"	"	"	"	"	"

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		Subgroup 9		Subgroup 10		Subgroup 11								
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t_{pd}	Propagation Delay $\overline{S}$ to $\overline{P_G}$	2.0	8.0	1.8	8.1	1.9	8.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.1	1.0	5.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{C_{n+4}}$	2.0	9.0	1.8	9.1	1.9	9.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.8	6.0	0.8	6.2	0.8	6.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{G_G}$	2.0	9.0	1.7	9.1	1.7	9.2	ns	"	"	"	"	"	"