MAX707, MAX708

μP Supervisory Circuits

The MAX707/708 are cost–effective system supervisor circuits designed to monitor Vcc in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 20 μsec of Vcc falling through the reset voltage threshold. Reset is maintained with 200 mS of delay time after Vcc rise above the reset threshold. The MAX707/708 have a low quiescent current of 12 μA at Vcc = 3.3 V, an active–high RESET and active–low $\overline{\text{RESET}}$ with a push–pull output. The output is guaranteed valid down to Vcc = 1.0 V. The MAX707/708 have a Manual Reset $\overline{\text{MR}}$ input and a +1.25 V threshold detector for power–fail input PFI. These devices are available in a Micro8 and SOIC–8 package.

Features

- Precision Supply–Voltage Monitor
  MAX707: 4.63 V Reset Threshold Voltage
  MAX708: Standard Reset Threshold Voltages (Typical):
  4.38 V, 3.08 V, 2.93 V, 2.63 V
- Reset Threshold Available from 1.6 V to 4.9 V with 100 mV Increments (Factory Option)
- 200 mS (Typ) Reset Timeout Delay
- 12 μA (Vcc = 3.3 V) Quiescent Current
- Active_High and Active_Low Reset Output
- Guaranteed RESET_L and RESET Output Valid to Vcc = 1.0 V
- Voltage Monitor for Power–Fail or Low–Battery Warning
- 8 Pin SO or Micro8 Package

Applications

- Computers
- Embedded System
- Battery Powered Equipment
- Critical μP Power Supply Monitor

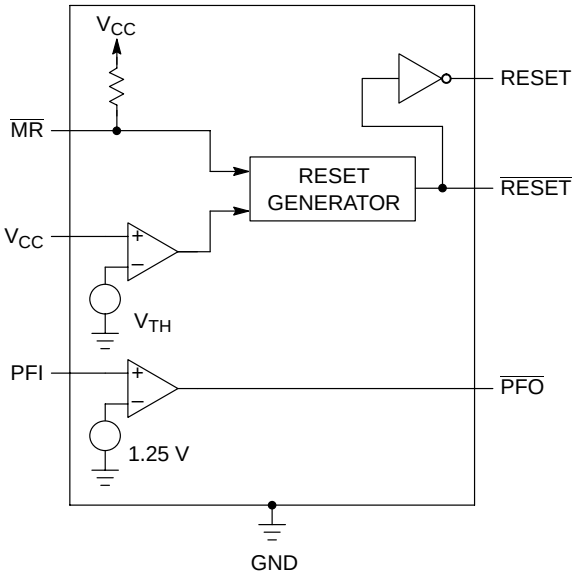
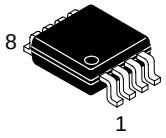


Figure 1. Representative Block Diagram

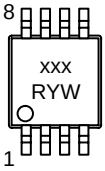
ON Semiconductor™

http://onsemi.com

MARKING DIAGRAMS

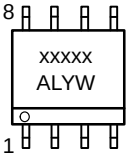


Micro8™
CUA SUFFIX
CASE 846A



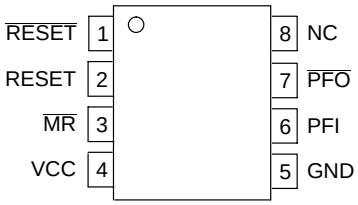
xxx = Specific Device Code (see page 9)
R = Factory Code
YW = Date Code

SO–8
ESA SUFFIX
CASE 751



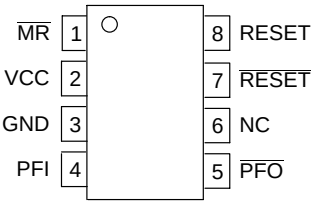
xxxxx = Specific Date Code (see page 9)
AL = Assembly Lot Code
YW = Date Code

PIN CONFIGURATION



(Top View)

Micro8



(Top View)

SO–8

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Output Voltage	V_{out}	–0.3 to (V_{CC} + 0.3)	V
Output Current (All Outputs)	I_{out}	20	mA
Input Current (V_{CC} and GND)	I_{in}	20	mA
Thermal Resistance Junction to Air Micro8 SO–8	$R_{\theta JA}$	 248 187	°C/W
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Latch–Up Performance Positive Negative	$I_{LATCH–UP}$	 300 280	mA

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL–STD–883, Method 3015.
   Machine Model Method 200 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

ELECTRICAL CHARACTERISTICS (V_{CC} = 1.0 V to 5.5 V, T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{CC} = 3.3 V.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}	1.0	–	5.5	V
Supply Current V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	 – –	 12 16	 22 28	μA
Reset Threshold MAX707 T_A = +25°C T_A = –40°C to +85°C MAX708 T_A = +25°C T_A = –40°C to +85°C MAX708T T_A = +25°C T_A = –40°C to +85°C MAX708S T_A = +25°C T_A = –40°C to +85°C MAX708R T_A = +25°C T_A = –40°C to +85°C	V_{TH}	 4.56 4.50 4.31 4.25 3.03 3.00 2.89 2.85 2.59 2.55	 4.63 4.38 3.08 2.93 2.63 	 4.70 4.75 4.45 4.50 3.13 3.15 2.97 3.00 2.67 2.70	V
Reset Threshold Hysteresis	V_{HYS}	–	0.01 V_{TH}	–	mV
V_{CC} Falling Reset Delay (V_{CC} = V_{TH} + 0.2 V to V_{TH} –0.2 V)	t_{PD}	–	20	–	μS
Reset Active Timeout Period	t_{RP}	140	200	330	mS
RESET_L, RESET_H Output Low Voltage $V_{CC} \geq$ 1.0 V, I_{ol} = 100 μA V_{CC} > 2.7 V, I_{ol} = 1.2 mA V_{CC} > 4.5 V, I_{ol} = 3.2 mA	V_{ol}	 – – –	 – – –	 0.3 0.3 0.3	V
RESET_L, RESET_H Output High Voltage $V_{CC} \geq$ 1.0 V, I_{oh} = 50 μA V_{CC} > 2.7 V, I_{oh} = 500 μA V_{CC} > 4.5 V, I_{oh} = 800 μA	V_{oh}	 0.8 V_{CC} 0.8 V_{CC} 0.8 V_{CC}	 – – –	 – – –	V
MR_L Pull–up Resistance	R_{MRI}	50	–	–	KΩ
MR_L Pulse Width (V_{TH} (max) < V_{CC} < 5.5 V)	t_{MR}	1.0	–	–	μS
MR_L Glitch Rejection (V_{TH} (max) < V_{CC} < 5.5 V)	–	–	0.1	–	μS
MR_L High_level Input Threshold (V_{TH} (max) < V_{CC} < 5.5 V)	V_{IH}	0.7 V_{CC}	–	–	V
MR_L Low_level Input Threshold (V_{TH} (max) < V_{CC} < 5.5 V)	V_{IL}	–	–	0.3 V_{CC}	V
MR_L to RESET_L and RESET_H Output Delay (V_{TH} (max) < V_{CC} < 5.5 V)	t_{MD}	–	0.2	–	μS
PFI Input Threshold (V_{CC} = 3.3 V, PFI Falling)	–	1.20	1.25	1.3	V
PFI Input Current	–	–250	0.01	250	nA
PFI to PFO Delay (V_{CC} = 3.3 V, $V_{OVERDRIVE}$ = 15 mV)	–	–	3.0	–	μS
PFO_L Output Low Voltage V_{CC} = 2.7 V, I_{ol} = 1.2 mA V_{CC} = 4.5 V, I_{ol} = 3.2 mA	V_{ol}	 – –	 – –	 0.3 0.3	V
PFO_L Output High Voltage V_{CC} = 2.7 V, I_{oh} = 500 μA V_{CC} = 4.5 V, I_{oh} = 800 μA	V_{oh}	 0.8 V_{CC} 0.8 V_{CC}	 – –	 – –	V

PIN DESCRIPTION (Pin No. with parentheses is for Micro8 package.)

Pin No.	Symbol	Description
1 (3)	$\overline{MR}$	Manual Reset Input. $\overline{MR}$ can be driven from TTL/CMOS logic or from a manual Reset switch. This input, when floating, is internally pulled up to V_{CC} with 50 KΩ resistor.
2 (4)	V_{CC}	Supply Voltage: C = 100nF is recommended as a bypass capacitor between V_{CC} and GND.
3 (5)	GND	Ground Reference
4 (6)	PFI	Power Fail Voltage Monitor Input. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5 (7)	$\overline{PFO}$	Power Fail Monitor Output. When PFI is less than 1.25 V, it goes low and sinks current. Otherwise, it remains high.
6 (8)	NC	Non–connective Pin
7 (1)	$\overline{RESET}$	Active Low $\overline{RESET}$ can be triggered by V_{CC} below the threshold level or by a low signal on $\overline{MR}$. It remains low for 200 ms (typ.) after V_{CC} rises above the reset threshold.
8 (2)	RESET	Active high RESET output the inverse of $\overline{RESET}$ one.

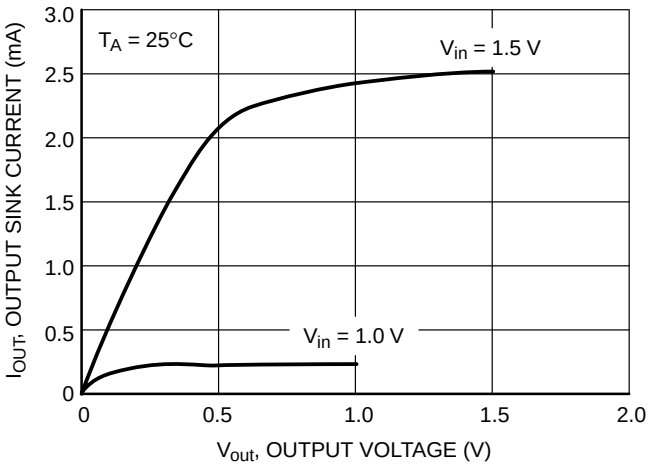


Figure 2. MAX707/708 Series 1.60 V Reset Output Sink Current vs. Output Voltage

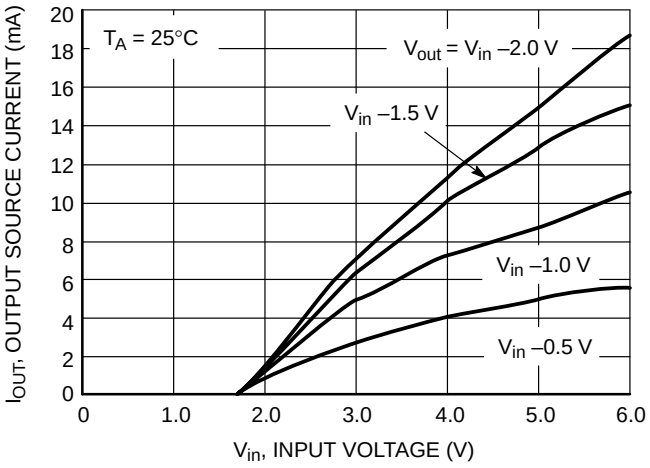


Figure 3. MAX707/708 Series 1.60 V Reset Output Source Current vs. Input Voltage

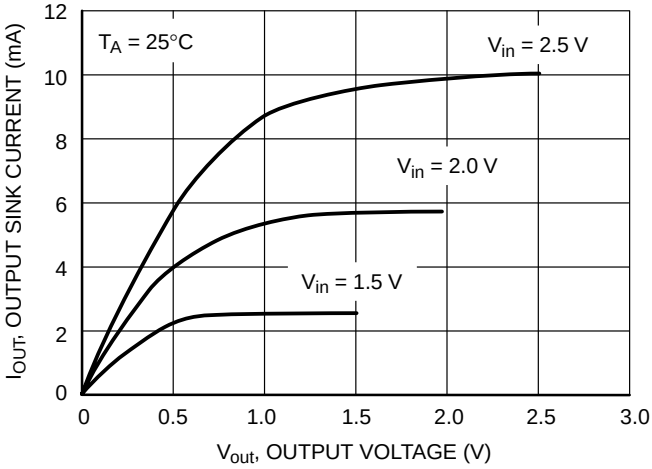


Figure 4. MAX707/708 Series 2.93 V Reset Output Sink Current vs. Output Voltage

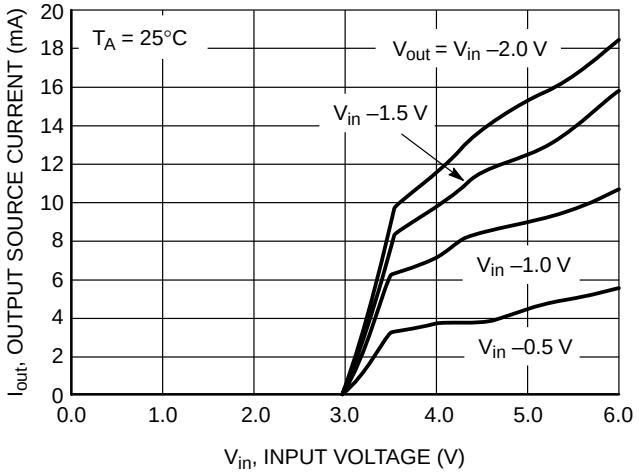


Figure 5. MAX707/708 Series 2.93 V Reset Output Source Current vs. Input Voltage

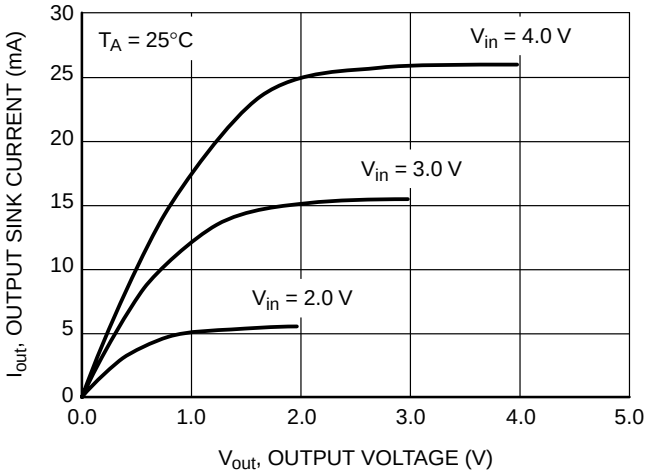


Figure 6. MAX707/708 Series 4.90 V Reset Output Sink Current vs. Output Voltage

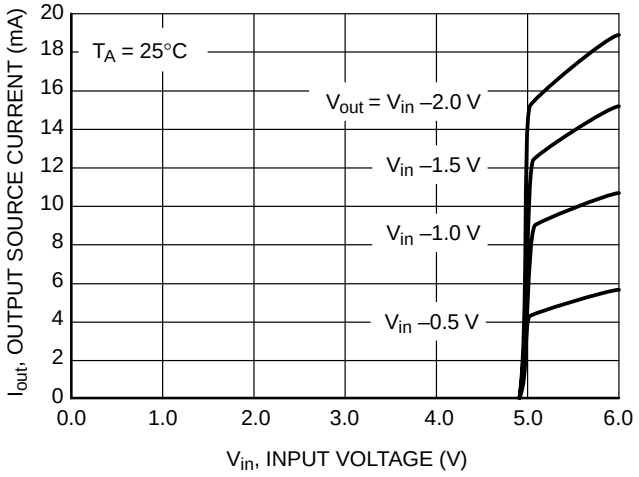


Figure 7. MAX707/708 Series 4.90 V Reset Output Source Current vs. Input Voltage

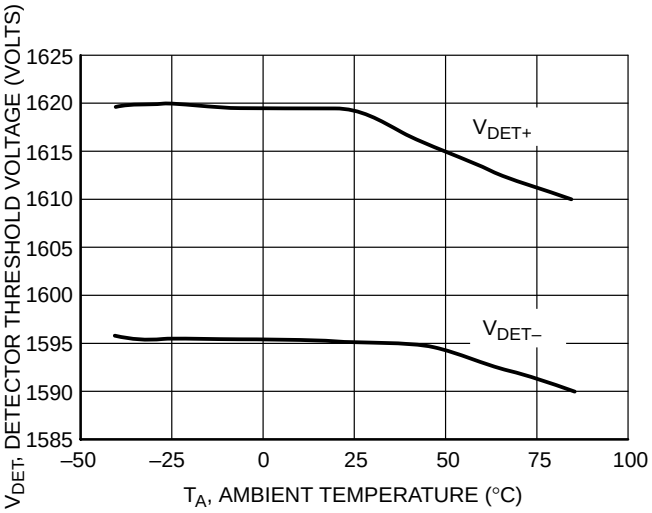


Figure 8. MAX707/708 Series 1.60 V Detector Threshold Voltage vs. Temperature

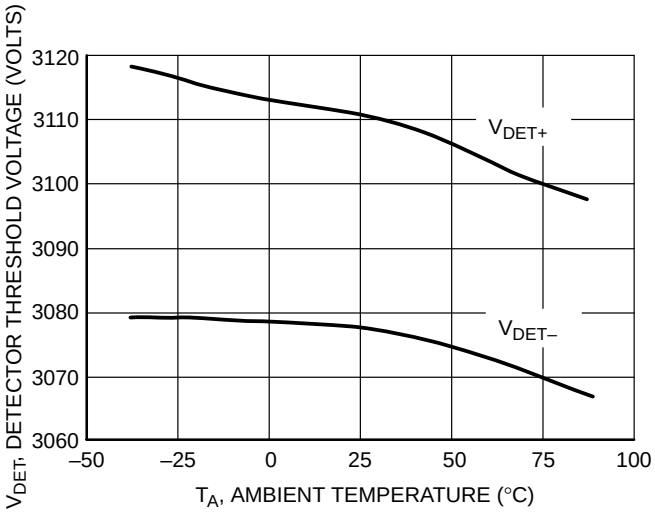


Figure 9. MAX707/708 Series 2.93 V Detector Threshold Voltage vs. Temperature

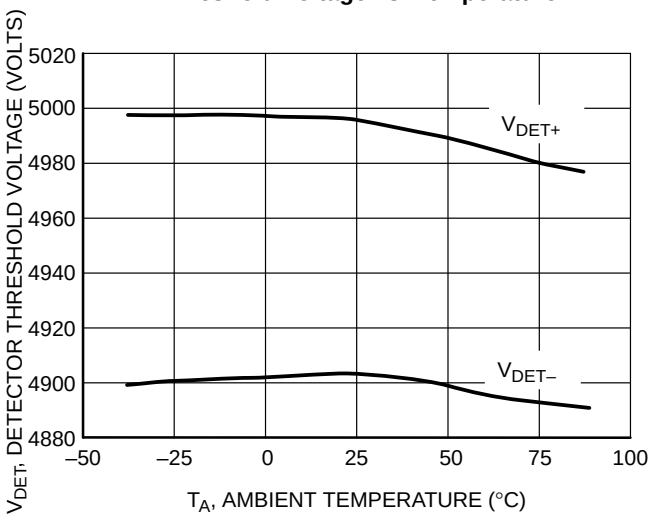


Figure 10. MAX707/708 Series 4.90 V Detector Threshold Voltage vs. Temperature

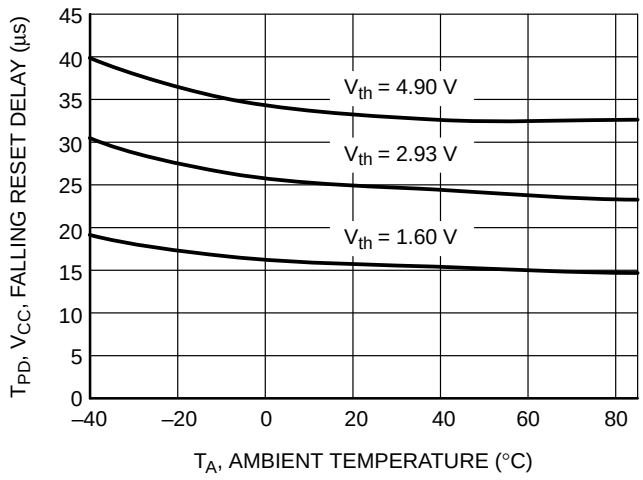


Figure 11. MAX707/708 Series V_{CC} Falling Reset Delay vs. Temperature

APPLICATIONS INFORMATION

Microprocessor Reset

To generate a processor reset, the manual Reset input allows different reset sources. A pushbutton switch can be one of these. It is effectively debounced by the 1.0 μs minimum reset pulse width. As $\overline{MR}$ is TTL/CMOS logic compatible, it can be driven by an external logic line.

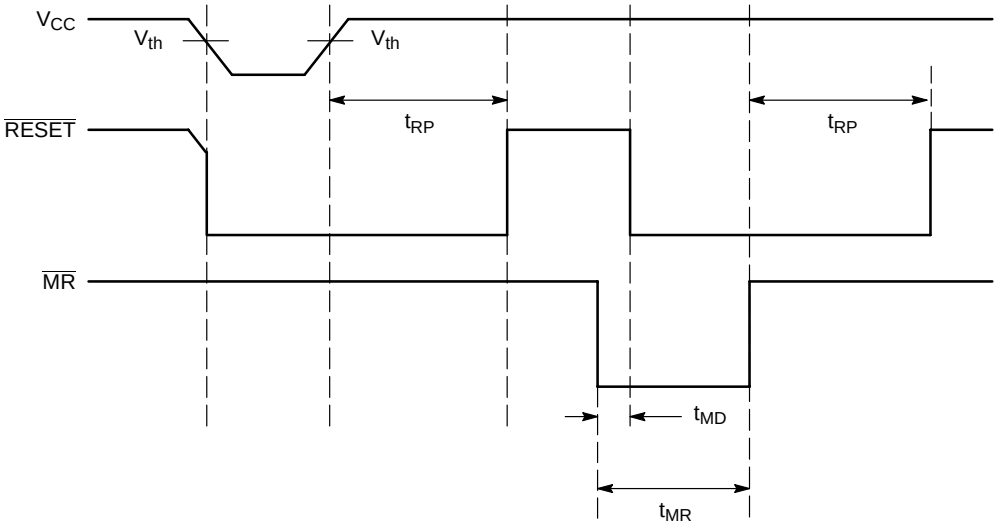


Figure 12. $\overline{RESET}$ and $\overline{MR}$ Timing

V_{CC} Transient Rejection

The MAX707/708 provides accurate V_{CC} monitoring and reset timing during power–up, power–down, and brownout/sag conditions, and rejects negative glitches on the power supply line. Figure 13 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. For a given overdrive, the point of the curve is the maximum width of the glitch allowed before the device generates a reset signal. Transient immunity can be improved by adding a capacitor (100 nF for example) in close proximity to the V_{CC} pin of the MAX707/708.

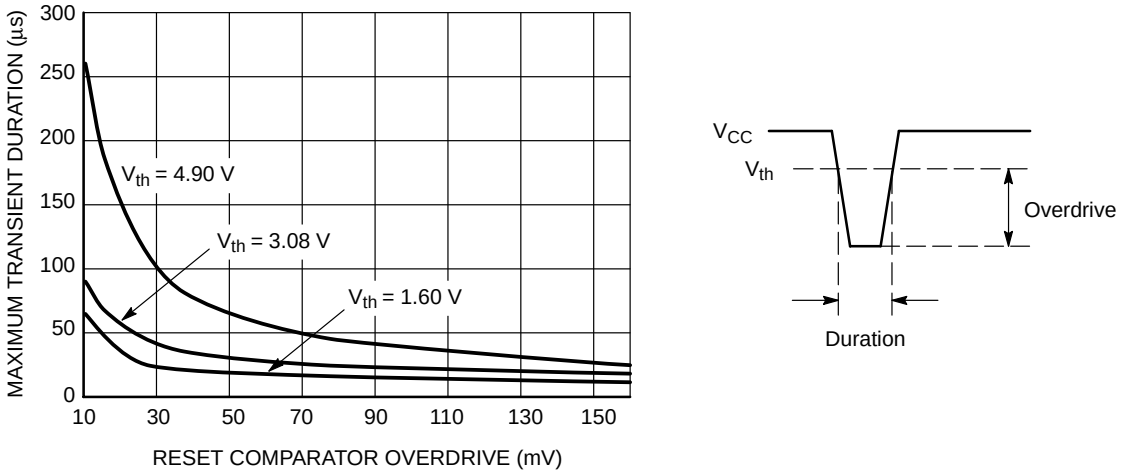


Figure 13. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

$\overline{\text{RESET}}$ Signal Integrity During Power–Down

The MAX707/708 $\overline{\text{RESET}}$ output is valid until V_{CC} falls below 1.0 V. Then, the output becomes an open circuit and no longer sinks current. This means CMOS logic inputs of the μP will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in the case $\overline{\text{RESET}}$ must be maintained valid to V_{CC} = 0 V, a pull down resistor must be connected from $\overline{\text{RESET}}$ to ground to discharge stray capacitances and hold the output low (Figure 14). This resistor value, though not critical, should be chosen large enough not to load $\overline{\text{RESET}}$ and small enough to pull it to ground. R = 100 kΩ will be suitable for most applications.

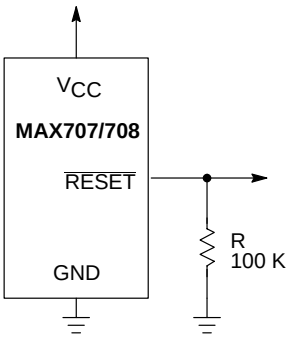


Figure 14. Ensuring $\overline{\text{RESET}}$ Valid to V_{CC} = 0 V

Interfacing with μPs with Bidirectional I/O Pins

Some μPs (such as Motorola 68HC11) have bidirectional reset pins. If, for example, the $\overline{\text{RESET}}$ output is driven high and the μP wants to put it low, indeterminate logic level may result. This can be avoided by adding a 4.7 kΩ resistor in series with the output of the MAX707/708 (Figure 15). If there are other components in the system that require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the μP, the buffer should be connected as shown with the solid line.

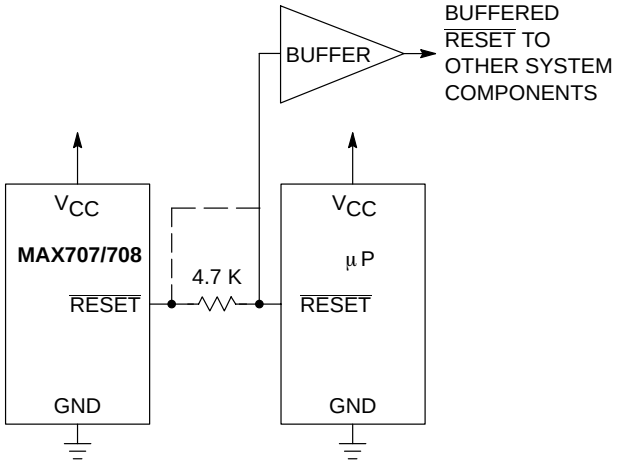
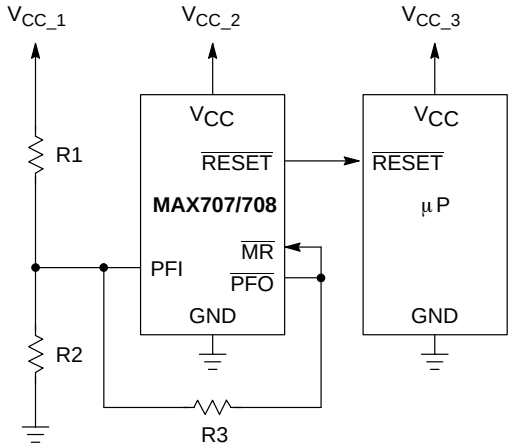
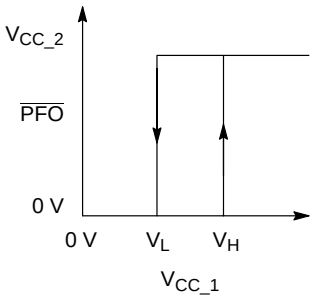


Figure 15. Interfacing to Bidirectional Reset I/O

Monitoring Additional Supply Levels

When connecting a voltage divider to PFI and adjusting it properly, you can monitor a voltage different than the unregulated DC one. As shown in Figure 16, to increase noise immunity, hysteresis may be added to the power–fail comparator just by a resistor between $\overline{\text{PFO}}$ and PFI. Not to unbalance the potential divider network, R3 should be 10 times the sum of the two resistors R1 and R2. If required, a capacitor between PFI and GND will reduce the sensitivity of the circuit to high–frequency noise on the line being monitored. The $\overline{\text{PFO}}$ output may be connected to $\overline{\text{MR}}$ input to generate a low level on the $\overline{\text{RESET}}$ when Vcc_1 drops out of tolerance. Thus a $\overline{\text{RESET}}$ is generated when one of the two voltages is below its threshold level.





$$VL = 1.25 + R1 \times \left(\frac{1.25}{R2} + \frac{1.25 - Vcc\_2}{R3}\right)$$

$$VH = 1.25 \times \left(1 + R1 \times \left(\frac{R2 + R3}{R2 \times R3}\right)\right)$$

$$VHYS = VH - VL = \frac{R1 \times Vcc\_2}{R3}$$

Figure 16. Monitoring Additional Supply Levels

ORDERING INFORMATION

Device	Package	Marking	Shipping
MAX707ESA–T	SO–8	S707	2500 Tape & Reel
MAX708ESA–T	SO–8	S708	2500 Tape & Reel
MAX708xESA–T (Note 3)	SO–8	S708x	2500 Tape & Reel
MAX707CUA–T	Micro8	SAC	4000 Tape & Reel
MAX708CUA–T	Micro8	SAD	4000 Tape & Reel
MAX708xCUA–T (Note 3)	Micro8	SAy (Note 4)	4000 Tape & Reel

3. The “x” denotes a suffix for V_{CC} threshold – see Table 1.
4. The “y” denotes a suffix for V_{CC} threshold – see Table 2.

Table 1. Suffix “x”

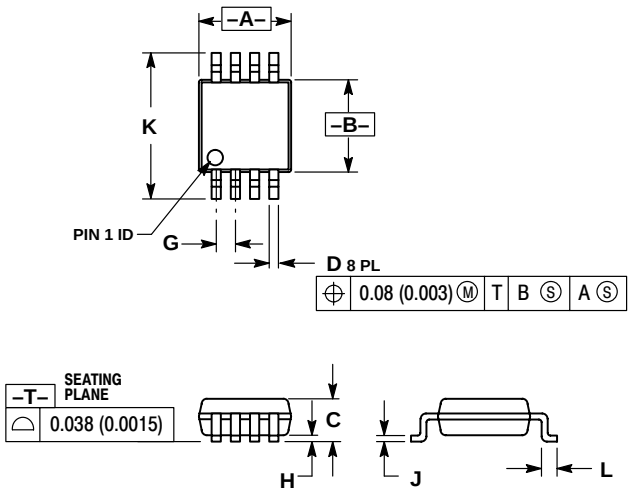
Suffix	Reset Vcc Threshold (V)
T	3.08
S	2.93
R	2.63

Table 2. Suffix “y”

Suffix	Reset Vcc Threshold (V)
E	3.08
F	2.93
G	2.63

PACKAGE DIMENSIONS

Micro8
CASE 846A–02
ISSUE E

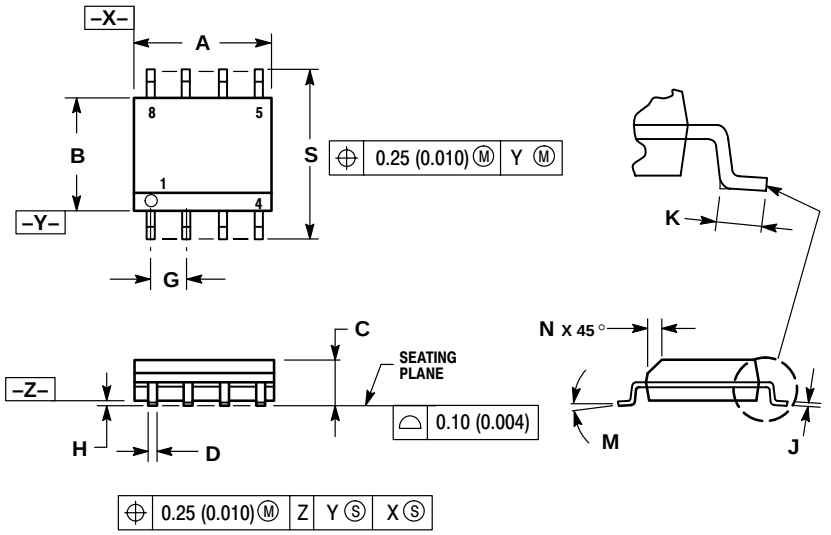


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

PACKAGE DIMENSIONS

SO–8
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Micro8 is a trademark of International Rectifier.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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