HMC703LP4E

8 GHz FRACTIONAL SYNTHESIZER

Typical Applications

The HMC703LP4E is ideal for:

- Microwave Point-to-Point Radios
- Base Stations for Mobile Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs, WiMAX
- Communications Test Equipment
- CATV Equipment
- Automotive Sensors
- AESA - Phased Arrays
- FMCW Radar Systems

Features

Wide band: DC - 8 GHz RF Input

Best Phase Noise and Spurious in the Industry:
-112 dBc/Hz @ 8 GHz Fractional, 50 kHz Offset

Figure of Merit

-230 dBc/Hz Fractional Mode

-233 dBc/Hz Integer Mode

High PFD rate: 100 MHz

< 50 fs RMS jitter

Frequency and Phase Modulation

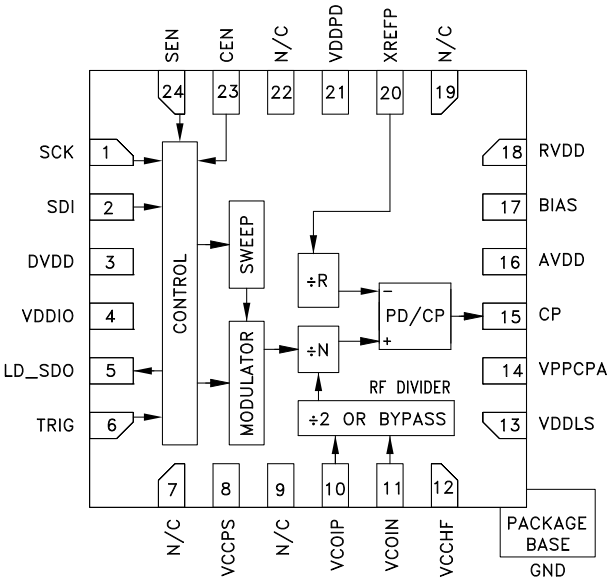
Integrated Frequency Sweeper

Triggered Frequency Hopping

External Triggering

24 Lead 4x4 mm SMT Package: 16 mm^2

Functional Diagram



General Description

The HMC703LP4E fractional synthesizer is built upon the high performance PLL platform also contained in the HMC704LP4E and Hittite's latest generation of PLL+VCO products. This platform has the best phase-noise and spurious performance in the industry - enabling higher order modulation schemes while minimizing blocker effects in high performance radios.

In addition, the HMC703LP4E offers frequency sweep and modulation features, external triggering, double-buffering, exact frequency control, phase modulation and more - while maintaining pin compatibility with the HMC700LP4E PLL.

Exact frequency mode with a 24-bit fractional modulator provides the ability to generate fractional frequencies with zero frequency error and very low channel spurious, an important feature for Digital Pre-Distortion systems.

The serial interface offers read back capability and is compatible with a wide variety of protocols.

For price, delivery and to place orders: Hittite Microwave Corporation, 2 Elizabeth Drive, Chelmsford, MA 01824
978-250-3343 • 978-250-3373 fax • Order On-line at www.hittite.com
Application Support: Phone: pll@hittite.com

Table 1. Electrical Specifications

Unless otherwise specified, data is collected at 3.3 V, and 5.0 V (on charge-pump), 100 MHz reference, 50 MHz f_{PD}. Min and Max are specified across temperature range from -40 °C to 85 °C ambient.

Parameter	Conditions	Min.	Typ.	Max.	Units
RF INPUT CHARACTERISTICS	[6][7]				
RF Input Frequency Range	[1]	DC		8000	MHz
Prescaler Input Freq Range	[1]	DC		4000	MHz
Power Range	[13]	-15	-10	-3	dBm
Return Loss	[15]	-18	-12	-7	dB
REF INPUT CHARACTERISTICS					
Frequency Range (3.3V)	[1][8]	DC	50	350	MHz
Power from 50 Ω Source	[12] with 100 Ω termination off chip		6		dBm
Return Loss	[15]	-16		-8	dB
Ref Divider Range (14 bit)		1		16,383	
PHASE DETECTOR RATE	[1]				
Integer Mode		DC	50	115	MHz
Fractional Mode B		DC	50	100	MHz
Fractional Mode A		DC	50	80	MHz
CHARGE PUMP					
CP Output Current	20 µA Steps, Charge Pump Gain = CP Current/2π Amps/rad	0.02		2.5	mA
CP HiK	see "Charge Pump Gain" section		3.5	6	mA
POWER SUPPLIES					
RVDD, AVDD, VCCPS, VCCHF, VCCPD, DVDD, VDDIO		2.7	3.3	3.5	V
VDDLS, VPPCP Charge Pump	VDDLS, VPPCP must be equal	2.7	5.0	5.2	V
3.3V - Current consumption	[9] 100 kHz PD 50 MHz PD 100 MHz PD		 34 54 74	 45 70 95	 mA mA mA
5V - Current consumption	All Modes 100 kHz PD 50 MHz PD w/ CP HiK 100 MHz PD w/ CP HiK		 3 7 13	 5 12 16	 mA mA mA
Power Down Current	[10]			100	uA
BIAS Reference Voltage	Pin 12. Measured with 10 GΩ Meter	1.880	1.920	1.960	V

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Table 34. Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
PHASE NOISE [14]					
Flicker Figure of Merit (FOM)[2]			-270		dBc/Hz
Floor Figure of Merit [11]	Integer HiK Mode Integer Normal Mode Fractional HiK Mode [3] Fractional Normal Mode [3]	-236 -232 -232 -228	-233 -230 -230 -227	-231 -228 -227 -225	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Flicker Noise at f_{offset}	PN_{flick} = Flicker FOM +20log(f_{vco}) -10log(f_{offset})				dBc/Hz
Phase Noise Floor at f_{vco} with f_{pd}	PN_{floor} = Floor FOM + 10log(f_{pd}) +20log(f_{vco}/f_{pd})				dBc/Hz
VCO referred Phase Noise Contribution of the PLL vs f_{offset}, f_{vco}, f_{pd}	$PN = 10\log(10^{(PNflick/10)} + 10^{(PNfloor/10)})$				dBc/Hz
Jitter	SSB 100Hz to 100MHz with HMC508LP5E VCO		50		fs
SPURIOUS	[4][5]				
Integer Boundary Spurs @~8GHz	offsets less than loop band-width, f_{pd} = 50MHz		-60	-52	dBc
LOGIC INPUTS					
Switching Theshold (Vsw)	VIH/VIL within 50 mV of Vsw	38	47	54	% VDDIO
LOGIC OUTPUT					
VOH Output High Voltage			VDDIO		V
VOL Output Low Voltage			0		V
Output impedance : Pull Up	VDDIO=3.3 V	115	150	180	Ohm
Output impedance : Pull Dn	VDDIO=3.3 V	130	135	210	Ohm
DC load				1.5	mA
Digital Output Driver Delay SCK to Digital Output Delay	1.7nsec with a 3 pF load		0.5ns+0.2ns/pF 8.2ns+0.2ns/pF		ns ns
RF Divider Range					
>4GHz Integer Mode	16 bit , Even values only	32		131,070	
< 4GHz Integer Mode	16 bit , All values	16		65,535	
> 4GHz Fractional Mode	16 bit	40.0		131,065.0	
< 4GHz Fractional Mode	16 bit	20.0		65,531.0	

[1] Frequency is guaranteed across process, voltage and temperature from -40°C to 85°C.
[2] With high charge-pump current, +12dBm 100MHz sine reference
[3] Fractional FOM degrades about 3dB/octave for prescaler input frequencies below 2GHz
[4] Using 50MHz reference with VCO tuned to within one loop bandwidth of an integer multiple of the PD frequency. Larger offsets produce better results. See the "Spurious Performance" section for more information.
[5] Measured with the HMC703LP4E evaluation board. Board design and isolation will affect performance.
[6] Internal divide-by-2 should be enabled for frequencies >4GHz
[7] At low RF Frequency, Rise and fall times should be less than 1ns to maintain performance
[8] Slew rate of greater or equal to 0.5 V/ns
[9] Current consumption depends upon operating mode and frequency of the VCO. Typical values are for fractional mode.
[10] Reference input disconnected
[11] Min/Max versus temperature and supply, under typical reference & RF frequencies and power levels
[12] Slew > 0.5V/ns is recommended , see Table 7, Figure 5, Figure 6 for more information.
[13] Operable with reduced spectral performance outside of this range.
[14] This section specifies the Phase Noise contribution of the PLL, solution phase noise with a given VCO, loop filter and reference requires a closed loop calculation using Hittite PLL Design Tool.
[15] As measured on HMC703LP4E Evaluation board, with 100Ohm external termination.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, plots are measured with a 50 MHz PD rate, VCO near 8 GHz, RF power ≈ -10 dBm, and a Wenzel 100 MHz sinusoid reference. The operating modes in the following plots refer to Integer (int), Fractional Modes A and B, HiKcp (HiK).

Figure 1. Floor FOM vs. Mode and Temp, 2.5 mA CP Current

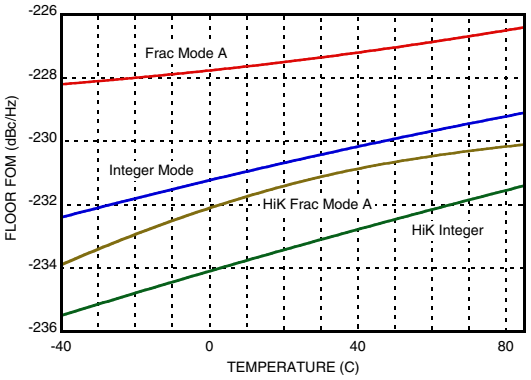


Figure 2. Flicker FOM vs. Mode and Temp, 2.5 mA CP Current

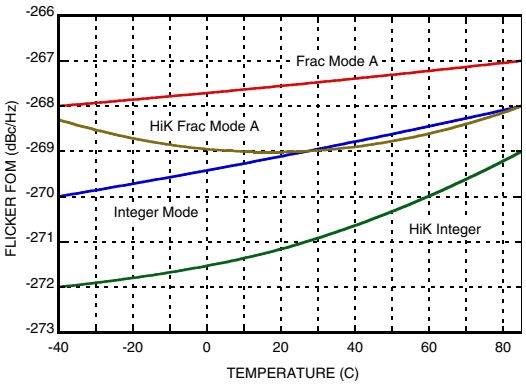


Figure 3. Floor FOM vs. Output Frequency and Mode, 2.5 mA CP Current

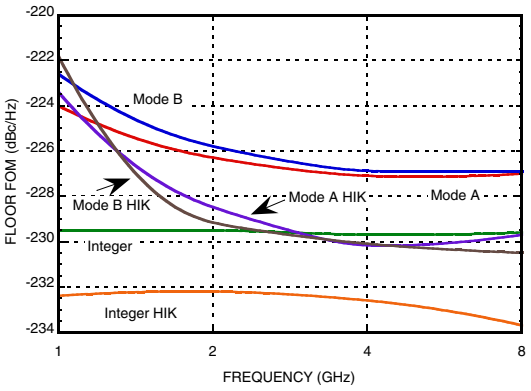


Figure 4. Flicker FOM vs. Output Frequency and Mode, 2.5 mA CP Current

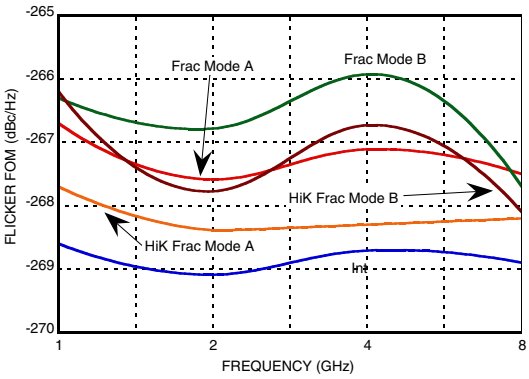


Figure 5. Floor FOM vs. Reference Power and Mode, 2.5 mA CP Current [1]

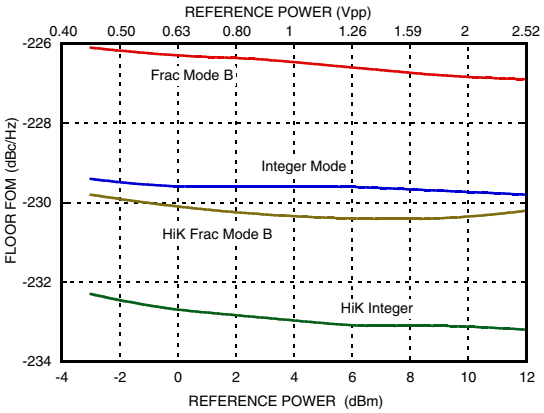
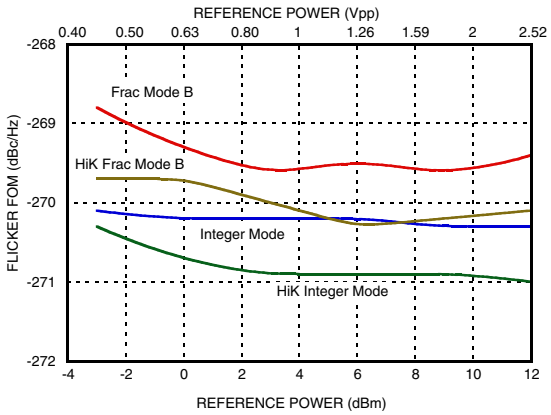


Figure 6. Flicker FOM vs. Reference Power and Mode, 2.5 mA CP Current [1]



[1] 100 MHz Sinusoidal Wenzel reference.

Figure 7. Flicker FOM vs. CP Current, Fractional Mode B, 2.5 mA CP Current

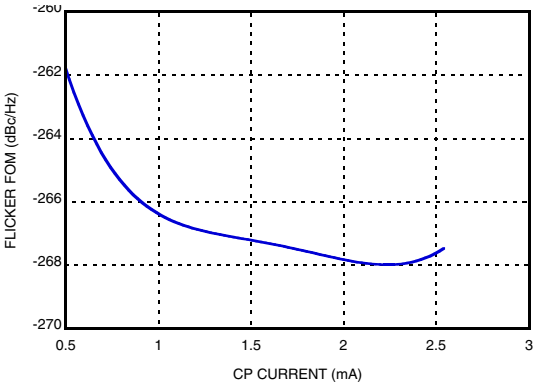


Figure 8. Floor FOM vs. CP Current, Fractional Mode B, 2.5 mA CP Current

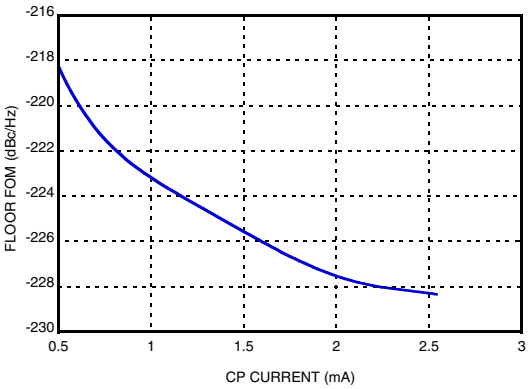


Figure 9. Flicker FOM vs. CP Voltage, CP Current = 2.5 mA [1]

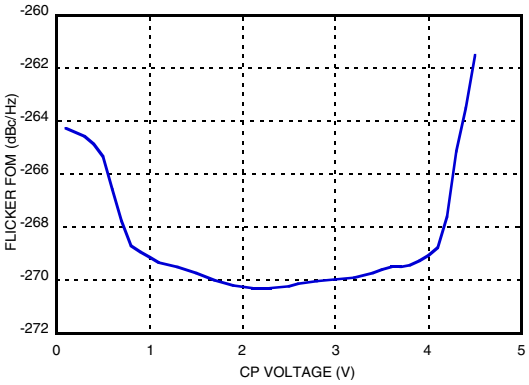


Figure 10. Floor FOM vs. CP Voltage, CP Current = 2.5 mA [1]

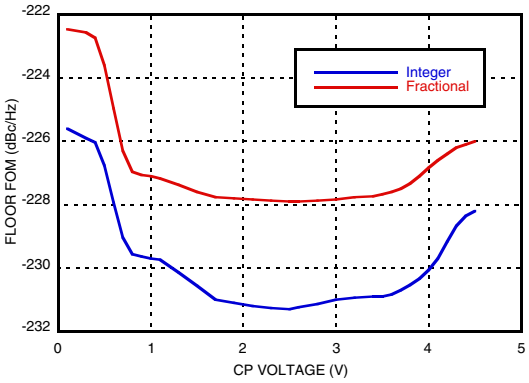


Figure 11. Flicker FOM vs. CP Voltage, HiKcp + CP Current = 6 mA [2]

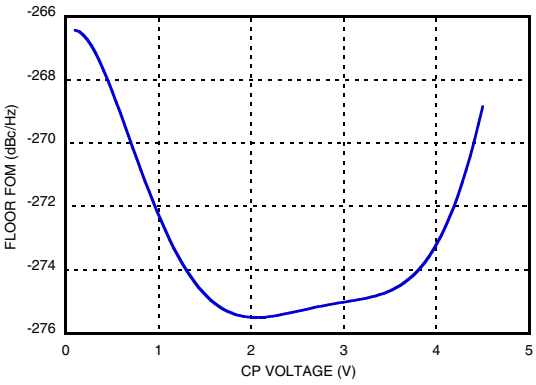
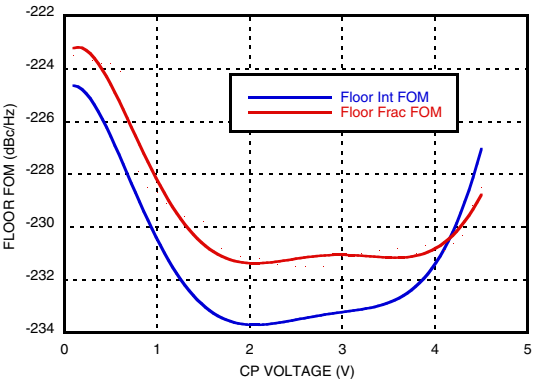


Figure 12. Floor FOM vs. CP Voltage, HiKcp + CP Current = 6 mA [2]



[2] Active Loop Filter, with DC bias point on -ve leg of op-amp swept.

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Figure 13. Typical Phase Noise & Spur Performance at 8 GHz + 200 kHz[3]

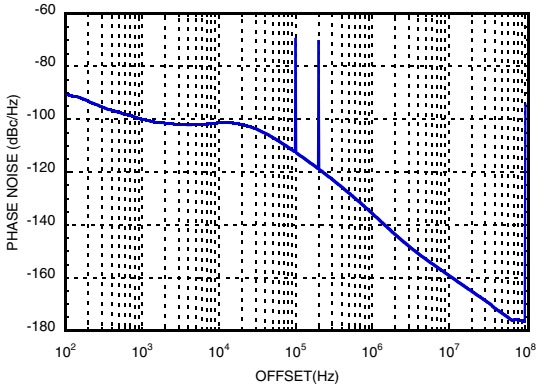


Figure 14. Fractional Performance, Exact Frequency Mode On at 8013.6 MHz [4]

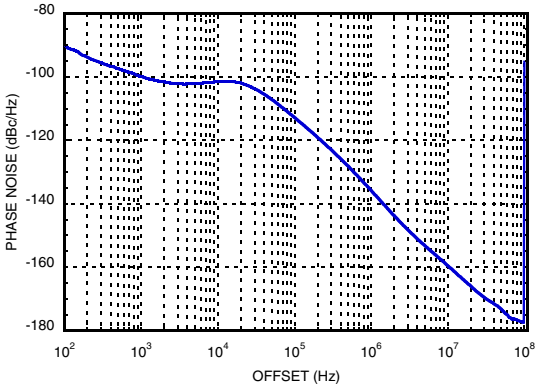


Figure 15. Integer Boundary Spur at 8 GHz + 20 kHz vs. Charge Pump Offset[5]

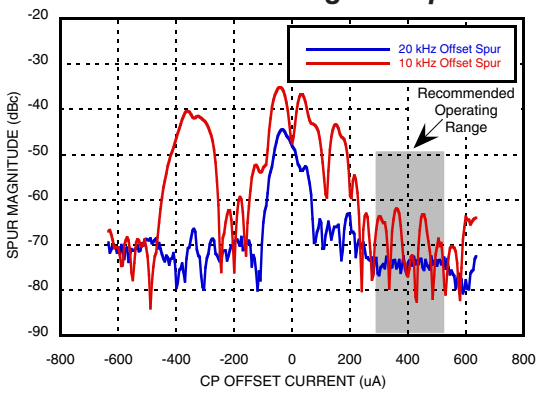


Figure 16. RF Input Limits [6]

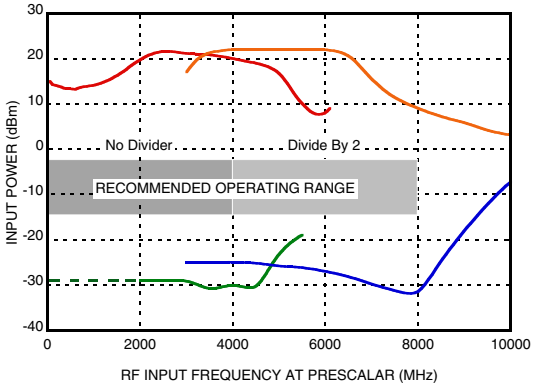


Figure 17. Modelled vs. Measured Phase Noise, Integer Mode HiK at 8 GHz [7]

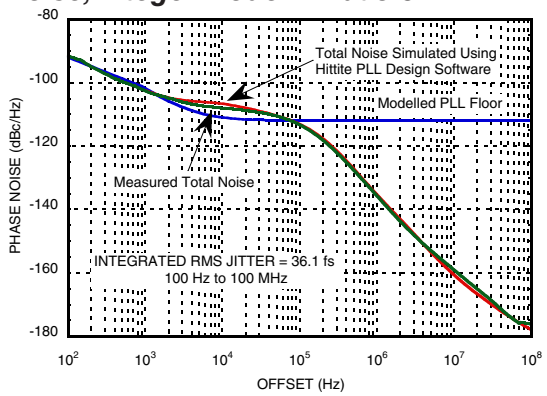
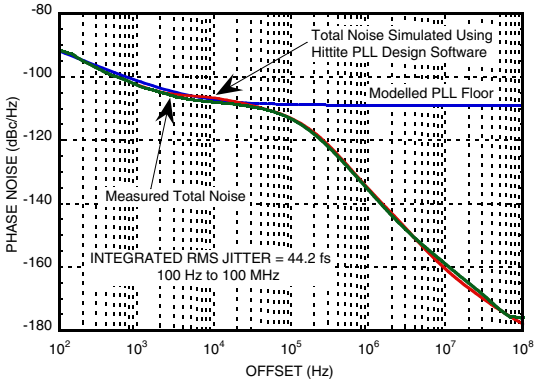


Figure 18. Modelled vs. Measured Phase Noise, Fractional Mode B, HiK at ~ 8 GHz [8]



[3] Output frequency = 8 GHz + 200 kHz using HMC508LP5E VCO, Reference Input = 100 MHz, PD frequency = 100 MHz, CP current = 2.5 mA, Fractional Mode B, 20 kHz bandwidth Loop Filter. Spur at 200kHz due to RF signal at 8GHz + 200kHz, spur at 100kHz due to prescaler input at 4GHz+100kHz. Reference feedthrough spur at 100 MHz offset.

[4] Exact Frequency Mode channel spacing 100 kHz, Fractional N, Rfout = 8013.6 MHz using HMC508LP5E VCO, Reference Input = 100 MHz, PD frequency = 100 MHz, Prescaler divide-by-2 selected. 20 kHz Loop Filter bandwidth, reference feedthrough spur at 100 MHz offset.

[5] Tuned to 8 GHz + 20 kHz, Prescaler at 4 GHz + 10 kHz, Loop bandwidth >> 20 kHz, Reference Frequency 50 MHz. Offset polarity should be positive for inverting configurations and negative otherwise.

[6] Low frequency minimum power levels not characterized. Low frequency limitation is only a function of external AC coupling capacitance signal slew rate.

[7] HiK integer mode measured at 8 GHz, Prescalar at 4 GHz, 50 MHz reference frequency.

[8] Active Fractional B Mode (Prescalar @ 4 GHz + 2.5 kHz), Reference Frequency 50 MHz.

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Figure 19. Floor FOM Near 8 GHz vs RF Input Power and Mode

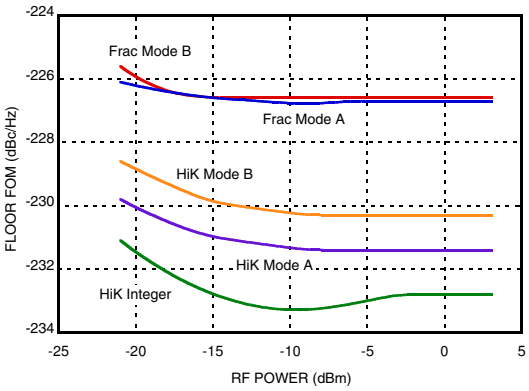


Figure 20. Flicker FOM Near 8 GHz vs. RF Input Power and Mode

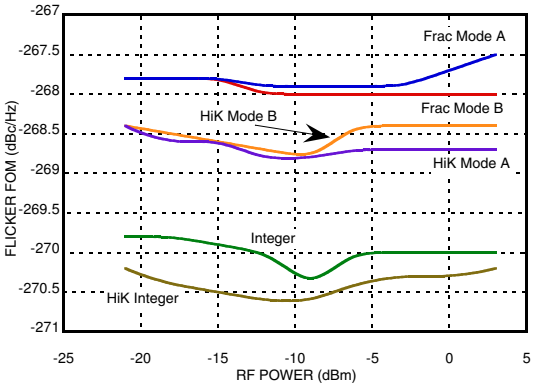


Figure 21. Reference Input Sensitivity, Square Wave, 50 Ω [9]

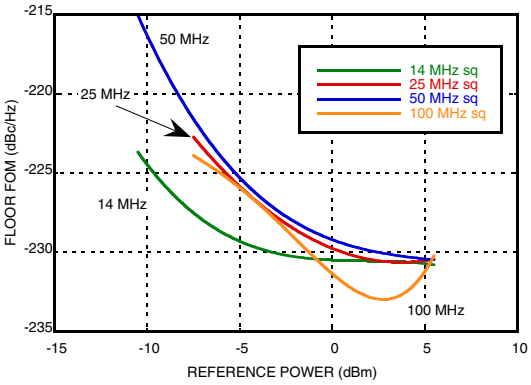


Figure 22. Reference Input Sensitivity Sinusoid Wave, 50 Ω [9]

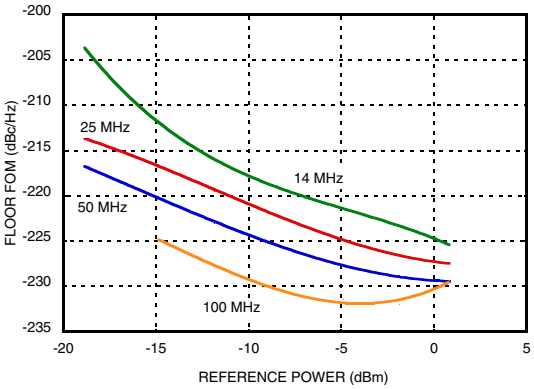


Figure 23. Reference Input Return Loss [10]

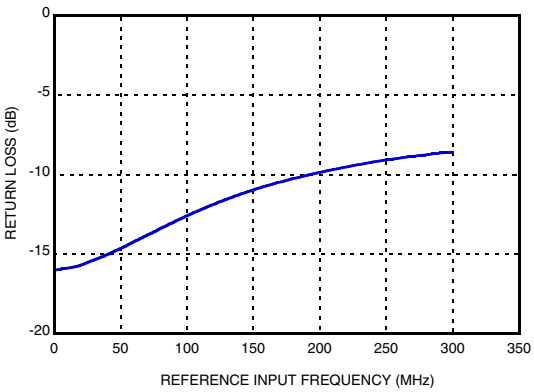
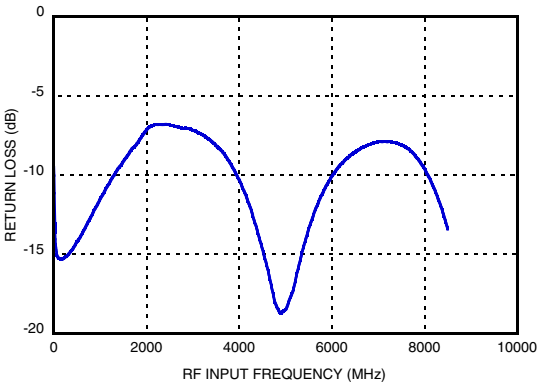


Figure 24. RF Input Return Loss [11]



[9] Measured with a 100 Ω external resistor termination, resulting in 50Ohm effective input impedance.. See "Reference Input Stage" for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[10] Measured with a 100 Ω external termination AC coupled on HMC703LP4E evaluation board, as in Figure 35.

[11] Measured with a 100 Ω external termination AC coupled on HMC703LP4E evaluation board, as in Figure 37.

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Application Support: pll@hittite.com

Figure 25. 2-Way Auto Sweep

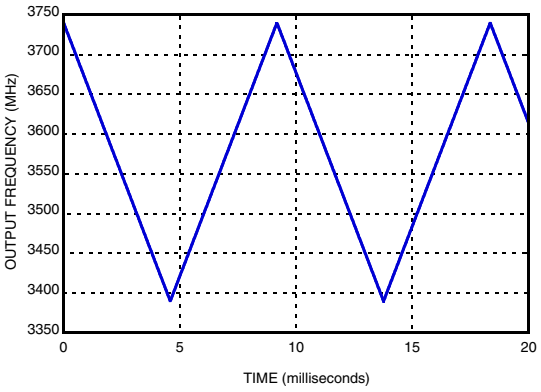


Table 2. Pin Descriptions

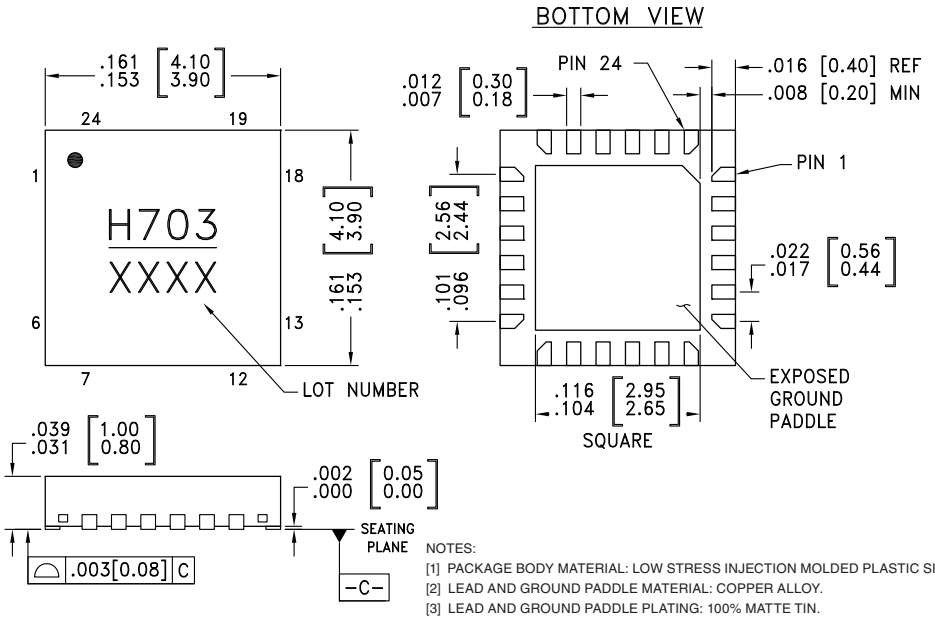
Pin Number	Function	Description
1	SCK	CMOS Input: Serial port clock
2	SDI	CMOS Input: Serial port data
3	DVDD	Power Supply for digital - Nominal 3.3 V MAX 25 mA, f_{PD} dependent
4	VDDIO	Power Supply for Digital IO - 3.3 V, 8 mA MAX (only when driving LD_SDO)
5	LD_SDO	CMOS Output: General Purpose Output - Lock Detect, Serial Data Out, others, Selectable
6	TRIG	CMOS Input : External Trigger pin.
7	N/C	No Connect
8	VCCPS	Power Supply for RF Divider, Nominal 3.3 V 35 mA MAX
9	N/C	No Connect
10	VCOIP	Differential RF Inputs. Normally AC Coupled, 2 V DC bias generated internally. For Single Ended operation, RFN must be AC coupled to the ground plane, typically 100 pF ceramic. DC Bias of 2.3 V is generated internally
11	VCOIN	
12	VCCHF	Power Supply for RF Buffer, Nominal 3.3 V, 6 mA MAX
13	VDDLS	Power Supply for PFD to CP Level Shifters, Nominal 5 V, 5 mA MAX, f_{PD} dependent.
14	VPPCPA	Power Supply for charge pump, Nominal 5 V, 10 mA MAX
15	CP	Charge pump output
16	AVDD	Power supply for analog bias generation, Nominal 3.3 V, 2 mA MAX
17	BIAS	External bypass decoupling for precision bias circuits, 1.920 V +/-2 mV NOTE: BIAS ref voltage cannot drive an external load. Must be measured with 10 GΩ meter such as Agilent 34410A, normal 10 MΩ DVM will read erroneously.
18	RVDD	Power Supply for Reference path, Nominal 3.3 V. 15 mA MAX reference dependent
19	N/C	No Connect
20	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
21	VDDPD	Power Supply for phase detector. Nominally 3.3 V. Decoupling for this supply is critical. 5 mA MAX, f_{PD} dependent
22	N/C	No Connect
23	CEN	CMOS Input: Hardware Chip Enable
24	SEN	CMOS Input: Serial port latch enable

Table 3. Absolute Maximum Ratings

Parameter	Rating
Max Vdc to paddle on supply pins 3,4,8,12,16,18,21	-0.3 V to +3.6 V
VDDLS, VPPCP	-0.3 V to +5.5 V
VCOIN, VCOIP Single Ended DC	VCCHF -0.2 V
VCOIN, VCOIP Differential DC	5.2 V
VCOIN, VCOIP Single Ended AC 50Ohm	+7 dBm
VCOIN, VCOIP Differential AC 50Ohm	+13 dBm
Digital Load	1 kΩ min
Digital Input 1.4 V to 1.7 V min rise time	20 nsec
Digital Input Voltage Range	-0.25 to VDDIO+0,5 V
Thermal Resistance (Jxn to Gnd Paddle)	25 °C/W
Operating Temperature Range	-40 °C to +85 °C
Storage Temperature Range	-65 °C to + 125 °C
Maximum Junction Temperature	+125 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity HBM	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 4. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC703LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1[2]	H703 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260°C

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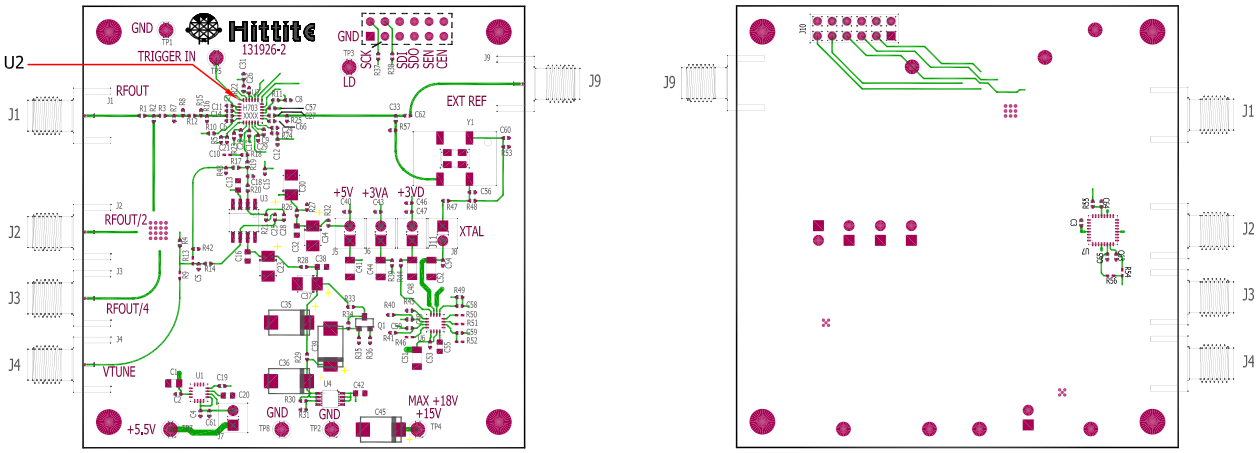
Evaluation PCB

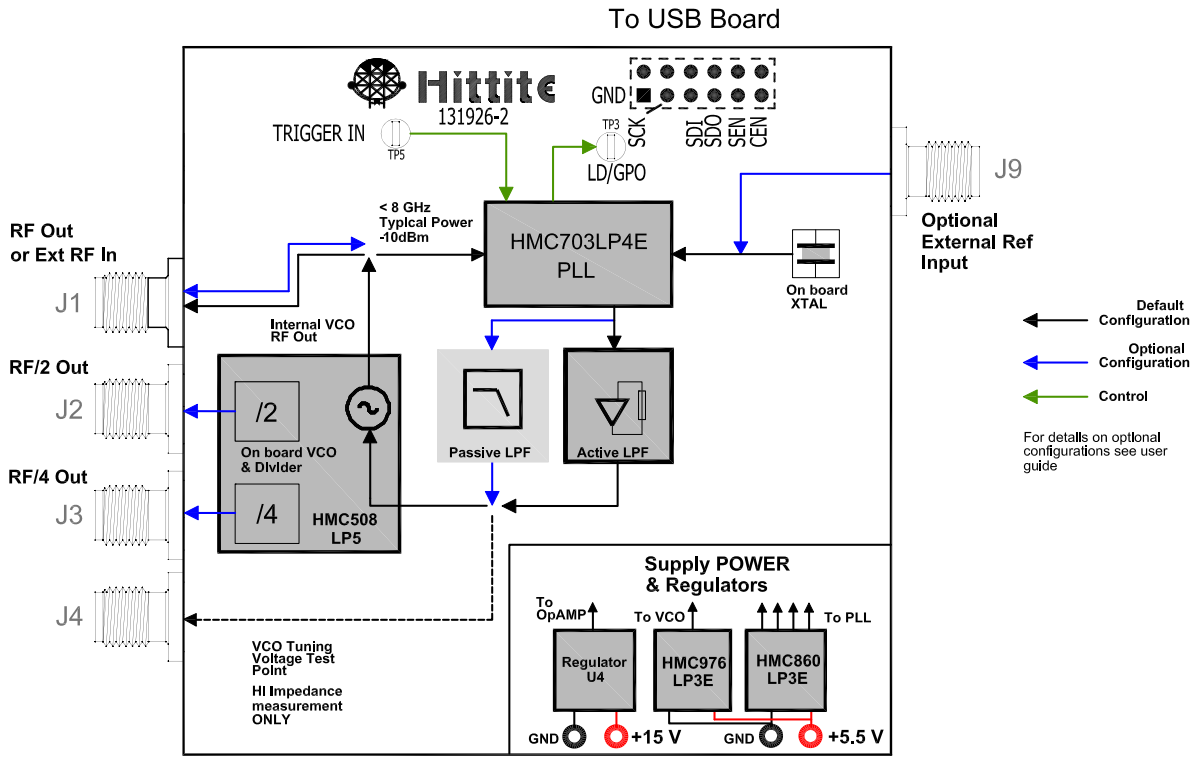


The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 5. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC703LP4E Evaluation PCB	EVAL01-HMC703LP4E
Evaluation Kit	HMC703LP4E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC703LP4E

Evaluation PCB Block Diagram



Evaluation PCB Schematic

To view Evaluation PCB Schematic please visit www.hittite.com and choose HMC703LP4E from "Search by Part Number" pull down menu to view the product splash page.

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Theory Of Operation

PLL Basics

In its most trivial form, a synthesizer IC, such as the HMC703LP4E forms the heart of the control loop to multiply a low frequency reference source up to a higher frequency. The phase detector (PD) and charge-pump (CP) drive the tuning signal of a voltage-controlled oscillator in an attempt to bring the phases, at the phase-detector input, into alignment. If the loop can manage this, it means that the phase detector inputs (reference and DIV) must also be at the same frequency. Since the frequency of the DIV signal = fvco / N, this means the control loop must have forced the frequency of the VCO output must be locked to N x fpd.

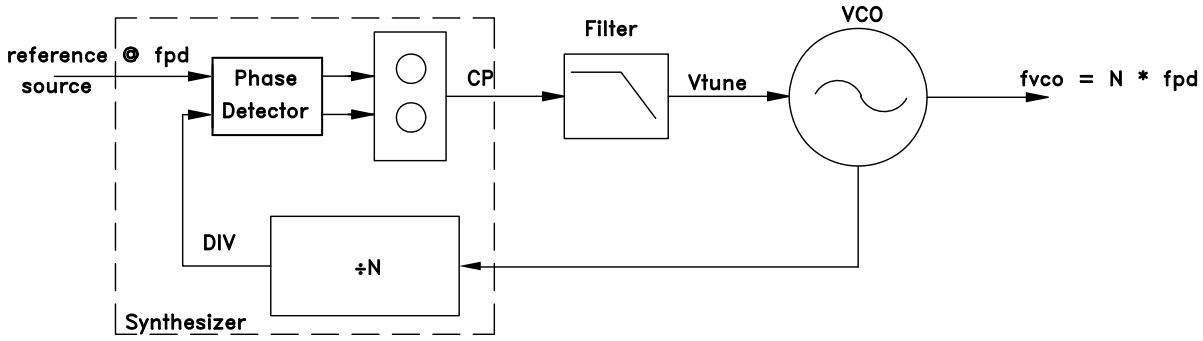

Figure 26. Typical PLL

In integer synthesizers, N can only take on discrete values (eg. 200, 201, etc.). In fractional synthesizers, such as the HMC703LP4E and others, N can also take on fractional levels, eg. N=20.4. In theory, the fractional divider normally permits higher phase-detector frequencies for a given output frequency, with associated improvements in signal quality (phase-noise). Unfortunately, fractional synthesizers suffer from imperfections which do not effect integer synthesizers. These problems can effect the phase noise, but more seriously they tend to manifest as spurious emissions - and these spurs are the most serious drawback of fractional synthesis.

Hittite's fractional synthesizer family (including the HMC703LP4E) offer drastic performance advantages over other fractional synthesizers in the industry.

The HMC703LP4E synthesizer consists of the following functional blocks:

1. Reference Path Input Buffer and 'R' Divider
2. VCO Path Input Buffer, RF Divide-by-2 and Multi-Modulus 'N' Divider
3. $\Delta\Sigma$ Fractional Modulator
4. Phase Detector
5. Charge Pump
6. Main Serial Port
7. Lock Detect and Register Control
8. Power On Reset Circuit

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High Performance Low Spurious Operation

The HMC703LP4E has been designed for the best phase noise and low spurious content possible in an integrated synthesizer. Spurious signals in a synthesizer can occur in any mode of operation and can come from a number of sources.

Figure of Merit, Noise Floor, and Flicker Noise Models

The phase noise of an ideal phase locked oscillator is dependent upon a number of factors:

a. Frequency of the VCO, and the Phase detector

b. VCO Sensitivity, kvco, VCO and Reference Oscillator phase noise profiles

c. Charge Pump current, Loop Filter and Loop Bandwidth

d. Mode of Operation: Integer, Fractional modulator style

The contributions of the PLL to the output phase noise can be characterized in terms of a Figure of Merit (FOM) for both the PLL noise floor and the PLL flicker (1/f) noise regions, as follows:

where:

Φ_p^2	Phase Noise Contribution of the PLL (rads²/Hz)
f_o	Frequency of the VCO (Hz)
f_{pd}	Frequency of the Phase Detector (Hz)
f_m	Frequency offset from the carrier (Hz)
F_{po}	Figure of Merit (FOM) for the phase noise floor
F_{p1}	Figure of Merit (FOM) for the flicker noise region

PLL Phase Noise Contribution

$$\Phi_p^2(f_0, f_m, f_{pd}) = \frac{F_{p1} f_0^2}{f_m} + \frac{F_{p0} f_0^2}{f_{pd}} \qquad \textit{(EQ 1)}$$

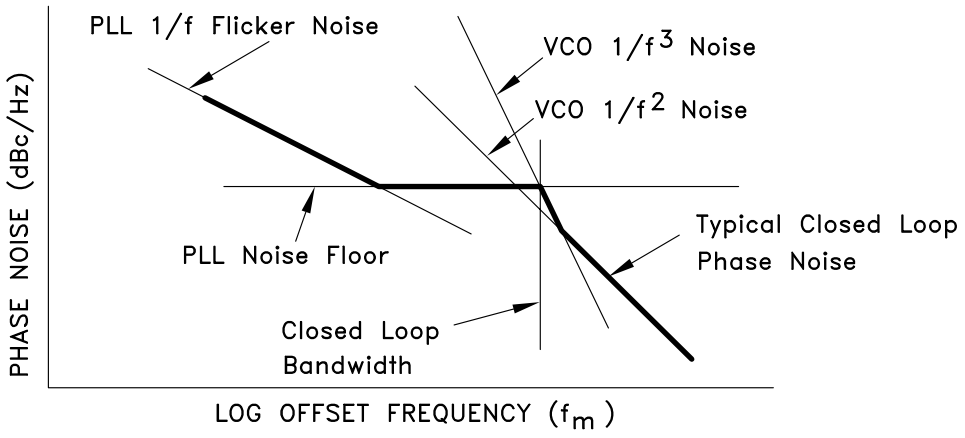

Figure 27. Figure of Merit Noise Models for the PLL

If the free running phase noise of the VCO is known, it may also be represented by a figure of merit for both $1/f^2$, F_{v2}, and the $1/f^3$, F_{v3}, regions.

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VCO Phase Noise Contribution

$$\Phi_v^2(f_0, f_m) = \frac{F_{v2} f_0^2}{f_m^2} + \frac{F_{v3} f_0^2}{f_m^3} \quad \textit{(EQ 2)}$$

The Figures of Merit are essentially normalized noise parameters for both the PLL and VCO that can allow quick estimates of the performance levels of the PLL at the required VCO, offset and phase detector frequency. Normally, the PLL IC noise dominates inside the closed loop bandwidth of the synthesizer, and the VCO dominates outside the loop bandwidth at offsets far from the carrier. Hence a quick estimate of the closed loop performance of the PLL can be made by setting the loop bandwidth equal to the frequency where the PLL and free running phase noise are equal.

The Figure of Merit is also useful in estimating the noise parameters to be entered into a closed loop design tool such as Hittite PLL Design, which can give a much more accurate estimate of the closed loop phase noise and PLL loop filter component values.

Given an optimum loop design, the approximate closed loop performance is simply given by the minimum of the PLL and VCO noise contributions.

PLL-VCO Noise

$$\Phi^2 = \min\left(\Phi_p^2, \Phi_v^2\right) \quad \textit{(EQ 3)}$$

An example of the use of the FOM values to make a quick estimate of PLL performance: Estimate the phase noise of an 8 GHz closed loop PLL with a 100 MHz reference operating in Fractional Mode B with the VCO operating at 8 GHz and the VCO divide by 2 port driving the PLL at 4 GHz. Assume an HMC509 VCO has free running phase noise in the $1/f^2$ region at 1 MHz offset of -135 dBc/Hz and phase noise in the $1/f^3$ region at 1 kHz offset of -60 dBc/Hz.

F_{v1_dB} =	-135	Free Running VCO PN at 1MHz offset
	+20*log10(1e6)	PNoise normalized to 1Hz offset
	-20*log10(8e9)	Pnoise normalized to 1Hz carrier
	= -213.1 dBc/Hz at 1Hz	VCO FOM
F_{v3_dB} =	-60	Free Running VCO PN at 1kHz offset
	+30*log10(1e3)	PNoise normalized to 1Hz offset
	-20*log10(8e9)	Pnoise normalized to 1Hz carrier
	= -168 dBc/Hz at 1Hz	VCO Flicker FOM

We can see from Figure 3 and Figure 4 respectively that the PLL FOM floor and FOM flicker parameters in fractional Mode A:

Fpo_dB = -227 dBc/Hz at 1Hz
Fp1_dB = -266 dBc/Hz at 1Hz

Each of the Figure of Merit equations result in straight lines on a log-frequency plot. We can see in the example below the resulting

PLL floor at 8 GHz = F_{po_dB} +20log10(fvco) -10log10(fpd) = -227+198 -80 = -109 dBc/Hz
PLL Flicker at 1 kHz = F_{p1_dB}+20log10(fvco)-10log10(fm) = -266 +198-30 = -98 dBc/Hz
VCO at 1 MHz = F_{v1_dB}+20log10(fvco)-20log10(fm)= -213 +198-120 = -135 dBc/Hz
VCO flicker at 1 kHz = F_{v3_dB}+20log10(fvco)-30log10(fm)= -168 +198-90 = -60 dBc/Hz

These four values help to visualize the main contributors to phase noise in the closed loop PLL. Each falls on a linear line on the log-frequency phase noise plot shown in Figure 27.

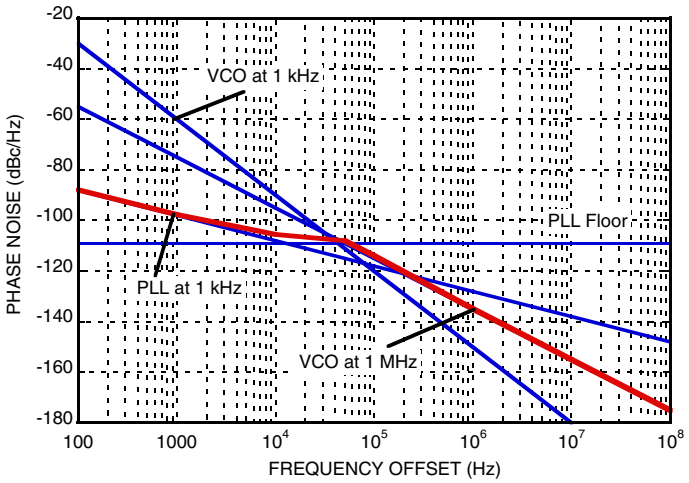

Figure 28. Figure of Merit Example

It should be noted that actual phase noise near the corner frequency of the loop bandwidth is affected by loop parameters and one should use a more complete design tool such as Hittite PLL Design for better estimates of the phase noise performance. Noise models for each of the components in Hittite PLL Design can be derived from the FOM equations or can be provided by Hittite applications engineering.

Spurious Performance

Integer Operation

The VCO always operates at an integer multiple of the PD frequency in an integer synthesizer. In general, spurious signals originating from an integer synthesizer can only occur at multiples of the PD frequency. These unwanted outputs are often simply referred to as reference sidebands.

Spurs unrelated to the reference frequency must originate from outside sources. External spurious sources can modulate the VCO indirectly through power supplies, ground, or output ports, or bypass the loop filter due to poor isolation of the filter. It can also simply add to the output of the synthesizer.

The HMC703LP4E has been designed and tested for ultra-low spurious performance. Reference spurious levels are typically below -100 dBc with a well designed board layout. A regulator with low noise and high power supply rejection, such as the HMC860LP3E, is recommended to minimize external spurious sources.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the synthesizer and isolation of the VCO load from the synthesizer. Typical board layout, regulator design, demo boards and application information are available for very low spurious operation. Operation with lower levels of isolation in the application circuit board, from those recommended by Hittite, can result in higher spurious levels.

Of course, if the application environment contains other interfering frequencies unrelated to the PD frequency, and if the application isolation from the board layout and regulation are insufficient, then the unwanted interfering frequencies will mix with the desired synthesizer output and cause additional spurs. The level of these spurs is dependant upon isolation and supply regulation or rejection (PSRR).

Fractional Operation

Unlike an integer synthesizer, spurious signals in a fractional synthesizer can occur due to the fact that the VCO operates at frequencies unrelated to the PD frequency. Hence intermodulation of the VCO and the PD harmonics can cause spurious sidebands. Spurious emissions are largest when the VCO operates very close to an integer multiple of the PD. When the VCO operates exactly at a harmonic of the PD then, no in-close mixing products are present.

Interference is always present at multiples of the PD frequency, f_{pd}, and the VCO frequency, f_{vco}. If the fractional mode of operation is used, the difference, Δ, between the VCO frequency and the nearest harmonic of the reference, will create what are referred to as integer boundary spurs. Depending upon the mode of operation of the synthesizer, higher order, lower power spurs may also occur at multiples of integer fractions (sub-harmonics) of the PD frequency. That is, fractional VCO frequencies which are near $nf_{pd} + f_{pd}d/m$, where n, d and m are all integers and d≤m (mathematicians refer to d/m as a rational number). We will refer to $f_{pd}d/m$ as an integer fraction. The denominator, m, is the order of the spurious product. Higher values of m produce smaller amplitude spurious at offsets of mΔ and usually when m>4 spurs are very small or unmeasurable.

The worst case, in fractional mode, is when d=1, and the VCO frequency is offset from nf_{pd} by less than the loop bandwidth. This is the "in-band fractional boundary" case.

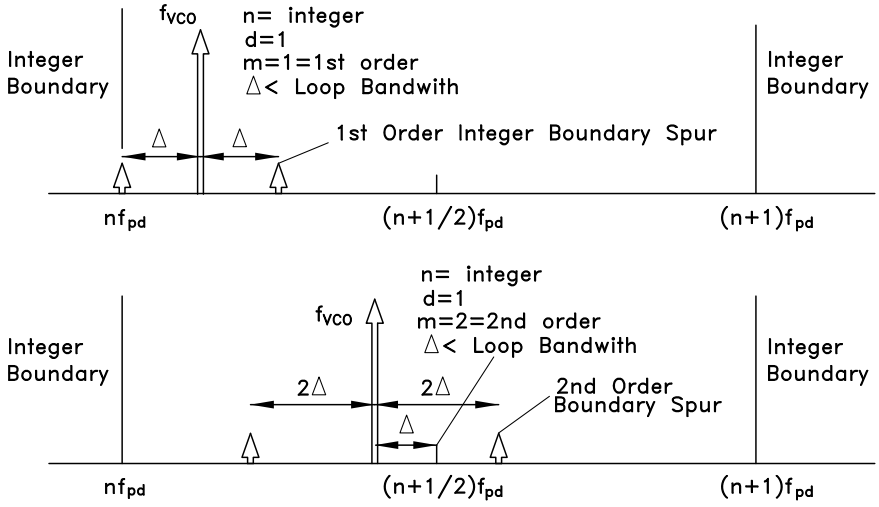

Figure 29. Fractional Spurious Example

Characterization of the levels and orders of these products is not unlike a mixer spur chart. Exact levels of the products are dependent upon isolation of the various synthesizer parts. Hittite can offer guidance about expected levels of spurious with our PLL and VCO application boards. Regulators with high power supply rejection ratios (PSRR) are recommended, especially in noisy applications.

When operating in fractional mode, charge pump and phase detector linearity is of paramount importance. Any non-linearity degrades phase noise and spurious performance. Phase detector linearity degrades when the phase error is very small and is operating back and forth between reference lead and VCO lead. To mitigate these non-linearities in fractional mode it is critical to operate the phase detector with some finite phase offset such that either the reference or VCO always leads. To provide a finite phase error, extra current sources can be enabled which provide a constant DC current path to VDD (VCO leads always) or ground (reference leads always). These current sources are called charge pump offset and they are controlled via Reg 09h. The time offset at the phase detector should be ~2.5 ns + 4 T_{ps}, where T_{ps} is the RF period at the fractional prescaler input in nanoseconds (ie. after the optional fixed divide by 2). The specific level of charge pump offset current is determined by this time offset, the comparison frequency and the charge pump current and can be calculated from:

$$\text{Required CP Offset} = (2.5 \cdot 10^{-9} + 4T_{PS}) \cdot (F_{comparison}) \cdot I_{CP} \text{ where:} \quad \textbf{(EQ 4)}$$

T_{PS}: is the RF period at the fractional prescaler input

I_{CP}: is the full scale current setting of the switching charge pump

Note that this calculation can be performed for the center frequency of the VCO, and does not need refinement for small differences (<25%) in center frequencies. Also, operation with unreasonably large charge pump offset may cause Lock Detect to incorrectly indicate an unlocked condition. To correct, reduce the offset to recommended levels.

Another factor in Fractional spectral performance is the choice of the Delta-Sigma Modulator mode. Mode B is normally recommended, as it allows higher PD frequencies and makes it easier to filter the fractional quantization noise. For low prescaler frequencies (<1.5GHz), however, mode A can offer better in-band spectral performance. See Reg 06h[0] for DSM mode selection. Finally, all fractional synthesizers create fractional spurs at some level. Hittite offers the lowest level fractional spurious in the industry in an integrated solution.

Operational Modes

The HMC703LP4E can operate in a eight of different modes (Reg 06h[7:5]), and supports "Triggering" from 3 different sources. The modes of operation include:

"Integer Mode"

"Fractional Mode"

"Exact Frequency Mode"

Frequency Modulation "FM Mode"

Phase Modulation "PM Mode"

"Frequency Sweep Mode" (3 types)

All modes require Fractional mode to be enabled except for Integer mode. Fractional mode allows fine frequency steps. Exact Frequency mode allows precise fractional frequency steps with zero frequency error. FM and PM modes can be used for simple communications links, with data rate limitations set by the loop filter bandwidth. The PM mode also allows for precise incremental phase adjustments, which can be important in phased arrays and other systems. Frequency sweep supports built-in one-way, two-way, or user defined frequency sweeps, useful in FMCW radar applications.

Depending on the mode, the auxiliary registers Reg 0Ah, Reg 0Ch and Reg 0Dh are used for different functions, as shown in Table 6.

Table 6. Operational Modes

Register Number	Register Name	PLL Operating Mode (SD_MODE = Reg 06h[7:5])					
		0	1	2	3	4	5 to 7
		Fractional Mode	Integer Mode	Exact Frequency Mode	FM (Frequency Modulation) Mode	PM (Phase Modulation) Mode	Ramp Mode
Function of Reg 03h	N Integer Part	Nint	N	Nint	Freq 1: Nint	Nint	Start Nint
Function of Reg 04h	N Fractional Part	Nfrac		Nfrac	Freq 1: Nfrac	Nfrac	Start Nfrac
Function of Reg 0Ah	Aux Register					Phase Step	Frequency step / reference clock
Function of Reg 0Ch	Alternate Integer				Freq 2: Nint		STOP Nint
Function of Reg 0Dh	Alternate Fractional			Channels / PD frequency	Freq 2: Nfrac		STOP Nfrac
Additional Functionality							
Double Buffer		YES	NO	YES	YES	YES	YES
On Trigger		Updates frequency, optionally initiates phase		Updates frequency, optionally initiates phase	Toggles frequency (level sensitive)	Increments / decrements phase	Proceeds to next stage of ramp

Those registers which are unused in a particular mode can take on any value, and are ignored.

Triggering

Depending on the operating mode, a trigger event is used to change frequency, FM modulate the frequency, modulate the phase, or advance the frequency ramp profile to its next state. In general the HMC703LP4E can be triggered via one of three methods. Not all modes support all trigger methods.

1. An external hardware trigger pin-6 (TRIG)
2. SPI write to TRIG BIT in Reg 0Eh[0]
3. SPI write to fractional register Reg 04h (frequency hopping triggers only).

Depending on the mode, the part is sensitive to either the rising edge, or the level of the trigger. The SPI's TRIG bit emulates the external TRIG pin, and so it must typically be written to 1 for a trigger, and then back to 0 in preparation for another trigger cycle. To use the external TRIG pin, it must be enabled via EXTTRIG_EN (Reg 06h[9]).

Fractional Mode or Exact Frequency Mode Frequency Updates

In non-modulated fractional modes (Reg 06h[7:5] = 0 or 2), if the external trigger is enabled, writes to N_{INT} and N_{frac} (Reg 03h and Reg 04h) are internally buffered and wait for an explicit trigger via either the TRIG pin or the SPI's TRIG bit before taking effect. If EXTTRIG_EN = 0, the write to N_{INT} is double-buffered, and waits for a fractional write to Reg 04h so that both N_{INT} and N_{frac} are internally recognized together. See the "Fractional Mode" section for more information on calculating the fractional multiplier for your application.

Initial Phase Control

On the HMC703LP4E, the user has control of the initial phase of the VCO via the 24-bit SEED Reg 05h. This seed phase is loaded on the 1st clock cycle following a trigger event, provided that autoseed (Reg 06h [8] = 1) is enabled. The value in Reg 05h represents the phase of the VCO. For example, if two synthesizers are triggered in parallel, but one has a SEED of 0.2 (0.2×2^{24}) and the other has a SEED of 0.7 (0.7×2^{24}), the steady state outputs of the two VCOs

(not accounting for any mismatch) will be 180° out of phase = ((0.7-0.2) x 360°). The user can take advantage of this for phase control of the outputs of multiple synthesizers.

If phase control is not needed, the best spurious operation is achieved with the SEED set to a busy binary number, for example 50F1CDh, or B29D08h.

Note that in Exact Frequency mode with an exact step of f_{step}, if autoseed is off, there can be a delay of up to $1/f_{step}$ after a trigger before a new fractional frequency is recognized.

Frequency Tuning

Integer Mode

In integer mode the VCO step size is fixed to that of the PD frequency, f_{pd}. Integer mode typically has lower phase noise than fractional mode for a given PD operating frequency. The advantage is usually of the order of 2 to 3 dB. Integer mode, however, often requires a lower PD frequency to meet channel step size requirements. The fractional mode advantage is that higher PD frequencies can be used, hence lower phase noise can often be realized. "Charge Pump Offset" should be disabled in integer mode. In integer mode the ΔΣ modulator is shut off and the N divider (Reg 03h) may be programmed to any integer value in the range 16 to 2^{16}-1. To use the HMC703LP4E in integer mode program Reg 06h[7:5] = 1, then program the integer portion of the frequency (as per (EQ 5)), ignoring the fractional part.

There is no double buffering in integer mode, i.e. write data then trigger the frequency change later. A write to the N_{INT} register (Reg 03h) immediately starts the RF frequency hop. There is no external trigger available in this mode. If double buffering is required, use fractional mode (Reg 06h[7:5] = 0), with N_{frac} (Reg 04h) = 0, and SEED (Reg 05h) = 0.

Fractional Mode

The HMC703LP4E is placed into fractional mode by setting SD_MODE (Reg 06h[7:5]) = 0

The frequency of a locked VCO controlled by the HMC703LP4E, f_{vco}, is given by

$$f_{ps} = \frac{f_{xtal}}{R}\,(N_{int} + N_{frac}) = f_{int} + f_{frac} \qquad \textbf{(EQ 5)}$$

$$f_{vco} = k\, f_{ps} \qquad \textbf{(EQ 6)}$$

Where:

f_{ps}	is the frequency at the prescalar input after any potential RF divide by 2
f_{vco}	is the frequency at the HMC703LP4E's RF port
k	is 1 if the RF Divide by 2 is bypassed, 2 if on (Reg 08h[17])
N_{int}	is the integer division ratio, Reg 03h, an integer between 20 and 2^{16}- 1
N_{frac}	is the fractional part, from 0.0 to 0.99999...,N_{frac}=Reg 04h/2^{24}
R	is the reference path division ratio, Reg 02h
f_{xtal}	is the frequency of the reference oscillator input
f_{pd}	is the PD operating frequency, f_{xtal}/R

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As an example, suppose we want to tune a VCO to 7910 MHz. Since the input frequency is > 4 GHz, the RF divide-by-2 must be engaged, so k=2:

f_{vco}	7,910 MHz
k	2
f_{ps}	3,955 MHz
f_{xtal}	= 50 MHz
R	= 1
f_{pd}	= 50 MHz
N_{int}	= 79
N_{frac}	= 0.1
Reg 04h	= round(0.1 x 2^{24}) = round(1677721.6) = 1677722

$$f_{ps} = \frac{50e6}{1}\left(79 + \frac{1677722}{2^{24}}\right) = 3955\ MHz + 1.2\ Hz\ error \qquad \textbf{(EQ 7)}$$

$$f_{vco} = 2\ (3955 + 1.2\ Hz) = 7910\ MHz + 2.4\ Hz\ error \qquad \textbf{(EQ 8)}$$

In this example the output frequency of 7910 MHz is achieved by programming the 16-bit binary value of 79d = 4Fh = 0000 0000 0100 1111 into *intg_reg* in Reg 03h, and the 24-bit binary value of 1677722d = 19999Ah = 0001 1001 1001 1001 1001 1010 into *frac_reg* in Reg 04h. The 2.4 Hz quantization error can be eliminated using the exact frequency mode if required.

Exact Frequency Mode

The absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example a 24 bit fractional modulator has frequency resolution set by the phase detector (PD) comparison rate divided by 2^{24}. In the case of a 50 MHz PD rate, this would be approximately 2.98 Hz, or 0.0596 ppm.

In some applications it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated. In some fractional synthesizers it is necessary to shorten the length of the accumulator (the denominator or the modulus) to accommodate the exact period of the step size. The shortened accumulator often leads to very high spurious levels at multiples of the channel spacing, $f_{step} = f_{PD}$/Modulus. For example 200 kHz channel steps with a 10 MHz PD rate requires a modulus of just 50. The Hittite method achieves the exact frequency step size while using the full 24 bit modulus, thus achieving exact frequency steps with very low spurious and a high comparison rate, which maintains excellent phase noise.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (eg. N = 50.0,50.5,50.25,50.75 etc.). Unfortunately, some common frequencies cannot be exactly represented. For example, N_{frac} = 0.1 = 1/10 must be approximated as round((0.1 x 2^{24})/ 2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz this translates to 1.2 Hz error. HMC703LP4E exact frequency mode addresses this issue, and can eliminate quantization error by programming the $N_{channels}$ (Reg 0Dh) to 10 (in this example). More generally, this feature can be used whenever the prescaler frequency, f_{ps}, can be exactly represented on a step plan where there are an integer number ($N_{channels}$) of frequency steps across integer-N boundaries. Assuming the RF divide by 2 is disabled so that f_{ps}=f_{vco}, this holds when the VCO frequency, f_{vco} satisfies (EQ 9), shown graphically in Figure 30.

$$f_{VCO} \bmod \left(f_{gcd} \right) = 0, \quad \text{where } f_{gcd} = \gcd(f_{VCO}, f_{PD}) \qquad \textit{(EQ 9)}$$
$$N_{channels} = f_{PD} / f_{gcd}, \text{ and } N_{channels} < 2^{24}$$

Where:

f_{PD} = frequency of the Phase Detector
f_{VCO} is the desired output frequency
f_N , f_N+1 are integer multiples of the Phase Detector
f_{gcd} stands for Greatest Common Divisor
eg. f_{gcd} (4000.200MHz, 50MHz)
= *200kHz*
therefore $N_{channels}$ = *50 MHz/200 kHz = 250*
f_{VCOn} are other VCO frequencies we can exactly tune to, given this f_{gcd} spacing

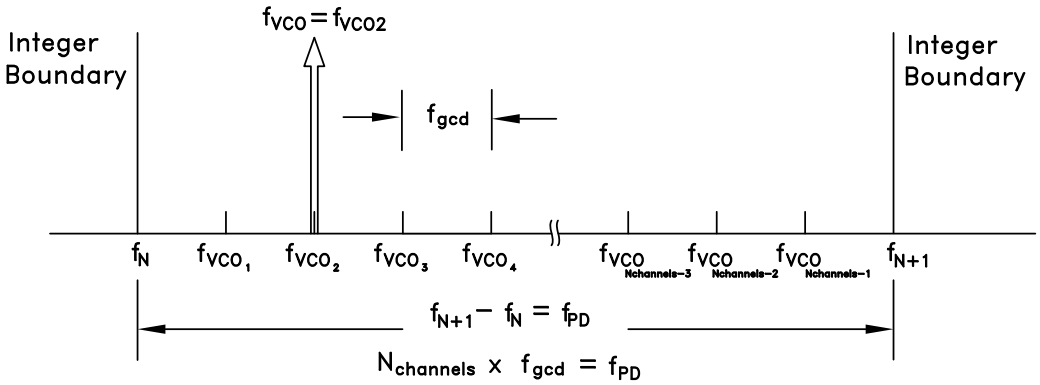

Figure 30. Exact Frequency Tuning

In the previous paragraph, it was assumed that a single frequency was to be achieved with zero error. Exact frequency mode also applies to cases where many exact frequencies are required, all of which fit on a particular channel spacing.

Example: To achieve exactly 50 kHz channel steps with a 61.44 MHz reference, calculate f_{gcd} and $N_{channels}$:

f_{PD} = 61.44 MHz
f_{step} = 50 kHz
f_{gcd} (61.44 MHz, 50 kHz)
Using the Euclidean algorithm to find the greatest common denominator:
61.440 MHz = 50 kHz x 1228 + 50 kHz
50 kHz = 40 kHz x 1 + 10 kHz
40 kHz = 10 kHz x 4 + 0 (0 remainder, algorithm complete)
f_{gcd} (61.44 MHz, 50 kHz) = 10 kHz
$N_{channels}$ = *61.44 MHz / 10 kHz = 6144*

For improved spectral performance (to keep spurs low and further out of band), it is best to keep f_{gcd} as high as possible ($N_{channels}$ as low possible) for a given application.

Using Hittite Exact Frequency Mode

To use Exact Frequency Mode, we recommend the following procedure:

1. Calculate the required f_{gcd} as either gcd(f_{VCO}, f_{PD}) or gcd(f_{PD}, f_{step}) depending on your application
2. Calculate the number of channels per integer boundary, $N_{channels}$= f_{PD} / f_{gcd} and program into Reg 0Dh
3. Set the modulator mode to Exact Frequency (SD_MODE in Reg 06h[7:5] = 2)

Then, for each frequency of interest, f_{VCO}:

4 Calculate the approximate value of N that is required: $N = f_{VCO}/f_{PD} = N_{INT} + N_{frac}$

5. Program N_{INT} into integer register Reg 03h
   Note: There is no need to re-program N_{INT} if it has not changed from the previous set-point.

6. Program the fractional register, Reg 04h = Ceiling(N_{frac}*2^{24})
   where the ceiling function means "round up to the nearest integer."

Example: To configure HMC703LP4E for exact frequency mode with channel spacing of 50 kHz, VCO frequency = 2000.200 MHz and f_{PD} =61.44 MHz:

1. f_{gcd}(61.44 MHz, 50 kHz) = 10 kHz (as above)
2. Calculate $N_{channels}=f_{PD} / f_{gcd}$ = 6144. Program into Reg 0Dh (6144 dec = 1800 hex)
3. Set the modulator mode to Exact Frequency (SD_MODE in Reg 06h[7:5] = 2)
4. Calculate N = 2000.2 MHz / 61.44 MHz = 32.55533854 = 32 + 0.55533854
5. Program integer divisor N_{INT} (Reg 03h) = 32d = 20h
6. Program fractional divisor Reg 04h= CEILING(0.55533854 x 2^{24}) = 9,317,035 = 8E2AABh

In the above example, without exact frequency mode, there would have been a -1.2 Hz error due to quantization.

FM Mode

The HMC703LP4E PM mode supports simple FSK modulation via a level sensitive trigger. FM mode can be used for simple communications links, with data rate limitations set by the loop filter bandwidth.

The HMC703LP4E is configured to operate in FM mode by writing Reg 06h[7:5] = 3.

The FM mode allows the user to toggle between two frequencies $F_0 = N_1*f_{PD}$ and $F_1 = N_2*f_{PD}$ based on the level of the TRIG.

The following procedure is recommended to configure HMC703LP4E to FM mode:

1. Lock in fractional mode (Reg 06h[7:5]= 0) to $F_0 = f_{PD}$ x (Reg 03h.Reg 04h).
2. Program (Reg 0Ch.Reg 0Dh) for F_1.
3. Change mode to FM (Reg 06h[7:5] = 3).
4. Select the trigger source Reg 06h[9] = 1, TRIG (pin-6), or Reg 06h[9] = 0 - trigger from SPI bit Reg 0Eh[0]
5. Switch between F_0 and F_1 on a trigger state 0/1 = F_0/F_1.

It is possible to change the next frequency state between trigger events, without affecting the output - ie. write the F_0 value while on F_1, or F_1 while on F_0 .

PM Mode

The HMC703LP4E PM mode supports simple bi-phase modulation via a level sensitive trigger. PM mode also supports programmable phase steps via an edge sensitive trigger. PM modes can be used for simple communications links, with data rate limitations set by the loop filter bandwidth.

The HMC703LP4E is configured to operate in all PM mode by writing Reg 06h[7:5] = 4. In general the modulation phase step, $\Delta\theta$, in either PM mode is given by

$$\Delta\theta = \frac{x \times 360}{2^{24}} \quad \text{(deg)}$$

where x = Reg 0Ah.

Bi-Phase Modulation

Phase step is programmed in Reg 0Ah as a fraction of 2π, where 2^{24} = 2π. For example, for bi-phase modulation a phase step of 180°, program Reg 0Ah= round((180/360) x 2^{24} = 8388608d = 800000h).

Phase modulation data is input via a "trigger" source, where the trigger is level dependent (Reg 06h[8] = 0), high trigger advances the phase and low trigger returns the phase.

Phase Step Control

Phase may also be advanced on the rising edge of the trigger only. Phase step is programmed in Reg 0Ah as a fraction of 360°, where 2^{24} = 2π. For example, for a 1° phase step, program Reg 0Ah= round((1/360) x 2^{24} = 46603d =B60Bh)

In summary the following procedure is recommended to configure HMC703LP4E for PM mode:

1. Lock in fractional mode (Reg 06h[7:5] = 0) to F = f_{PD} x (Reg 03h.Reg 04h).
2. Program (Reg 0Ah) to the intended phase step.
3. Change mode to PM (Reg 06h[7:5] = 4).
4. Change trigger option to edge or level (Reg 06h[8])
5. Select the trigger source Reg 06h[9] = 1, TRIG (pin-6), or Reg 06h[9] = 0 - trigger from SPI write to Reg 0Eh).

Frequency Sweep Mode

The HMC703LP4E features a built-in sweeper mode, that supports external or automatic triggered sweeps. The maximum sweep range is only limited by the VCO dynamics and range.

Sweeper Mode includes:

a. Automatic 2-Way Sweep Mode
INITIAL trigger, ramp, ramp back, ramp, ramp back, ...
Selected by writing Reg 06h[7:5] = 7

b. Triggered 2-Way Sweep Mode
INITIAL trigger, ramp, wait for trigger, ramp back, wait for trigger, ramp, ...
Selected by writing Reg 06h[7:5] = 6

c. Triggered 1-Way Sweep Mode -
INITIAL trigger, ramp, wait for trigger, hop back to initial frequency, wait for trigger, ramp, ...
Selected by writing Reg 06h[7:5] = 5

Applications include test instrumentation, FMCW sensors, automotive radars and others.

The parameters of the sweep function are illustrated in Figure 31. The HMC703LP4E generates a sweep by implementing miniature frequency steps in time. A smooth and continuous sweep is then generated, at the output of the VCO, after the stepped signal is filtered by the loop filter, as shown in Figure 31. The stepped sweep approach enables the HMC703LP4E to be in lock for entire duration of the sweep. This gives the HMC703LP4E a number of advantages over conventional methods including:

- The ability to generate a linear sweep.
- The ability to have phase coherence between different ramps, so that the phase profile of each sweep is identical.
- The ability to generate sweeps with identical phase and phase noise performance.
- The ability to generate user defined sweeps in single-step ramp mode.

The HMC703LP4E sweep function cycles through a series of discrete frequency values which may be

a. Stepped by an automatic sequencer or,

b. Single stepped by individual triggers in Single Step Mode.

Triggering of each sweep, or step, may be configured to operate:

a. Via a serial port write of 1 to Reg 0Eh[0] (it should then be returned to 0)

b. Automatically generated internally

c. Triggered via TRIG pin-6

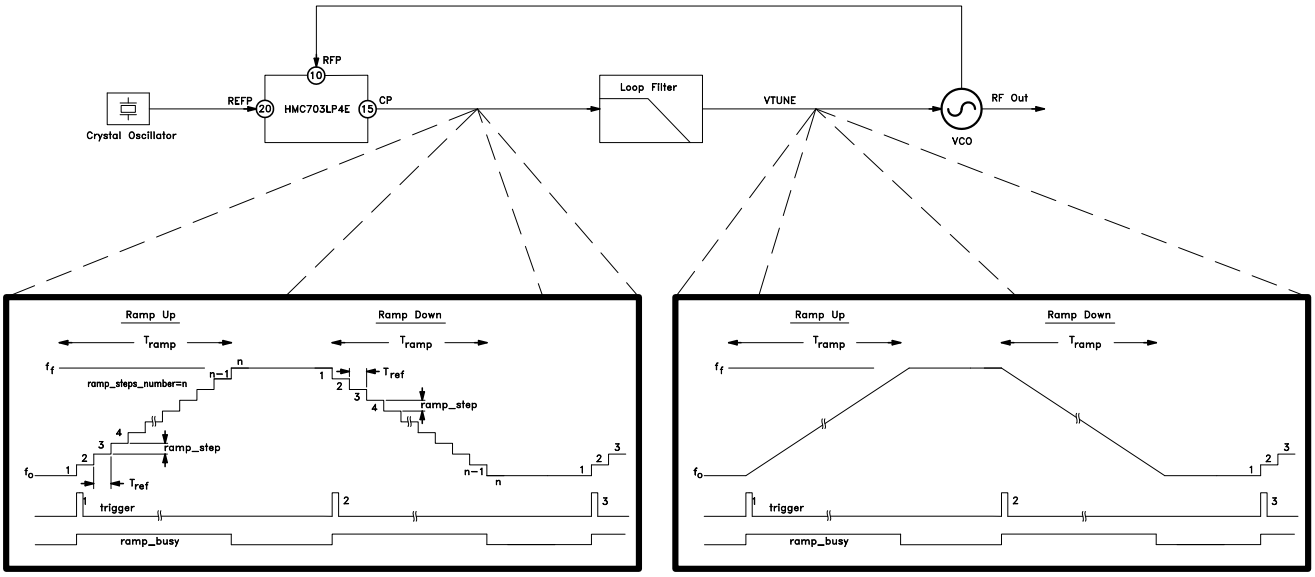

Figure 31. HMC703LP4E Sweep Function

2-Way Sweeps

The HMC703LP4E can be configured to operate in 2-Way Sweep mode by programming Reg 06h [7:5] = 6 or 7. A 2-way sweep is shown in Figure 32. The start of the sweep can be triggered by external TRIG pin-6 if EXTTRIG_EN = 1, or the SPI_TRIG (Reg 0Eh). In automatic 2-Way sweep (Reg 06h [7:5] = 7), the ramp restarts immediately, without waiting for an external trigger.

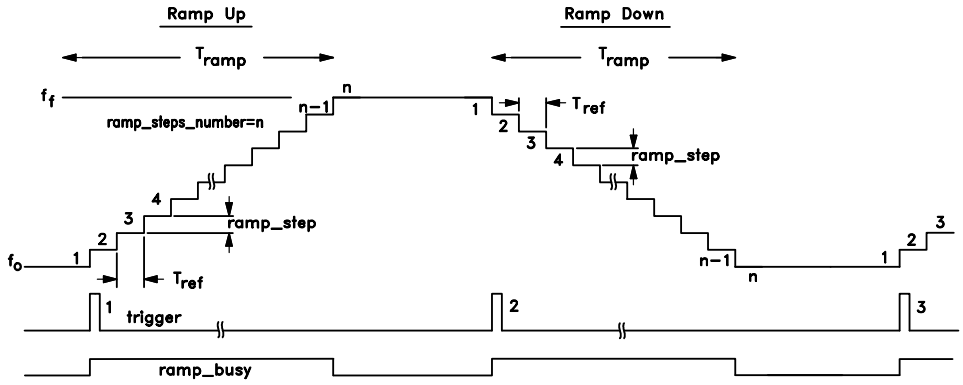

Figure 32. 2-Way Triggered Sweep

1-Way Sweeps

The HMC703LP4E can be configured to operate in Triggered 1-Way Sweep mode by programming Reg 06h [7:5] = 6. Triggered 1-way sweeps are shown in Figure 33. Unlike 2-Way sweeps, Triggered 1-Way sweeps force the VCO to hop back to the start frequency upon the next trigger. Triggered 1-Way sweeps also require a 3rd trigger to start the new sweep. The 3rd trigger should be timed appropriately to allow the VCO to settle after the large frequency hop back to the start frequency. Subsequent odd numbered triggers will start the 1-Way sweep and repeat the process. 1-way sweep can be triggered by external TRIG pin-6 if EXTTRIG_EN = 1, or the SPI_TRIG (Reg 0Eh).

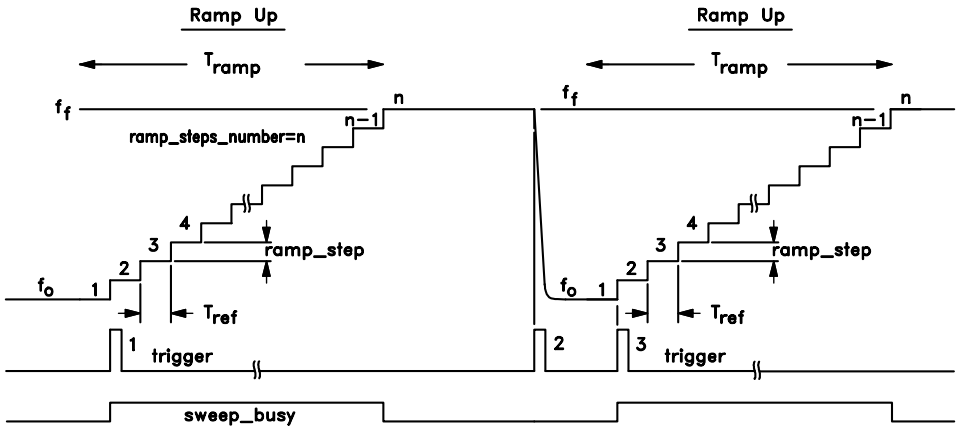

Figure 33. 1-Way Sweep Control

Single Step Ramp Mode

With any of the sweeper profiles, the HMC703LP4E can be configured to operate in single step mode. This causes it to wait for an explicit trigger before every change in the frequency setpoint. A Single Step 1-Way Ramp is shown in Figure 34. In this mode, a trigger is required for each step of the ramp. Similar to autosweep, the ramp_busy flag will go high on the first trigger, and will stay high until the n^{th} trigger. The n+1 trigger will cause the ramp to jump to the start frequency in 1-way ramp mode. The n+2 trigger will restart the 1-way ramp. Single step ramp mode can be triggered by external TRIG pin-6 if EXTTRIG_EN = 1, or the SPI_TRIG (Reg 0Eh).

In single-step mode (Reg 06h[23] = 1), the HMC703LP4E has the capability to generate arbitrarily shaped profiles defined by the timing density of the trigger pulses. On each trigger event the frequency is stepped by the step value programmed in Reg 0Ah. In addition, the HMC703LP4E allows the flexibility to change the step size (Reg 0Ah) during the ramp, between steps, adding another degree of freedom to ramp profile generation. Note that the maximum trigger rate where operation can be guaranteed is $f_{PD}/5$. In addition, the step register (Reg 0Ah) should not be updated via the SPI during the first two reference clock cycles after the trigger. The discrete nature of the frequency updates is smoothed by the loop filter, and should not pose a problem provided that update rate is > 10 x the loop bandwidth.

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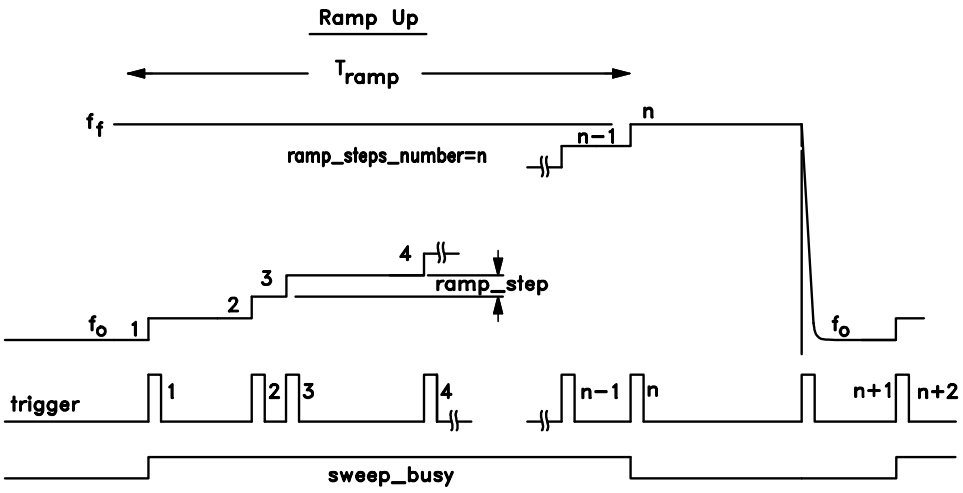

Figure 34. Single Step Ramp Mode

The user should be aware that the synthesized ramp is subject to normal phase locked loop dynamics. If the loop bandwidth in use is much wider than the rate of the steps then the locking will be fast and the ramp will have a staircase shape. If the update rate is higher than the loop bandwidth, as is normally the case, then the loop will not fully settle before a new frequency step is received. Hence the swept output will have a small lag and will sweep in a near continuous fashion.

Detailed Sweeper Configuration

The Following procedure is recommended to configure the frequency sweep in HMC703LP4E:

1. Lock in fractional mode (Reg 06h[7:5] = 0) to the start frequency (f_0).
2. Program frequency step Reg 0Ah and stop N (Reg 0Ch,Reg 0Dh). Note that stop N must be exactly equal to start N plus an integer number of steps (Reg 0Ah). If it is not, the sweeper function will not terminate properly. This normally means rounding the stop N up or down slightly to ensure it falls on a step boundary.
3. Change Mode to Reg 06h[7:5] = 5,6, or 7 - depending on the desired profile.

Note that the ramp step Reg 0Ah is signed two's complement. If negative, the first ramp has a negative slope, and vice-versa.

Setting autoseed (Reg 06h[8] = 1) ensures that different sweeps have identical phase profile. This is achieved by loading the seed (Reg 05h) into the phase accumulator at the beginning of each ramp

Setting Reg 06h[22] = 1 ensures identical phase AND quantization noise performance on each sweep by resetting the entire delta-sigma modulator at the beginning of each ramp.

Note that, while the HMC703LP4E can enforce phase coherence between different frequency sweeps, there will be a phase discontinuity if the start phase that is programmed in SEED (Reg 05h) is different from the phase state that the PLL finds itself in at the end of the ramp. This discontinuity can be prevented by tailoring the sweep profile such that the phase of the PLL at the start of the ramp is equal to phase at the end of the ramp.

Example: Configure a sweep from f_0 = 3000 MHz to f_f = 3105 MHz in Tramp ≈ 2 ms, with f_{PD} = 50 MHz:

1. Start in fractional mode (Program Reg 06h[7:5] = 0)

1. Calculate Start N and Stop N, Program Start N (Reg 03h,Reg 04h)

Start N = 3000.0 MHz / 50.0 MHz = 60.0

Stop N = 3105.0 MHz / 50.0 MHz = 62.1

Program Reg 03h = 60, Reg 04h = 0

2. Calculate how many reference cycles will occur in 2 ms. Given that Tref = 1 / f_{PD} = 20ns,

Nbr of Steps = Tramp/Tref = 2ms/20ns = 100,000

3. Calculate the desired N step size, given Start N, Stop N and Nbr of Steps

N_Step_Size_desired = (62.1 - 60.0) / 100,000 = 21u [fractions of N]

4. Quantize the fractional N step into the 24 bit step size

Program Reg 0Ah = 21u x 2^{24} = round(352.32) = 352

5. Readjust the stop frequency slightly to ensure it falls exactly on a step boundary

Due to step quantization,there will be some finite error in either the sweep time or sweep span.

We have 3 choices:

a) Target an accurate sweep time, sacrifice resolution on stop frequency

Sweep time = 100k cycles = 2 ms

Stop N = Start N + 100,000 x 352/2^{24} (Keep 100k cycles)

Stop N = 60.000 + 35,200,000 / 2^{24} ≈ 62.09808

Program Reg 0Ch= 62, Reg 0Dh = 35,200,000 MOD 2^{24} = 1,645,568 ≈ 0.09808

f_f ≈ 3104.904 (96 kHz lower stop frequency then desired)

b) Target an accurate stop frequency, at the expense of sweep time accuracy

Given step size of 352/2^{24}, how many cycles to get from 60.0 to 62.1

Nbr of Steps = (62.1 - 60.0) / (352/2^{24}) = 100,091.345

Must round to 100,091 steps.

*Sweep time = Tref * 100,091 = 2.00182ms (1.82 us longer than desired)*

Stop N = 60.0 + 100,091 x 352/2^{24} ≈ 62.0999927

Program Reg 0Ch= 62, Reg 0Dh = 35,232,032 MOD 2^{24} = 1,677,600 ≈ 0.0999927

f_f = 3104.99964 MHz (362 Hz lower stop frequency then desired)

c) A combination of situation a and b

6. Program SD_Mode based on desired trigger and ramp/hop profile (Reg 06h[7:5] = 5,6, or 7)

7. Trigger via either the external pin or SPI TRIG bit.

Continue to issue triggers to advance the ramp profile to the next stage...

Sweeper Configuration for Ultra Fine Step Sizes

In cases where finer step size resolution is desired, it is possible to reduce the f_{PD}, along with performance implications it has, or use a single-step mode (Reg 06h[23] = 1) and provide a lower frequency clock on the external trigger pin to reduce the update rate. The HMC703LP4E can generate a lower frequency clock by programming the R divider appropriately, and not using it for the PD (Reg 06h[21] = 1), but rather routing it out of the HMC703LP4E via the GPO. The R divider output can then be looped back to the TRIG pin of the HMC703LP4E to use as a low rate trigger. See "Ref Path 'R' Divider" for more details.

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Reference Input Stage

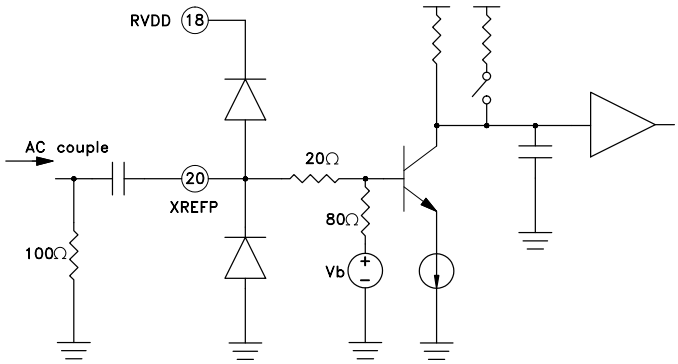

Figure 35. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation. High Gain (recommended below 200 MHz), and High frequency, for 200 to 350 MHz operation. The buffer is internally DC biased, with 100 Ω internal termination. For 50 Ω match, an external 100 Ω resistance to AC ground should be added, followed by an AC coupling capacitance (impedance < 1 Ohm), then to the XREFP pin of the part.

At low frequencies, a relatively square reference is recommended to keep the input slew rate high. At higher frequencies, a square or sinusoid can be used. The following table shows the recommended operating regions for different reference frequencies. If operating outside these regions the part will normally still operate, but with degraded performance.

Minimum pulse width at the reference buffer input is 2.5 ns. For best spur performance when R = 1, the pulse width should be > (2.5 ns + 8 Tps), where Tps is the period of the VCO at the prescaler input. When R > 1 minimum pulse width is 2.5 ns.

Table 7. Reference Sensitivity Table

	Square Input			Sinusoidal Input		
Frequency (MHz)	Slew > 0.5V/ns	Recommended Swing (Vpp)			Recommended Power Range (dBm)	
	Recommended	Min	Max	Recommended	Min	Max
< 10	YES	0.6	2.5	x	x	x
10	YES	0.6	2.5	x	x	x
25	YES	0.6	2.5	ok	8	15
50	YES	0.6	2.5	YES	6	15
100	YES	0.6	2.5	YES	5	15
150	ok	0.9	2.5	YES	4	12
200	ok	1.2	2.5	YES	3	8
200 to 350	x	x	x	YES[1]	5	10
Note: For greater than 200 MHz operation, use buffer in High Frequency Mode. Reg 08h[18] = 1						

Input referred phase noise of the PLL when operating at 50 MHz is between -150 and -156 dBc/Hz at 10 kHz offset depending upon the mode of operation. The input reference signal should be 10dB better than this floor to avoid degradation of the PLL noise contribution. It should be noted that such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

Ref Path 'R' Divider

The reference path "R" divider is based on a 14 bit counter and can divide input signals of up to 350 MHz input by values from 1 to 16,383 and is controlled by Reg 02h[13:0]. The reference divider output may be viewed in test mode on the LD_SDO pin, by setting Reg 0Fh[4:0] = 9d.

The HMC703LP4E can use the undivided reference, while exporting a divided version for auxiliary purposes (eg. ramp triggers, FPGAs etc.) on the GPO, if Reg 06h[21] = 1.

RF Path

The RF path is shown in Figure 36. This path features a low noise 8 GHz RF input buffer followed by an 8 GHz RF divide-by-2 with a selectable bypass. If the VCO input is below 4 GHz the RF divide-by-2 should be by-passed for improved performance in fractional mode. The RF divide-by-2 is followed by the N divider, a 16 bit divider that can operate in either integer or fractional mode with up to 4 GHz inputs. Finally the N divider is followed by the Phase Detector (PD), which has two inputs, the RF path from the VCO (V) and the reference path (R) from the crystal. The PD can operate at speeds up to 100 MHz in fractional Mode B (recommended), 80 MHz in fractional Mode A and 115 MHz in integer mode.

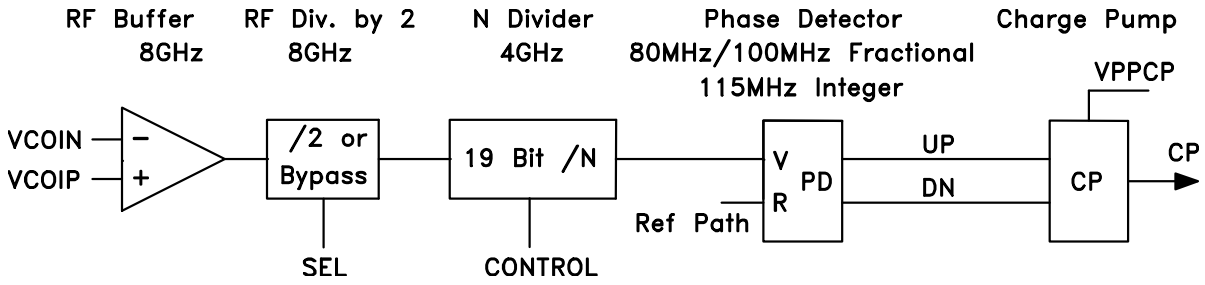

Figure 36. RF Path

RF Input Stage

The RF input stage provides the path from the external VCO to the phase detector via the RF or 'N' divider. The RF input path is rated to operate up to 8 GHz across all conditions. The RF input stage is a differential common emitter stage with internal DC bias, and is protected by ESD diodes as shown in Figure 37. This input is not matched to 50 Ω. A 100 Ω resistor placed across the inputs can be used for a better match to 50 Ω. In most applications the input is used single-ended into either the VCOIP or VCOIN pin with the other input connected to ground through a DC blocking capacitor. The preferred input level for best spectral performance is -10 dBm nominally.

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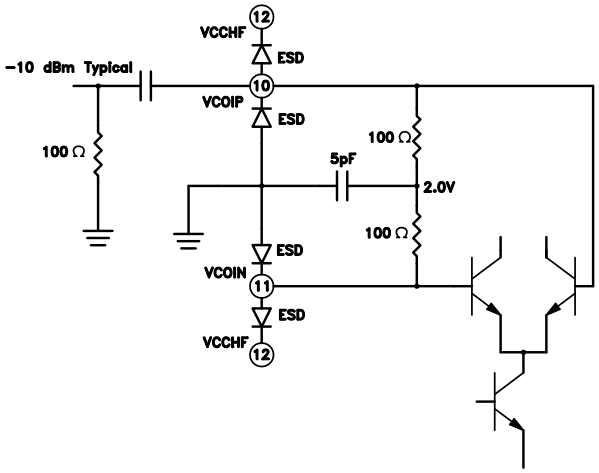

Figure 37. RF Input Stage- shown with single ended device

RF Path 'N' Divider

The main RF path 'N' divider is capable of divide ratios anywhere between 2^{16}-1 (524,287) and 16 . This divider for example could divide a 4 GHz input to a PD frequency anywhere between its maximum output limit of 115 MHz to as low as 7.6 kHz. The 'N' divider output may be viewed in test mode on LD_SDO by setting Reg 0Fh[4:0] = 10d. When operating in fractional mode the N divider can change by up to +/-4 from the average value. Hence the selected divide ratio in fractional mode is restricted to values between 2^{16}-5 (65,531) and 20.

If the VCO input is above 4 GHz then the 8 GHz fixed RF divide-by-2 should be used, Reg 08h[17] = 1. In this case the integer division range is restricted to even numbers over the range 2*(2^{16}-5) (131,062) down to 40.

PLL Jitter

The standard deviation of the arrival time of the VCO signal, or the jitter, may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi^2(f_0)$, at offsets less than the loop 3dB bandwidth and a 20dB per decade roll off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 38.

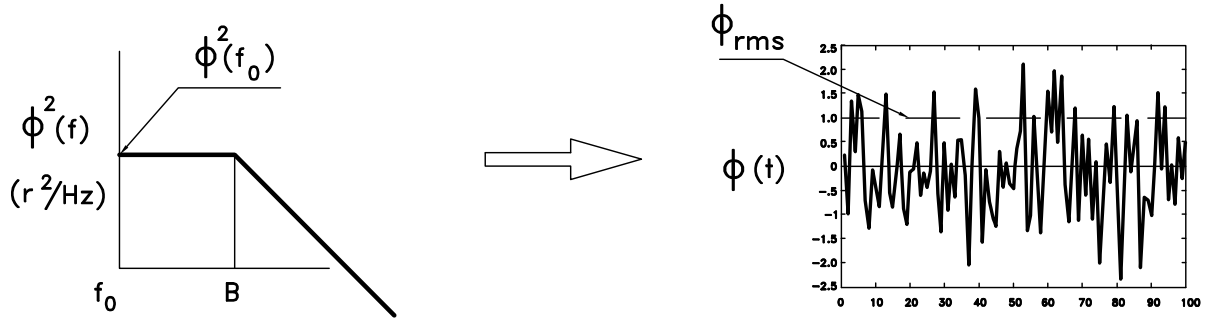

Figure 38. PLL Phase Noise and Jitter

With this simplification the total integrated VCO phase noise, Φ^2_v, in rads^2 is given by

$$\Phi^2_v = \Phi^2(f_0)\, B\pi \qquad \textit{(EQ 10)}$$

where
Φ^2 is the single sideband phase noise in rads^2/Hz inside the loop bandwidth, and
B is the 3 dB corner frequency of the closed loop PLL

The integrated phase noise at the phase detector, Φ^2_{pd}, is just scaled by N^2 ie. $\Phi^2_{pd} = \Phi^2_v/N^2$

The rms phase jitter of the VCO (Φ_v) in rads, is just the square root of the phase noise integral.

Since the simple integral of (EQ 10) is just a product of constants, we can easily do the integral in the log domain. For example if the phase noise inside the loop is -110 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio is 100, then the integrated phase noise at the phase detector, in dB, is given by;

$\Phi^2_{pd} = 10\log(\Phi^2(f_0)\, B\pi/N^2) = -110 + 5 + 50 - 40 = -95$ dBrads, or equivalently $\Phi = 10^{-95/20}$ = 18 µrads = 1 milli-degrees rms.

While the phase noise reduces by a factor of 20logN after division to the reference, due to the increased period of the PD reference signal, the jitter is constant.

The rms jitter from the phase noise is then given by $T_{jpn}=T_{pd}\,\Phi^2_{pd}/2\pi$

In this example if the PD reference was 50 MHz, T_{pd} = 20 nsec, and hence T_{jpn} = 56 femto-sec.

Charge Pump and Phase Detector

The Phase Detector or PD has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PD as f_{pd}. Most formula related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PD, f_{pd} is sometimes referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies in a linear fashion over nearly ±2π radians (±360) of input phase difference.

Charge Pump and Phase Detector Functions

Phase detector register Reg 0Bh allows manual access to control special phase detector features.

Reg 0Bh[2:0] allows fine tuning of the PD reset path delay. This adjustment can be used to improve performance at very high PD rates. Most often this register is set to the recommended value only.

Reg 0Bh[5] and [6] enables the PD UP and DN outputs respectively. Disabling prevents the charge pump from pumping up or down respectively and effectively tri-states the charge pump while leaving all other functions operating internally.

CP Force UP Reg 0Bh[7] and CP Force DN Reg 0Bh[8] allows the charge pump to be forced up or down respectively. This will force the VCO to the ends of the tuning range which can be useful for testing of the VCO.

PD Force Mid Reg 0Bh[9] will disable the charge pump current sources and place a voltage source on the loop filter at approximately VPPCP/2. If a passive filter is used this will set the VCO to the mid-voltage tuning point which can be useful for testing of the VCO.

Lock Detect

Each PD (Phase Detector) cycle, the HMC703LP4E measures phase error at the PD. The measured phase error must be:

- < ~220 degrees if 40 MHz <= f_{PD} <= 120 MHz, and
- < ~14 ns if f_{pd} < 40 MHz,

for a number of consecutive cycles (number of cycles is programmable in Reg 07h[2:0]), in order for HMC703LP4E to declare a lock. A single phase error outside of these criteria disqualifies lock, and the lock counter (maximum value of lock counter = Reg 07h[2:0]) is restarted.

Note that in some cases, the PLL may be locked with a phase error that exceeds 180 degrees, or 12 ns, whichever is smaller. This can occur if the offset current is inappropriately programmed too high. It is not recommended to operate in this condition because it leads to degraded phase noise performance. In such a case the lock detect circuit would not declare a locked condition, even though the PLL is locked.

The HMC703LP4E lock-detect functionality is self-calibrating relative to the reference frequency. Typically the lock-detect training is only required once on power-up, or each time the reference frequency or the R divider value (Reg 02h) is changed.

To train the lock-detect circuitry of the HMC703LP4E on power-up, set:

- set Reg 07h [11] = 1 to enable lock-detect counters
- set Reg 07h [14] = 1 to enable the lock-detect timer
- set Reg 07h [20] = 1 to train the lock-detect timer

These bits can all be written simultaneously.

On any change of the PD frequency (via either the external reference frequency, or the R divider setting (Reg 02h)), the lock-detect circuit should be retrained by toggling Reg 07h [20] Off and then back On.

The lock-detect indication can be read from the SPI via Reg 12h[1], or can be exported on the LD_SDO pin via the GPO mux(Reg 0Fh[4:0]). See LD_SDO pin description for more information.

Cycle Slip Prevention (CSP)

When changing frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than +/-2π radians. Since the gain of the PD varies linearly with phase up to +/-2π, the gain of a conventional PD will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than 0 radians. The output current from the charge pump will cycle from maximum to minimum even though the VCO has not yet reached its final frequency.

The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomenon is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle Slipping increases the time to lock to a value much greater than that predicted by normal small signal Laplace analysis.

The HMC703LP4E mitigates the effects of cycle-slips by increasing the charge-pump current when the phase error is larger than ~220 degrees or ~14 ns (whichever is less as measured by the lock-detect circuit). The circuit is normally most effective for PD frequencies <= 50 MHz.

PD Polarity

Reg 0Bh[4]=0 sets the PD polarity for use with a passive loop filter together with a VCO with a positive tuning slope (increasing tuning voltage increases VCO frequency).

Reg 0Bh[4]=1 inverts the PD polarity. This is most often used if an inverting op-amp is used in an active loop filter together with a VCO with a positive tuning slope.

Charge Pump Tri-state

Reg 0Bh[5]=Reg 0Bh[6]=0 tri-states the charge pump. This effectively freezes charge on the loop filter and allows the VCO to run open loop, provided that CP offset is also disabled.

Charge Pump Gain

Reg 09h[6:0] and Reg 09h[13:7] program current gain settings for the charge pump. Pump ranges can be set from 0 µA to 2.54 mA in 20uA steps. Charge pump gain affects the loop bandwidth. The product of VCO gain (K_{vco}) and charge pump gain (K_{cp}) can be held constant for VCO's that have a wide ranging K_{vco} by adjusting the charge pump gain. This compensation helps to keep the loop bandwidth constant.

In addition to the normal CP current as described above, there is also an extra output source of current that offers improved noise performance. HiK_{cp} provides an output current that is proportional to the loop filter voltage. This being the case, HiK_{cp} should only be operated with active op-amp loop filters that define the voltage as seen by the charge pump pin. With 2.5 V as observed at the charge pump pin, the HiK_{cp} current is 3.5 mA.

There are several configurations that could be used with the HiK_{cp} feature. For lowest noise, HiK_{cp} could be used without the normal charge pump current (the charge pump current would be set to 0). In this case, the loop filter would be designed with 3.5 mA as the effective charge pump current.

Another possible configuration is to operate with both the HiK_{cp} and normal charge pump current sources. In this case the effective charge pump current would be 3.5mA + programmed normal charge pump current which could offer a maximum of 6 mA.

With passive loop filters the voltage seen by the charge pump pin will vary which would cause the HiK_{cp} current to vary widely. As such, HiK_{cp} should not be used on passive loop filter implementations.

A simplified diagram of the charge pump is shown in Figure 39. The current gain of the pump in Amps/radian is equal to the gain setting of this register divided by 2π.

Charge Pump Offset

Reg 09h[20:14] controls the charge pump current offsets. Reg 09h[21] and Reg 09h[22] enable the UP and DN offset currents respectively. Normally, only one is used at a time. As mentioned earlier charge pump offsets affect fractional mode linearity . Offset polarity should be chosen such that the divided VCO lags the reference signal. This means down for non-inverting loop filters.

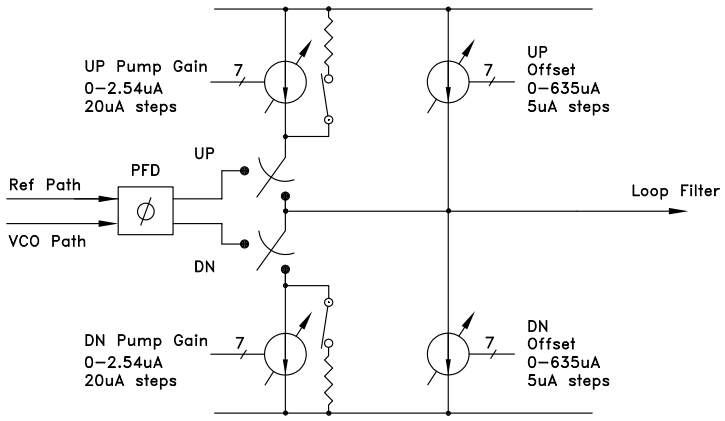

Figure 39. Charge Pump Gain and Offset Control - Reg09h

Seed Register and AutoSeed Mode

The start phase of the fractional modulator digital phase accumulator (DPA) may be set to any values via the seed register Reg 05h. If autoseed Reg 06h[8] is set, then the PLL will automatically reload the start phase from Reg 05h[23:0] into the DPA every time a new fractional frequency is selected. If autoseed is not set, then the PLL will start new fractional frequencies with the value left in the DPA from the last frequency. Hence the start phase will effectively be random. Certain zero or binary seed values may cause spurious energy correlation at specific frequencies. Correlated spurs are advantageous only in very special cases where the spurious are known to be far out of band and are removed in the loop filter. For most cases a pseudo-random seed setting is recommended. Further, since the autoseed always starts the accumulators at the same place, performance is repeatable if autoseed is used. Reg 05h's default value typically provides good performance.

Power on Reset

The HMC703LP4E features a hardware Power on Reset (POR) on the digital supply DVDD. All chip registers will be reset to default states approximately 250 µs after power up of DVDD. Once the supply is fully up, if the power supply then drops below 0.5 V the digital portion will reset. Note that the SPI control inputs must also be 0 at power-down, otherwise they will inadvertently power the chip via the ESD protection network.

Power Down Mode

Hardware Power Down

Chip enable may be controlled from the hardware CEN pin 23, or it may be controlled from the serial port. Reg 01h[0] =1 assigns control to the CEN pin. Reg 01h[0] =0 assigns control to the serial port Reg 01h[1]. For hardware test reasons or some special applications it is possible to force certain blocks to remain on inside the chip , even if the chip is disabled. See the register Reg 01h description for more details.

Chip Identification

Version information may be read from the synthesizer by reading the content of chip_ID in Reg 00h.

General Purpose Output (GPO) Pin

The PLL shares the LD_SDO (Lock-Detect/Serial Data Out) pin to perform various functions. While the pin is most commonly used to read back registers from chip via the SPI, it is also capable of exporting a variety of interesting signals and real time test waveforms (including Lock Detect). It is driven by a tri-state CMOS driver with ~200 Ω Rout. It has logic associated with it to dynamically select whether the driver is enabled, and to decide which data to export from the chip.

In its default configuration, after power-on-reset, the output driver is disabled, and only drives during appropriately addressed SPI reads. This allows it to share the output with other devices on the same bus.

Depending on the SPI mode, the read section of SPI cycle is recognized differently

HMC SPI Mode: The driver is enabled during the last 24 bits of SPI READ cycle (not during write cycles).

Open SPI Mode: The driver is enabled if the chip is addressed - ie. The last 3 bits of SPI cycle = '000'b before the rising edge of SEN (Note A).

To consistently monitor any of the GPO signals, including Lock Detect, set Reg 0Fh[7] = 1 to keep the SDO driver always on. This stops the LDO driver from tri-stating and means that the SDO line cannot be shared with other devices.

The chip will naturally switch away from the GPO data and export the SDO during an SPI read (Note B). To prevent this automatic data selection, and always select the GPO signal, set "Prevent AutoMux of SDO" (Reg 0Fh[6] = 1). The phase noise performance at this output is poor and uncharacterized. Also, the GPO output should not be toggling during normal operation. Otherwise the spectral performance may degrade.

Note that there are additional controls available, which may be helpful if sharing the bus with other devices:

- To allow the driver to be active (subject to the conditions above) even when the chip is disabled - set Reg 01h[7] = 0.
- To disable the driver completely, set Reg 08h[5] = 0 (it takes precedence over all else).
- To disable either the pull-up or pull-down sections of the driver, Reg 0Fh[8] = 0 or Reg 0Fh[9] = 0 respectively.

Note A: If SEN rises before SCK has clocked in an 'invalid' (non-zero) chip -address, the part will start to drive the bus.

Note B: In Open Mode, the active portion of the read is defined between the 1st SCK rising edge after SEN, to the next rising edge of SEN.

Example Scenarios:

- Drive SDO during reads, tri-state otherwise (to allow bus-sharing)
  - No action required.
- Drive SDO during reads, Lock Detect otherwise
  - Set GPO Select Reg 0Fh[4:0] = '00001' (which is default)
  - Set "Prevent GPO driver disable" (Reg 0Fh[7] = 1)
- Always drive Lock Detect
  - Set " Prevent AutoMux of SDO" Reg 0Fh[6] = 1
  - Set GPO Select Reg 0Fh[4:0]= 00001 (which is default)
  - Set "Prevent GPO driver disable" (Reg 0Fh[7] = 1))

The signals available on the GPO are selected by changing "GPO Select", Reg 0Fh[4:0].

VCO Tuning

Passive Filter

The HMC703LP4E is targeted for high performance applications with an external VCO. The synthesizer charge pump has been designed to work directly with VCOs that can be tuned nominally over 1.0 to 4.0 Volts on the varactor tuning port with a +5 V charge pump supply voltage. Slightly wider ranges are possible with a +5.2 V charge pump supply or with slightly degraded performance. Hittite PLL Design software is available to design passive loop filters driven directly from the PLL charge pump.

High Voltage Tuning, Active Filter

Optionally an external op-amp may be used in the loop filter to support VCOs requiring higher voltage tuning ranges. Loop filter design is highly application specific, and can have significant impact on the PLL performance. Its impact on PLL performance should be well characterized, and optimized for best PLL performance. Hittite's PLL Design software is available to design active loop filters with external op-amps. Various filter configurations are supported.

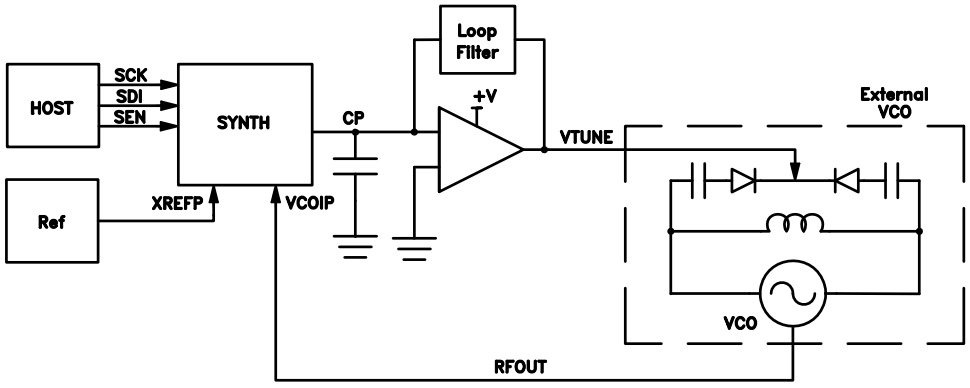

Figure 40. Synthesizer with Active Loop Filter and Conventional External VCO

MAIN SERIAL PORT

Serial Port Modes of Operation

The HMC PLL-VCO serial port interface can operate in two different modes of operation.

a. HMC Mode (HMC Legacy Mode) - Single slave per HMCSPI Bus.

b. Open Mode - Up to 8 slaves per HMCSPI Bus. The HMC703LP4E only uses 5 bits of address space.

Both protocols support 5 bits of register address space. HMC Mode can support up to 6 bits of register address but, is restricted to 5 bits when compatibility with Open Mode is offered.

Register 0 Modes

Register 0 has a dedicated function in each mode. Open Mode allows wider compatibility with other manufacturers SPI protocols.

Table 8. Register 0 Comparison - Single vs Multi-User Modes

	Single User HMC Mode	Single Or Multi-User Open Mode
READ	Chip ID 24 Bits	Chip ID 24Bits
WRITE	Soft Reset, General Strobes	Read Address [4:0] Soft reset [5] General Strobes [24:6]

Serial Port Mode Decision after Power-On Reset

On power up, both types of modes are active and listening. All digital IO must be low at power-up.

A decision to select the desired Serial Port mode (protocol) is made on the first occurrence of SEN or SCK , after which the Serial Port mode is fixed and only changeable by a power down.

a. If a rising edge on SEN is detected first HMC Mode is selected.

b. If a rising edge on SCK is detected first Open mode is selected.

Serial Port HMC Mode - Single PLL

HMC Mode (Legacy Mode) serial port operation can only address and communicate with a single PLL, and is compatible with most HMC PLLs and PLLs with integrated VCOs.

The HMC Mode protocol for the serial port is designed for a 4 wire interface with a fixed protocol featuring

a. 1 Read/Write bit

b. 6 Address bits

c. 24 data bits

Serial Port Open Mode

The Serial Port Open Mode features:

a. Compatibility with general serial port protocols that use a shift and strobe approach to communication.

b. Compatible with HMC multi-Chip solutions, useful to address multiple chips of various types from a single serial port bus.

The HMC Open Mode protocol has the following general features:

a. 3 bit chip address, can address up to 8 devices connected to the serial bus (= 000 on HMC703LP4E)

b. Wide compatibility with multiple protocols from multiple vendors

c. Simultaneous Write/Read during the SPI cycle

d. 5 bit register address space

e. 3 wire for Write Only capability, 4 wire for Read/Write capability.

HMC RF PLLs with integrated VCOs also support HMC Open Mode. HMC700, HMC701, HMC702 and some generations of microwave PLLs with integrated VCOs do not support Open Mode.

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Typical HMC Open Mode serial port operation can be run with SCK at speeds up to 50 MHz.

Serial Port HMC Mode Details

Typical serial port HMC Mode operation can be run with SCK at speeds up to 50MHz.

HMC Mode - Serial Port WRITE Operation

AVDD = DVDD = 3.3V +/-10%, AGND = DGND = 0V

Table 9. SPI HMC Mode - Write Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_1	SEN to SCK setup time	8			nsec
t2	SDI to SCK setup time	3			nsec
t3	SCK to SDI hold time	3			nsec
t4	SEN low duration	20			nsec
t5	SCK to SEN fall	10			nsec
	Max SPI Clock Frequency		50		MHz

A typical HMC Mode WRITE cycle is shown in Figure 41.

- **a.** The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
- **b.** The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low indicates a Write cycle (/WR).
- **c.** Host places the six address bits on the next six falling edges of SCK, MSB first.
- **d.** Slave shifts the address bits in the next six rising edges of SCK (2-7).
- **e.** Host places the 24 data bits on the next 24 falling edges of SCK, MSB first.
- **f.** Slave shifts the data bits on the next 24 rising edges of SCK (8-31).
- **g.** The data is registered into the chip on the 32nd rising edge of SCK.
- **h.** SEN is cleared after a minimum delay of t_5. This completes the write cycle.

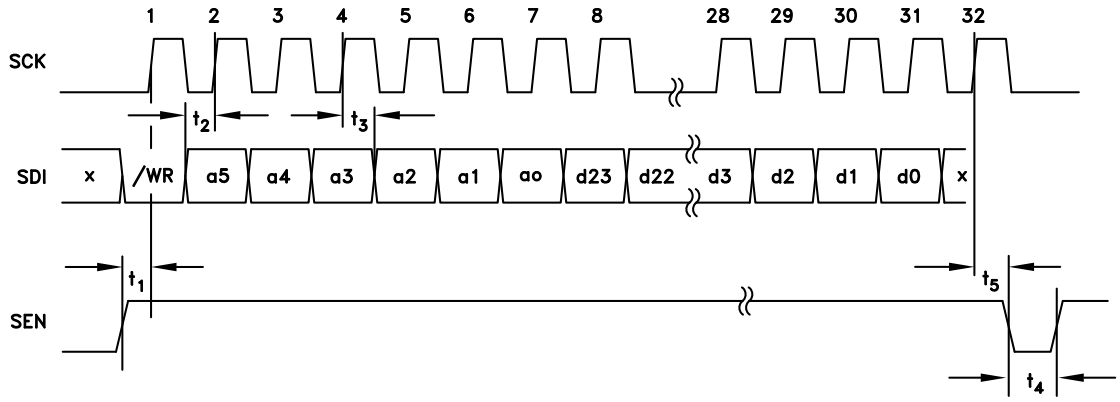

Figure 41. Serial Port Timing Diagram - HMC Mode WRITE

HMC Mode - Serial Port READ Operation

A typical HMC Mode READ cycle is shown in Figure 42.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCK. Note: The Lock Detect (LD) function is usually multiplexed onto the LD_SDO pin. It is suggested that LD only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in Figure 42.

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI high initiates the READ cycle (RD)

c. Host places the six address bits on the next six falling edges of SCK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCK (2-7).

e. Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. Slave restores Lock Detect on the 32nd rising edge of SCK.

h. SEN is cleared after a minimum delay of t_6. This completes the cycle.

Table 10. SPI HMC Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_1	SEN to SCK setup time	8			ns
t2	SDI setup to SCK time	3			ns
t3	SCK to SDI hold time	3			ns
t4	SEN low duration	20			ns
t5	SCK to SDO delay		8.2ns+0.2ns/pF		ns
t6	SCK to SEN fall	10			ns

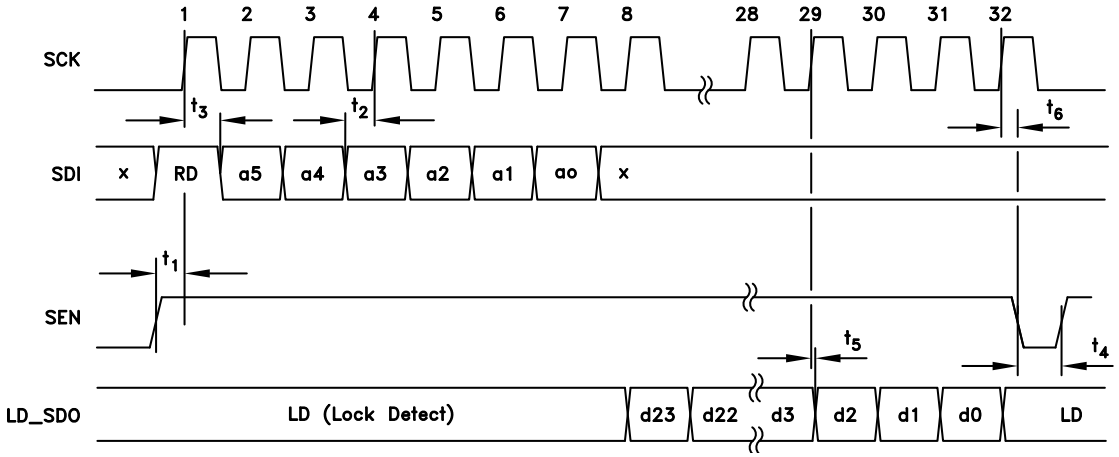

Figure 42. HMC Mode Serial Port Timing Diagram - READ

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Serial Port Open Mode Details

Open Mode - Serial Port WRITE Operation

Table 11. SPI Open Mode - Write Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_1	SDI setup time	3			ns
t2	SDI hold time	3			ns
t3	SEN low duration	10			ns
t4	SEN high duration	10			ns
t5	SCK 32 Rising Edge to SEN Rising Edge	10			ns
	Serial port Clock Speed	DC	50		MHz
t_6	SEN to SCK Recovery Time	10			ns

A typical WRITE cycle is shown in Figure 43.

- **a.** The Master (host) places 24 bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCK.
- **b.** the slave (synthesizer) shifts in data on SDI on the first 24 rising edges of SCK
- **c.** Master places 5 bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCK (25-29)
- **d.** Slave shifts the register bits on the next 5 rising edges of SCK (25-29).
- **e.** Master places 3 bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCK (30-32). The HMC703LP4E chip address is fixed at 000.
- **f.** Slave shifts the chip address bits on the next 3 rising edges of SCK (30-32).
- **g.** Master asserts SEN after the 32nd rising edge of SCK.
- **h.** Slave registers the SDI data on the rising edge of SEN.

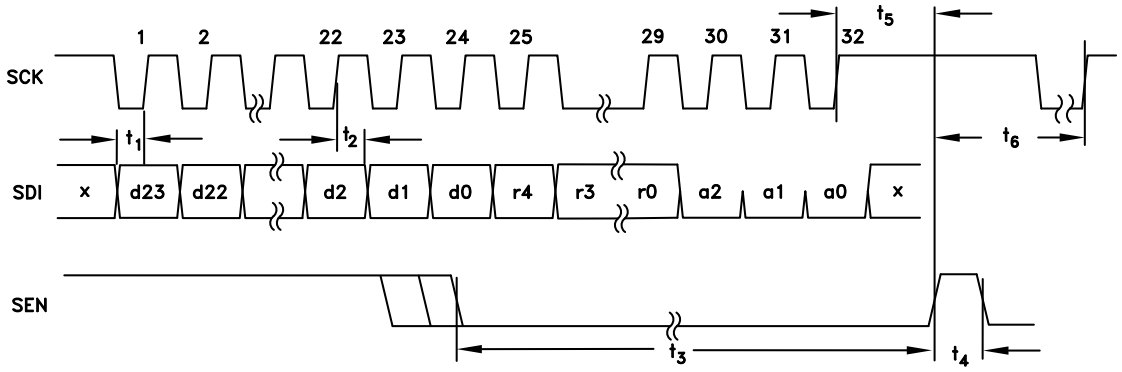

Figure 43. Open Mode - Serial Port Timing Diagram - WRITE

Open Mode - Serial Port READ Operation

A typical READ cycle is shown in Figure 44.

In general, in Open Mode the LD_SDO line is always active during the WRITE cycle. During any Open Mode SPI cycle LD_SDO will contain the data from the address pointed to by Reg 00h[4:0]. If Reg 00h[4:0] is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress. If it is desired to READ from a spe-

cific address, it is necessary in the first SPI cycle to write the desired address to Reg 00h[4:0], then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the Open Mode two cycle procedure to read from any random address is as follows:

- **a.** The Master (host), on the first 24 falling edges of SCK places 24 bit data, d23:d0, MSB first, on SDI as shown in Figure 44. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on the next cycle.
- **b.** the slave (synthesizer) shifts in data on SDI on the first 24 rising edges of SCK
- **c.** Master places 5 bit register address , r4:r0, (the address the WRITE ADDRESS register), MSB first, on the next 5 falling edges of SCK (25-29). r4:r0=00000.
- **d.** Slave shifts the register bits on the next 5 rising edges of SCK (25-29).
- **e.** Master places 3 bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCK (30-32).The HMC703LP4E chip address is fixed at 000.
- **f.** Slave shifts the chip address bits on the next 3 rising edges of SCK (30-32).
- **g.** Master asserts SEN after the 32nd rising edge of SCK.
- **h.** Slave registers the SDI data on the rising edge of SEN.
- **i.** Master clears SEN to complete the address transfer of the two part READ cycle.
- **j.** If we do not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.
- **k.** Master places the same SDI data as the previous cycle on the next 32 falling edges of SCK.
- **l.** Slave (synthesizer) shifts the SDI data on the next 32 rising edges of SCK.
- **m.** Slave places the desired data (i.e. data from address in Reg 00h[4:0]) on LD_SDO on the next 32 rising edges of SCK. Lock Detect is disabled.
- **n.** Master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to Lock Detect on LD_SDO.

Note that if the chip address bits are unrecognized (a2:a0), the slave will tri-state the LD_SDO output to prevent a possible bus contention issue.

Table 12. SPI Open Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_1	SDI setup time	3			ns
t2	SDI hold time	3			ns
t3	SEN low duration	10			ns
t4	SEN high duration	10			ns
t5	SCK Rising Edge to SDO time		8.2+0.2ns/pF		ns
t6	SEN to SCK Recovery Time	10			ns
t7	SCK 32 Rising Edge to SEN Rising Edge	10			ns

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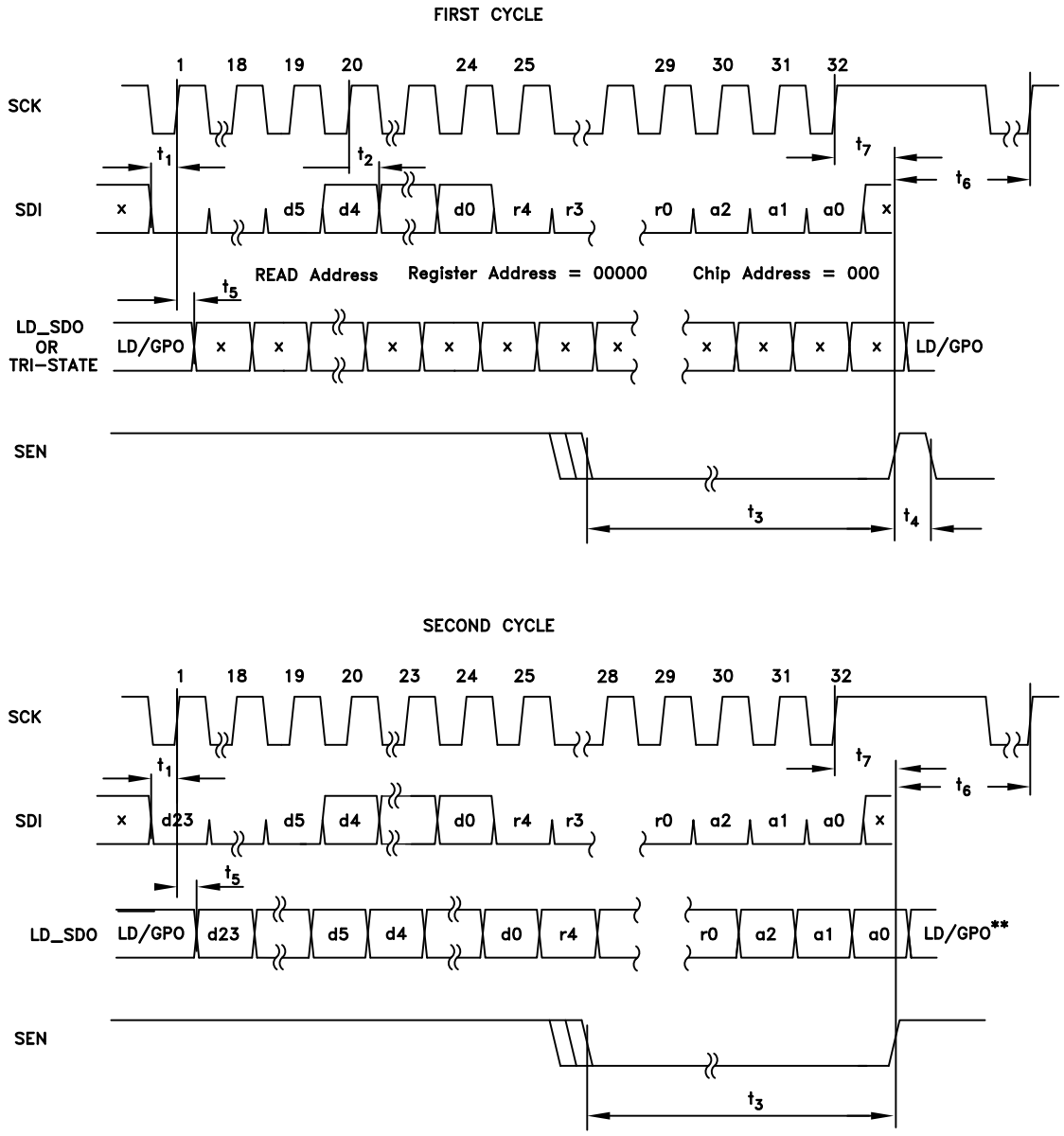

**Note: Read-back on LD_SDO can function without SEN, Hoewer SEN rising edge is required to return the LD_SDO to the GPO state

Figure 44. Open Mode - Serial Port Timing Diagram - READ Operation 2-Cycles

REGISTER MAP

Table 13. Reg 00h ID Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	RO	chip_ID	24	97370h	PLL ID

Table 13. Reg 00h Open Mode Read Address/RST Strobe Register (Write Only) (Continued)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[4:0]	WO	ReadAddr	5	0	Write the intended read address to this register for Open Mode register reads. On the 1st SPI clock of the next cycle the data is read and the shift-out begins.

Table 13. Reg 00h Open Mode Read Address Register (Write Only) (Continued)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
5	WO	SoftRst	1	0	Soft-reset. When 1, it Resets the registers to POR state, and issues POR to analog.

Table 14. Reg 01h RST Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
0	R/W	EnPinSel	0	0	If 1, the master chip enable is taken from the pin rather than from the SPI.
1	R/W	EnFromSPI	1	1	The master Enable from the SPI. Write a 0 to power-down the chip.
[9:2]	R/W	EnKeepOns	8	0	While the chip is disabled, the user has the option to keep the following sub-circuits active by writing a 1 to the appropriate bits. [2] Bias, [3] PFD, [4] CHP, [5] RefBuf, [6] VCOBuf, [7] GPO, [8] VCODIVA, [9] VCODIVB
10	R/W	EnSyncChpDis	1	0	If 1, then following a disable event, the charge-pump is disabled synchronously on the falling edge of the divided reference to tri-state the charge pump without transient.

Table 15. Reg 02h REFDIV Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[13:0]	R/W	rdiv	14	1	Reference Divider 'R' Value Divider use also requires refBufEn Reg08[3]=1 min 1d max 16383d

Table 16. Reg 03h Frequency Register - Integer Part

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[15:0]	R/W	intg	16	25d	The (base) integer portion of the prescaler divide ratio. In any of the fractional modes of operation, this value is double buffered, and does not take effect until a 'Trigger' event. See 'Operation Modes' for more information. In integer mode, this value can range from 16 to 65535. In fractional mode it should be restricted between 20 and 65531.

Table 17. Reg 04h Frequency Register - Fractional Part

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	frac	24	0	VCO Divider Fractional part (24 bit unsigned) see Fractional Frequency Tuning N_{FRAC} = Reg 04h/2^{24} Used in Fractional Modes only min 0d max 2^24-1 = FFFFFFh = 16,777,215d

Table 18. Reg 05h Seed

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	SEED	24	654321h	The initial starting point for the fractional modulator at the "Trigger" position. This value effects the phase of the output, and can effect some types of spurious content. During sweeps, the modulator can optionally be reloaded with this value at the start of each ramp.

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Table 19. Reg 06h SD CFG Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	Modulator Type	1	1	Modulator Type A (1) or Type B(0) Type B is easier to filter out of band, but can have reduced in-band spectral performance at prescaler frequencies <1.5GHz.
[4:1]	R/W	Reserved 1	4	15	Program 15
[7:5]	R/W	SD Mode	3	0	See “Operational Modes” for mode information. 0 - Fractional 1 - Integer 2 - Exact Freq Fractional (Program Reg 0Dh appropriately) 3 - FM mode (Program Reg 0Ch/Reg 0Dh for F2) 4 - PM mode (Program phase step in Reg 0Ah) 5 - Sweep - 1 way - Ramp then Hop (Triggered) 6 - Sweep - 2 way - Ramp Both directions (Triggered) 7 - Sweep - 2 way Auto - Ramp Both directions Continuously
[8]	R/W	autoseed (Frac modes) unidirectional phase (PM)	1	1	Non PM Mode 1: the modulator phase is initialized on trigger events or at the start of a frequency ramp. 0: the modulator is not re-initialized In PM mode (Reg06h[7:5]=4) 1: Trigger on rising edge only 0: Bi-phase modulation, level dependent
[9]	R/W	External Trigger Enable (EXTTRIG_EN)	1	1	Chooses to use the external TRIG pin for trigger events (frequency hops, ramp movement, phase or FM modulation). The function of this bit and the trigger system vary depending on SD Mode. See “Operational Modes” for more information.
[12:10]	R/W	Reserved 7	3	7	Program to 7
[13]	R/W	Force DSM Clock on	1	0	Forces the modulator clock on, despite being in integer mode. This is useful to test coupling from digital to analog.
[14]	R/W	BIST Enable	1	0	Internal Use only - Program to 0
[16:15]	R/W	Number of Bist Cycles	2	0	Internal Use only
[18:17]	R/W	DSM Clock Source	2	0	0 - SD Clock from Mcounter (Recommended > 50MHz) 1 - VDIV PFD Clock 2 - RDIV PFD Clock - Use for Phase Coherence 3 - XTAL (Use for BIST)
[19]	R/W	Invert DSM Clock	1	0	Test/BIST only
[20]	R/W	Reserved 0	1	0	Program to 0
[21]	R/W	Force RDIV bypass	1	0	If 1, the Rdivider can be used (and exported on GPO), but the PFD still uses the undivided XTAL
[22]	R/W	Disable Reset of extra accumulators on ramp	1	0	The Autoseed bit determines if the phase accumulator of the DSM is reset at the start of a frequency ramp. Normally the other accumulators are also reset - allowing for exact repeatability from cycle-to-cycle. This extra initialization is avoided if this bit is set - which can lead to more graceful transients at the start of a ramp.
[23]	R/W	Single Step Ramp Mode	1	0	Single step ramp mode. Advances the ramp one step per trigger. Can be used to generate arbitrary sweep profiles with an external trigger. Can also be used for sweep synchronization with the system.

Table 20. Reg 07h Lock Detect Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	R/W	LKDCounts	3	5	Lock Detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65535
[10:3]	R/W	Reserved	8	12d	Program 12d
[11]	R/W	LockDetect Counters Enable	1	1	Enable Lock Detect Counters (R07[14] should also = 1)
[13:12]	R/W	Reserved	2	0	Program 0
[14]	R/W	Lock Detect Timer Enable	1	1	Enable Lock Detect Timer (R07[11] should also = 1)
[15]	R/W	Cycle Slip Prevention Enable	1	0	Increases Charge Pump gain for phase errors larger than lock-detect timer.
[19:16]	R/W	Reserved 0	4	0	Reserved
[20]	R/W	Train Lock Detect Timer	1	0	This bit must be programmed from 0 to 1 after a change of PD reference clock frequency (via either the external reference or a change to the Rdivider).
[21]	R/W	Reserved	1	0	Reserved - Program to 1

Table 21. Reg 08h Analog EN Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	EnBias	1	1	Bias
[1]	R/W	EnCP	1	1	Charge-Pump
[2]	R/W	EnPFD	1	1	PFD
[3]	R/W	EnXtal	1	1	Reference Buffer
[4]	R/W	EnVCO	1	1	VCO Buffer
[5]	R/W	EnGPO	1	1	GPO Output Buffer Enable (If 0 the buffer is HiZ, if 1 the buffer MAY be HiZ depending on GPOSel and SPI activity)
[6]	R/W	EnMcnt	1	1	Mcounter
[7]	R/W	EnPS	1	1	Prescaler
[8]	R/W	EnVCOBias	1	1	VCO Divider Related Biases
[9]	R/W	EnOpAmp	1	1	Charge-Pump Amplifier
[12:10]	R/W	VCOOutBiasA	3	3	RF Divider Bias A Sel
[15:13]	R/W	VCOOutBiasB	3	3	RF Divider Bias B Sel
[16]	R/W	VCOBWSel	1	1	RF Buffer Bias Sel
[17]	R/W	RFDiv2Sel	1	0	Enables RF Divide/2
[18]	R/W	XtalLowGain	1	0	Lowers the gain (and extends BW) of the XTAL buffer
[19]	R/W	XtalDisSat	1	0	Disables saturation protection on the XTAL buffer

Table 22. Reg 09h Charge Pump Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[6:0]	R/W	CPIdn	7	100	Main Sink Current (20uA steps)
[13:7]	R/W	CPIup	7	100	Main Source Current (20uA steps)
[20:14]	R/W	CPOffset	7	0	Offset current (5uA steps) - See "Charge-Pump Phase offset" for more information.
[21]	R/W	CPSrcEn	1	0	Offset current polarity (Source Offset current) Recommended 0 in integer mode , PFDInv in FRAC modes.
[22]	R/W	CPSnkEn	1	1	Offset current polarity (Sink Offset current) Recommended 0 in integer mode ,NOT PFDInv in FRAC modes.
[23]	R/W	CPHiK	1	0	Hi Gain Mode (~4mA CP I boost depending on Vcp) - Use only with active loop filter configurations, where Vcp is controlled to offer better phase-noise.

Table 23. Reg 0Ah Modulation Step Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	MODSTEP	24	0	Fractional Modulation Step size for Ramp/Phase Modulation modes (Ignored in Integer, Normal Fractional, FM, or Exact Freq modes) This value is signed two's complement. Positive values ramps up, negative values ramp down.

Table 24. Reg 0Bh PD Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	R/W	PFDDly	3	1	Dead-zone avoidance delay (0~1 ns, 3~3 ns. > 3 is unused)
[3]	R/W	PFDShort	1	0	Tie both PD inputs to Ref or Div based on phase select.
[4]	R/W	PFDInv	1	0	Swap PD inputs for use in inverting loop configurations. 0- Use with a positive tuning slope VCO and passive loop filter (default) 1- Use with a negative tuning slope, or with an inverting active loop filter with a positive tuning slope VCO
[5]	R/W	PFDUpEn	1	1	0 will disable up pulses from propagating to the CP
[6]	R/W	PFDDnEN	1	1	0 will disable dn pulses from propagating to the CP
[7]	R/W	PFDForceUp	1	0	1 will force to the top rail.
[8]	R/W	PFDForceDn	1	0	1 will force to the bottom rail.
[9]	R/W	PFDForceMid	1	0	1 will force to mid-rail
[12:10]	R/W	PSBiasSel	3	0	PS Bias Current
[14:13]	R/W	OpAmpBiasSel	2	3	OpAmp Bias Current
[16:15]	R/W	McntClkGateSel	2	3	If the quantized divide ratio is guaranteed to be within a certain range, this feature can be enabled to reduce toggle activity and power consumption slightly. (0: 16 to 31, 1: 16 to 127, 2: 16 to 1023, 3: 16 to max)
[17]	R/W	VDIVExt	1	0	Extend VCO Divider Output Pulse width
[18]	R/W	LKDProcTesttoCP	1	0	Muxes the lock-detect oscillator to the CP force up/dn for observation.

Table 25. Reg 0Ch ALTINT

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[15:0]	R/W	ALTINT	16	25d	Stop freq for Ramp mode, Alternate freq for FM mode. See "Operation Modes" for more information.

Table 26. Reg 0Dh ALTFRAC

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	ALTFRAC	24	0	Stop freq for Ramp mode, Alternate freq for FM mode, number of channels/boundary for Exact frequency mode. See "Operation Modes" for more information.

Table 27. Reg 0Eh SPI TRIG

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	SPITRIG	1	0	This bit can be used as an alternative to the external TRIG pin. If Reg06h[9] (EXTTRIG_EN)= 0 then this bit is used to trigger sweep, FM, or PM modes, Trigger requires initial state of 0 followed by a write of 1. Register must be reset to 0 before subsequent triggers. If Reg06[8] = 0, then in PM mode this register is level sensitive and modulates the phase. See "Operating Modes" for more information.

Table 28. Reg 0Fh GPO Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[4:0]	R/W	GPOSel	5	1	0: Static test voltage - as defined by Reg 0Fh[5] 1: lock detect 2: lkd trigger 3: lkd window 4: process osc test 5: CSP UP control 6: CSP DN control 7: rdiv core 8: xtal 9: rdiv_pfd 10: vdiv_pfd 11: mcnt_sd 12: ramp_busy 13: ramp_started 14: ramp_trig_pulse 15:bist_busy 16: dn 17: up 18: bist_clk 19: ramp_clk 20: intg strobe 21: frac strobe 22: spi strobe 23: SPI sle 24: sd reload 25: sd full-reload 29 lkd training 30 outbuf en
[5]	R/W	GPOTest	1	0	Static test signal for output when GPOSel=1
[6]	R/W	GPOAlways	1	0	Prevents auto-muxing the GPO with SDO. It always stays GPO.
[7]	R/W	GPOOn	1	0	Keeps the GPO Driver in output mode (rather than selective drive based on ChipAddr), unless EnGPO=0.
[8]	R/W	GPOPullUpDis	1	0	Disables the GPO pull-up transistor (suitable for wired or with external pull-up or analog lock-detect methods)
[9]	R/W	GPOPullDnDis	1	0	Disables the GPO pull-dn transistor (suitable for wired or with external pull-dn or analog lock-detect methods)

Table 29. Reg 10h Reserve Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[8:0]	RO	Reserved	9	0	Reserved

Table 30. Reg 11h Reserve Register (Read Only)

BIT	*TYPE*	*NAME*	*W*	*DEFLT*	*DESCRIPTION*
[18:0]	*RO*	*Reserved*	*19*	*0*	*Reserved*

Table 31. Reg 12h GPO2 Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	RO	GPO	1	0	GPO
[1]	RO	Lock Detect	1	0	Lock Detect
[2]	RO	Ramp Busy	1	0	Ramp Busy

Table 32. Reg 13h BIST Status (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[15:0]	RO	BIST Signature	16		Internal Use Only
[16]	RO	BIST Busy	1		Internal Use Only

Table 33. Reg 14h Lock Detect Timer Status (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	RO	LkdSpeed	3	0	Lock Detect Timer Trained Speed
[3]	RO	LkdTraining	1	0	Lock Detect Timer is busy training