SONY CXA1076K/CXA1176K

8-bit 200/300 MSPS Flash A/D Converter

Description

The CXA1076K/CXA1176K are monolithic flash A/D converters capable of digitizing 0 to −2V analog input signal into 8-bit binary code at a sampling rate of 200MSPS (CXA1076K)/ 300MSPS (CXA1176K).

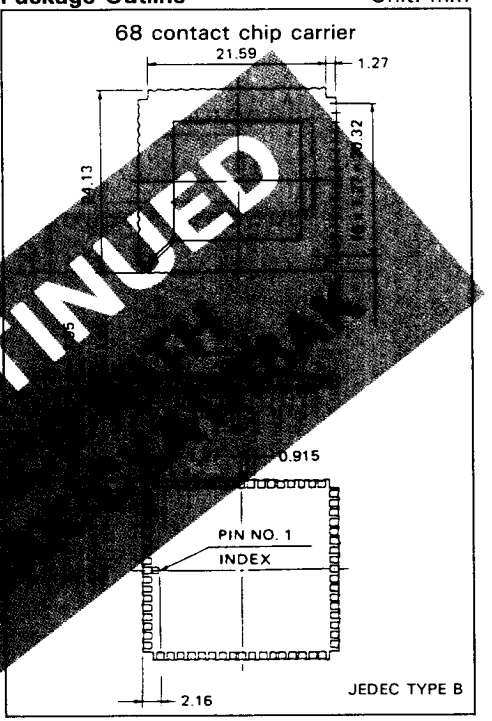
They operate with a single −5.2V power supply and consume only 720/1300 mW.

The digital I/O level is compatible with 100K/10KH/10K series ECL, and complementary digital output makes ease to interface to external circuits. Output ports have a capability to drive into 50 Ω load to −2 V.

In addition to 8-bit output data, they have a over range output and two digital inputs w enable to program output format for tru verse binary and offset two's compl

Package Outline

Unit: mm



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Features

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- Ultra high speed 3 SPS
- Wide input band widt M
- Low power consu 20/ 20
- Internal linearity sa
- Complement L outp
- Over range
- Programmab t fo
- Small 68 LCC

Applications

Digital oscilloscope, rad sing, transient capture and fast digital signal processing.

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	0.5 to −7	V
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}	0.5 to V_{EE}	V
	V_{RT}-V_{RB}	0 to 2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to V_{EE}	V
• Digital output current	ID0 to ID7, IOR	0 to −30	mA
	$\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$	0 to −30	mA
• Operating temperature	T_a	−25 to +75	°C
	T_c	−55 to +125	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.8	W

70125-YA

SONY® CXA1076AK/CXA1176AK

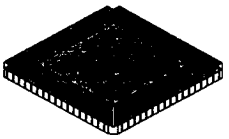
8-bit 200/300 MSPS Flash A/D Converter

Advance Information

Evaluation Board Available — CXA1076AK PCB/CXA1176AK PCB

Notice: This specification is subject to change.

68 pin LCC (Ceramic)



Description

CXA1076AK/CXA1176AK are monolithic flash A/D converters capable of digitzing 0 to −2 V analog input signal into 8-bit binary code at a sampling rate of 200MSPS (CXA1076AK)/ 300MSPS (CXA1176AK).

They operate with a single −5.2 V power supply and consume only 1450 mW.

The digital I/O level is compatible with 100K/10KH/10K series ECL, and complementary digital output makes ease to interface to external circuits. Output ports have a capability to drive into 50 Ω load to −2 V.

In addition to 8-bit output data, they have an over range output and two digital inputs which enable to program output format for true or inverse binary and offset two's complement.

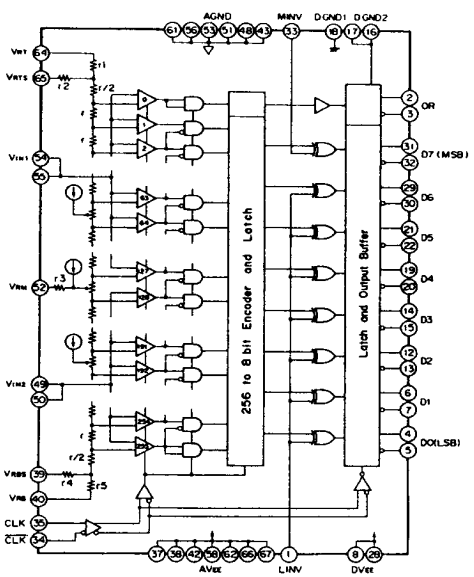
Features

- Ultra high speed
- Wide input band width
- Low power consumption 1450 mW
- Internal linearity compensation circuit
- Complementary ECL output
- Over range output
- Programmable output format
- Small 68 LCC package
- Pin replacable with CXA1076K/CXA1176K

Applications

Digital oscilloscope, radar, image processing, transient capture and fast digital signal processing.

Block Diagram



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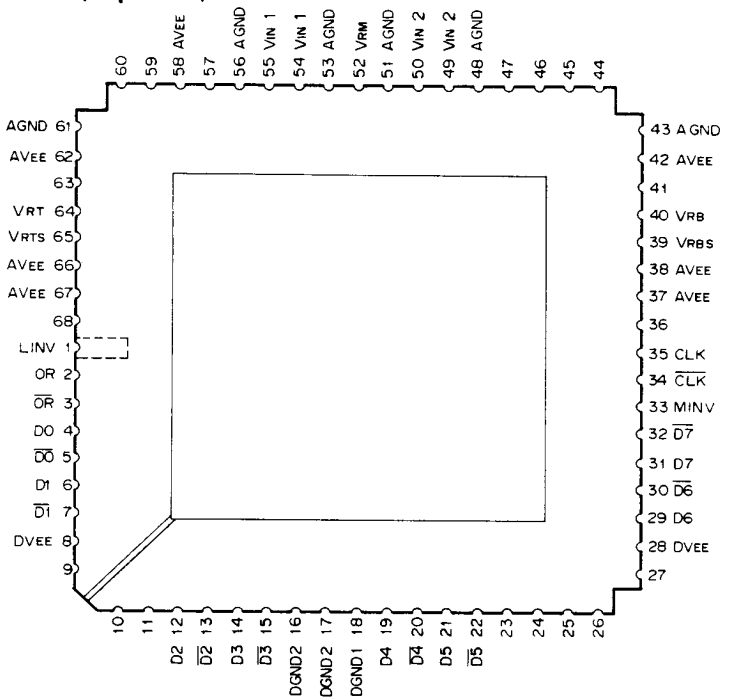
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	0.5 to −7	V
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}	0.5 to V_{EE}	V
	V_{RT}-V_{RB}	0 to 2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to V_{EE}	V
• Digital output current	ID0 to ID7, IOR	0 to −30	mA
	$\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$	0 to −30	mA
• Operating temperature	T_a	−25 to +75	°C
	T_c	−55 to +125	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.8	W

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	AV_{EE}, DV_{EE}	−4.95	−5.2	−5.5	V
Supply votage	$\lvert AV_{EE} - DV_{EE} \rvert$		0	0.05	V
Ground	| DGND − AGND |		0	0.05	V
Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
Reference input voltage	V_{RT}	−0.1	0	+0.2	V
Reference input voltage	V_{RB}	−2.2	−2	−1.9	V
Digital input voltage	V_{IH}	−1.0		−0.7	V
Digital input voltage	V_{IL}	−1.9		−1.6	V
Clock pulse width	TPW1 (CXA1076AK)	3.5			ns
Clock pulse width	TPW0 (CXA1076AK)	1.5			ns
Clock pulse width	TPW1 (CXA1176AK)	2.5			ns
Clock pulse width	TPW0 (CXA1176AK)	0.8			ns

Pin Configulation (Top View)



Timing Chart

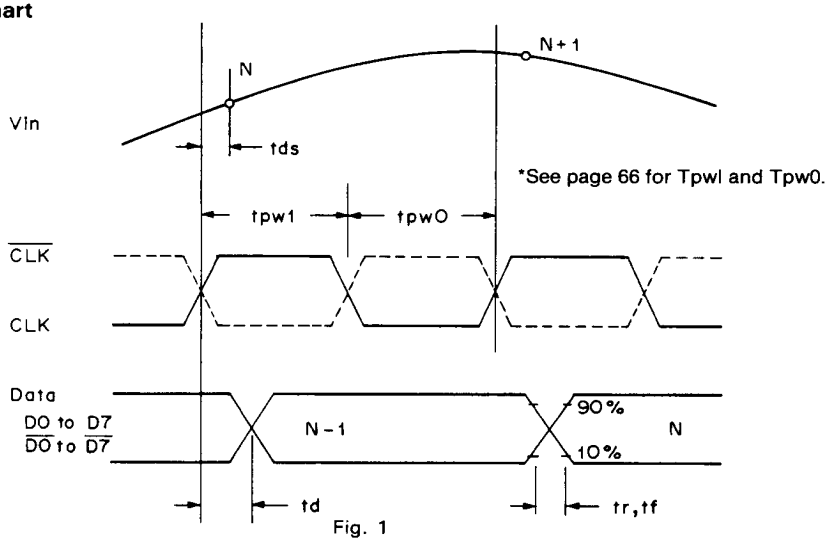
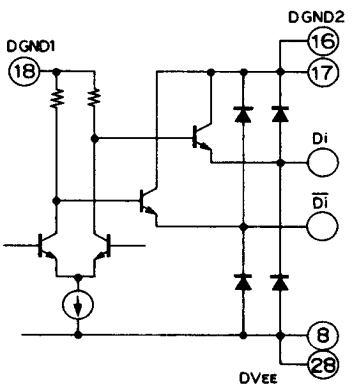
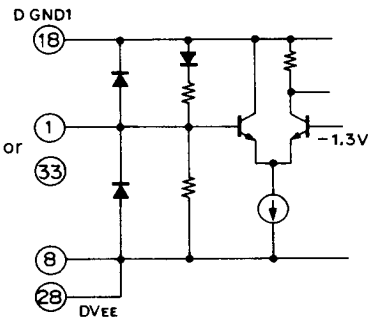
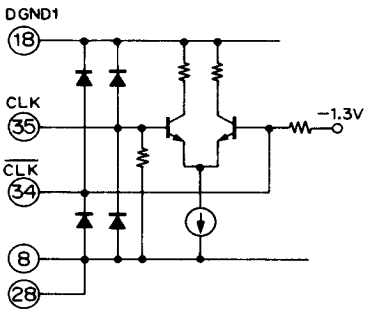
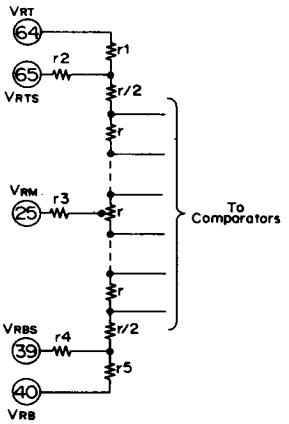
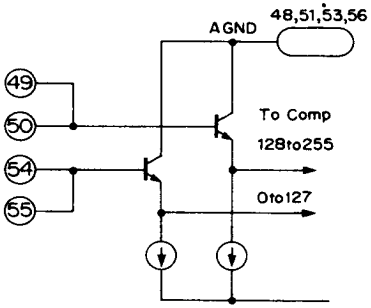
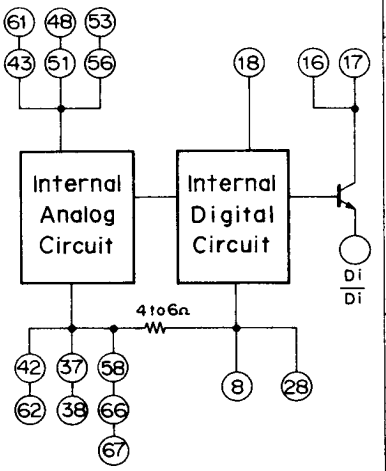


Fig. 1

Pin Description and I/O Equivalent Circuits

No.	Symbol	Equivalent circuit	Description
4 5	D_0 $\overline{D_0}$		LSB and complementary LSB output
6 7	D_1 $\overline{D_1}$		D_1 to D_6: output $\overline{D_1}$ to $\overline{D_6}$: complementary output
12 13	D_2 $\overline{D_2}$		
14 15	D_3 $\overline{D_3}$		
19 20	D_4 $\overline{D_4}$		
21 22	D_5 $\overline{D_5}$		
29 30	D_6 $\overline{D_6}$		
31 32	D_7 $\overline{D_7}$		MSB and complementary MSB output
2 3	$\overline{OR}$ OR		Over Range and complementary Over Range output
33	MINV		Polarity select for MSB (Refer to coding table) L level is maintained with left open.
1	LINV		Polarity select for LSBs (Refer to coding table) L level is maintained with left open.

No.	Symbol	Equivalent circuit	Description
35	CLK		CLK input
34	$\overline{CLK}$		Complementary CLK input V_{BB} (−1.3V) is maintained with left open. With bypassing, it can be used as a reference for single CLK input.
64	V_{RT}		Analog reference voltage (Top) (0V Typ.)
65	V_{RTS}		Reference voltage sense (Top)
52	V_{RM}		Reference voltage mid-point It can be used as a linearity compensation.
39	V_{RBS}		Reference voltage sense (Bottom)
40	V_{RB}		Analog reference voltage (Bottom) (−2V Typ.)
49 50 54 55	V_{IN}		Analog input All of the pins must be wired externally.

No.	Symbol	Equivalent circuit	Description
43, 48, 51, 53, 56, 61	AGND (*1)		Analog ground
37, 38, 42, 58, 62, 66, 67	AVEE (*1)		Analog supply
18	DGND1		Digital ground
16 17	DGND2 (*1)		Digital ground for output drive
8 28	DVEE (*1)		Digital supply
9, 10 11, 23 24, 25 26, 27 36, 68	NC		Empty pins It is recommended to wire these pins to DGND.
41, 44 45, 46 47, 57 59, 60 63	NC		Empty pins It is recommended to wire these pins to AGND.

(*1) All of these pins must be wired to the respective external circuit.

Input-Output Reference and Output Format

Vin	Step	MINV 1 LINV 1	0 1	1 0	0 0
		OR MSB LSB	OR MSB LSB	OR MSB LSB	OR MSB LSB
0V		0 0 0 0 · · · 0 0	0 1 0 0 · · · 0 0	0 0 1 1 · · · 1 1	0 1 1 1 · · · 1 1
	0	1 0 0 0 · · · 0 0	1 1 0 0 · · · 0 0	1 0 1 1 · · · 1 1	1 1 1 1 · · · 1 1
	1	1 0 0 0 · · · 0 1	1 1 0 0 · · · 0 1	1 0 1 1 · · · 1 0	1 1 1 1 · · · 1 0
		·	·	·	·
		·	·	·	·
		·	·	·	·
−1V	127	1 0 1 1 · · · 1 1	1 1 1 1 · · · 1 1	1 0 0 0 · · · 0 0	1 1 0 0 · · · 0 0
	128	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0	1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1
		·	·	·	·
		·	·	·	·
		·	·	·	·
	254	1 1 1 1 · · · 1 0	1 0 1 1 · · · 1 0	1 1 0 0 · · · 0 1	1 0 0 0 · · · 0 1
	255	1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0
−2V		1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0

Table 1

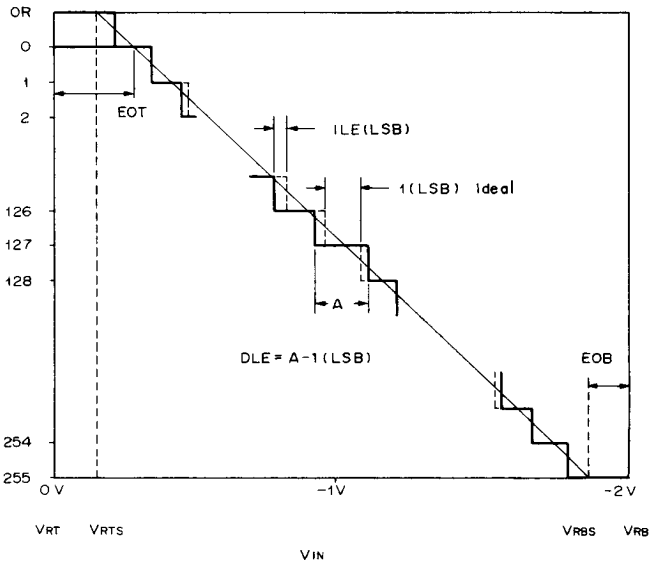


Fig. 2

Electrical Characteristics — CXA1076AK

T_a = 25°C, AV_{EE} = DV_{EE} = −5.2 V
V_{RT} = V_{RTS} = OV, V_{RB} = V_{RBS} = −2 V

Notice: Some parameter specs are subject to change.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate (1)		Fc	V_{IN} = FS, F_{IN} = 1 kHz	200	240		MSPS
Maximum conversion rate (2)		Fc	V_{IN} = FS F_{IN} = 49.999 MHz	200	240		MSPS
Resolution			Fc = 200 MSPS		8		bit
Integral linearity		EIL			±0.3	±0.5	LSB
Differential linearity		EDL			±0.3	±0.5	LSB
Offset error	V_{RT}	EOT		12.0	14.5	17.0	mV
	V_{RB}	EOB		4.0	6.5	9.0	mV
Analog input capacitance		CIN	V_{IN} = −1 V +0.07 rms	21	25	35	pF
Analog input current		IIN	V_{IN} = OV	70	150	700	μA
Supply current	Analog	IEEA		150	200	260	mA
	Digital	IEED		60	70	90	mA
Referrence resistance		RREF	V_{RT} to V_{RB}	75	90	108	Ω
Residual resistance		r1, r5		0.43	0.52	0.62	Ω
		r2, r4		0.64	0.77	0.92	Ω
		r3		2.8	3.4	4.1	Ω
Input level digital	H	VIH		−1.0	−0.85	−0.7	V
	L	VIL		−1.9	−1.75	−1.6	V
Output level digital	H	VOH	R_L = 50 Ω to −2 V FO = 1 (100 K ECL)	−1.05			V
	L	VOL				−1.6	V
Output data delay		td		1.7	2.0	3.1	ns
Rise time output digital		tr		0.8	1.2	1.5	ns
Fall time output digital		tf		0.8	1.2	1.5	ns
Full scale input BW (−3dB)		BWF	V_{IN} = FS (*1)		220		MHz
Small signal input BW		BWS	V_{IN} = 0.6 Vp-p (*1)		TBD		MHz
Aperture jitter		taj			3.0	3.6	ps
Sampling delay		tds		0.6	0.8	1.1	ns
SNR1			F_{IN} = 1 MHz FS (*1) Fc = 200MSPS		−46	−45.5	dB
SNR2			F_{IN} = 80 MHz, 0.6 Vp-p Fc = 200MSPS (*1)		TBD		dB
Differential gain		DG	NTSC 40 IRE mod. ramp Fc = 200 MSPS			1.0	%
Differential phase		DP				0.5	deg.
Error rate		ER	Fc = 200 MSPS F_{IN} = 49.999 MHz V_{IN} = 2 Vp-p tpw1 = 3.5 ns tpw0 = 1.5 ns Error Threshold: 32 LSB			10^{-8}	times/ sample

(*1) Source impedance = 50 Ω.

Electrical Characteristics — CXA1176AK

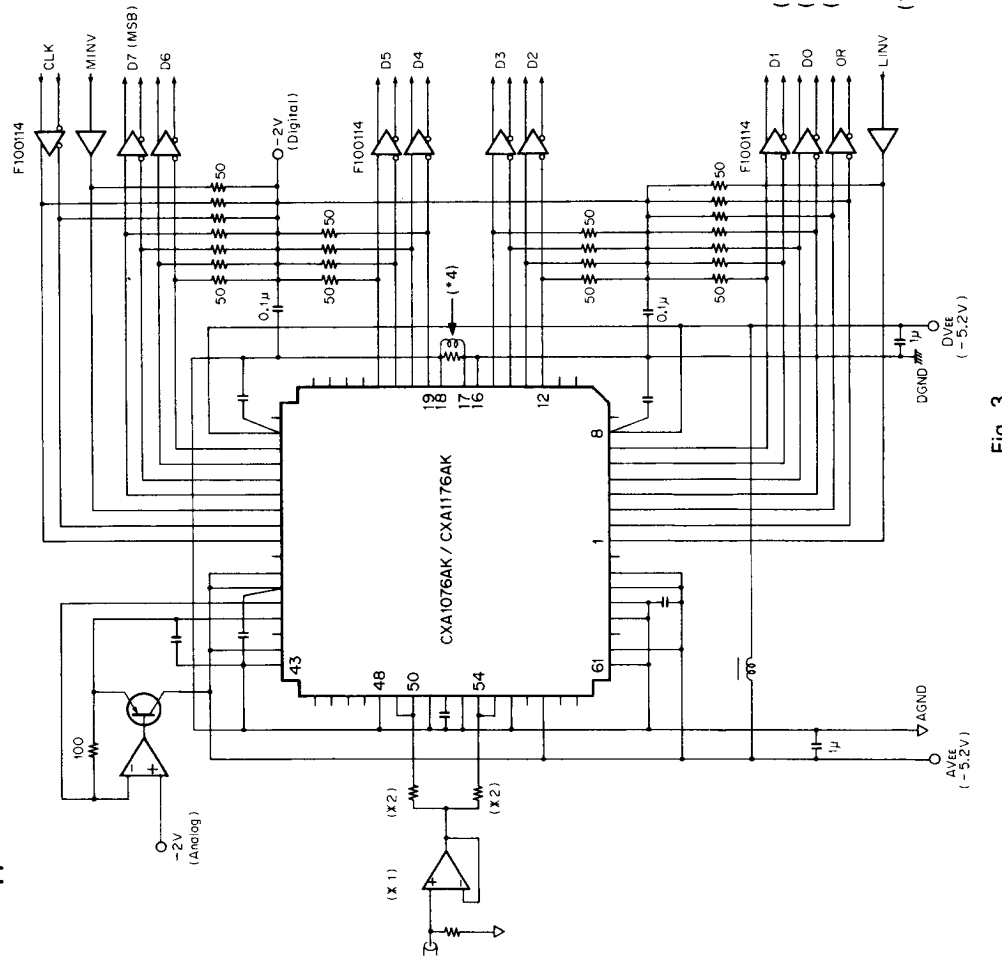
T_a = 25°C, AV_{EE} = DV_{EE} = −5.2 V
V_{RT} = V_{RTS} = OV, V_{RB} = V_{RBS} = −2 V

Notice: Some parameter specs are subject to change.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate (1)		Fc	V_{IN} = FS, F_{IN} = 1 kHz	300	340		MSPS
Maximum conversion rate (2)		Fc	V_{IN} = FS F_{IN} = 62.499 MHz	250	290		MSPS
Resolution			Fc = 300 MSPS		8		bit
Integral linearity		E_{IL}			±0.3	±0.5	LSB
Differential linearity		E_{DL}			±0.3	±0.5	LSB
Offset error	V_{RT}	E_{OT}		12.0	14.5	17.0	mV
	V_{RB}	E_{OB}		4.0	6.5	9.0	mV
Analog input capacitance		C_{IN}	V_{IN} = −1 V +0.07 rms	21	25	35	pF
Analog input current		I_{IN}	V_{IN} = OV	70	150	700	μA
Supply current	Analog	I_{EEA}		150	200	260	mA
	Digital	I_{EED}		60	70	90	mA
Referrence resistance		R_{REF}	V_{RT} to V_{RB}	75	90	108	Ω
Residual resistance		r1, r5		0.43	0.52	0.62	Ω
		r2, r4		0.64	0.77	0.92	Ω
		r3		2.8	3.4	4.1	Ω
Input level digital	H	V_{IH}		−1.0	−0.85	−0.7	V
	L	V_{IL}		−1.9	−1.75	−1.6	V
Output level digital	H	V_{OH}	R_L = 50 Ω to −2 V FO = 1 (100 K ECL)	−1.05			V
	L	V_{OL}				−1.6	V
Output data delay		td		1.7	2.0	3.1	ns
Rise time output digital		tr		0.8	1.2	1.5	ns
Fall time output digital		tf		0.8	1.2	1.5	ns
Full scale input BW (−3dB)		BWF	V_{IN} = FS (*2)		250		MHz
Small signal input BW		BWS	V_{IN} = 0.6 Vp-p (*2)		TBD		MHz
Aperture jitter		taj			3.0	3.6	ps
Sampling delay		tds		0.6	0.8	1.1	ns
SNR1			F_{IN} = 1 MHz FS Fc = 300MSPS (*2)		−46	−45.5	dB
SNR2			F_{IN} = 80 MHz, 0.6 Vp-p Fc = 300MSPS (*2)		TBD		dB
Differential gain		DG	NTSC 40 IRE mod. ramp Fc = 300 MSPS			1.0	%
Differential phase		DP				0.5	deg.
Error rate		ER	Fc = 250 MSPS F_{IN} = 62.499 MHz V_{IN} = 2 Vp-p tpw1 = 3.0 ns tpwo = 1.0 ns Error Threshold: 32 LSB			10^{-8}	times/ sample

(*2) Source impedance = 50 Ω.

Application Circuit



(*1) Comlinear CLC231 or equiv.
(*2) To be selected (2 to 20Ω)
(*3) Capacitors are 0.01μF ceramic chip not otherwise specified.
(*4) R: 1 Ω with very low inductance
L: 0.22 μH
This is optional for preventing oscillation

Fig. 3

Notes on Application

1) AGND, DGND, AV_{EE} and DV_{EE} planes on a PCB should be designed to make those impedance small for the noise suppression benefits. Those planes should be made as wide as possible on the PCB with at least double layer metal patterns.

2) It is recommended to separate the analog and digital V_{EE} on the PCB patterns to make reduce a noise contamination from digital system to analog system.

3) If separate V_{EE} and GND are used, it is recommended to connect the digital and analog planes by a core inductor with good frequency characteristics to avoid the DC voltage difference between analog and digital planes.
The DC voltage difference between AGND and DGND degrades performance and a continual voltage difference between AV_{EE} and DV_{EE} may cause a destruction of the device.

4) The analog and analog power supply pins should be bypassed as close to the device as possible to their respective grounds with at least a 10 nF ceramic chip capacitor. A 1 μF tantalum capacitor can also be used for low frequency bypassing.

5) Pin connections for the device should be made as short as possible. Using of a socket might degrade the performance because of an increasing of lead inductance. A possible compromise is to use AMP's socket 55159-2 (with heat sink).

6) A wide band drive amplifier with sufficient drivability and stable operation should be used to drive analog input pin. Comlinear's CLC231 may be used with adiquate frequency compensation.

7) As the analog input impedance of the device is capacitive, the driving amplifier occationally falls into unstable condition and oscillates locally. This instability can be prevented with a resistor inserted in series between the output pin of the amplifier and V_{IN} pins of the device. The resistor is to be selected from 2 to 20 Ω. Separate input for V_{IN} as shown in an application circuit (Fig. 3) may give a good result.

8) Digital output is delivered in complementary to make ease to interface in high speed operation. A 50 Ω termination at the endpoint of the wiring for both Di and $\overline{Di}$ is recommended for noise suppression benefits.

9) V_{RTS} and V_{RBS} pins can be used as a sense for precise adjustment of reference voltage. Fig. 4 shows the adjustment scheme.

10) Internal current compensation circuit for the reference resistor is furnished in the device. This circuit compensates input bias current of the comparators to maintain the linearity over wide temperature range.
V_{RM}, the mid-point of the reference resistor can be used as a trimming pin for more accurate linearity as shown in Fig. 4.
V_{RT}, V_{RB} and V_{RM} should be bypassed to AGND with at least a 100 nF ceramic chip capacitor.

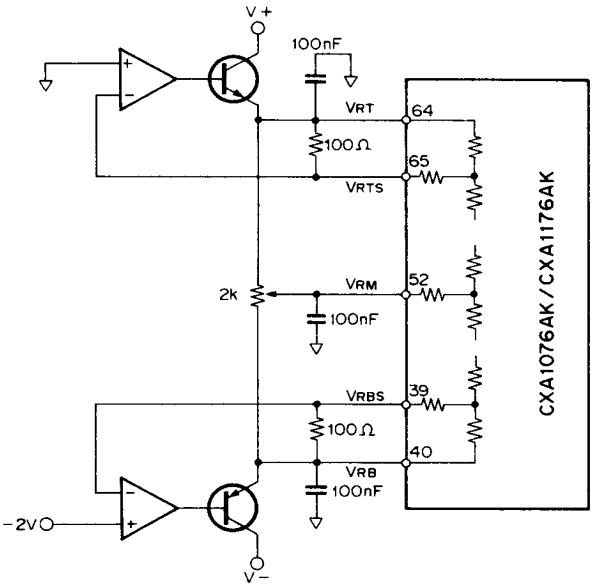
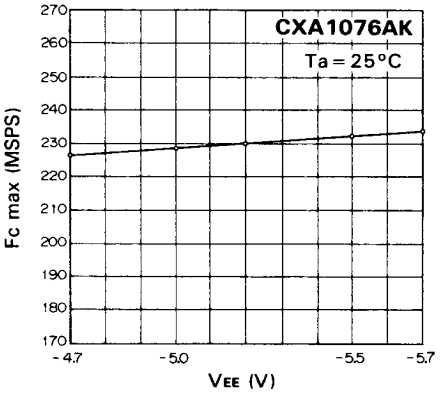


Fig. 4

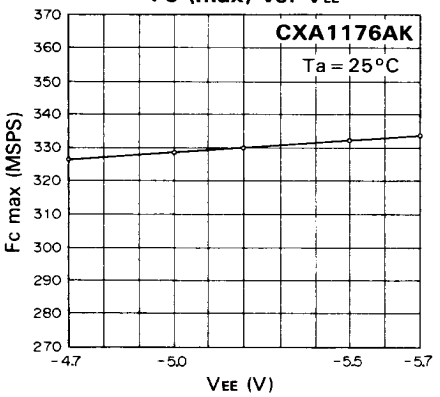
11) OR and $\overline{OR}$ output indicate that the input signal exceeds positive input range. MINV and LINV are not effective to the polarity of OR and $\overline{OR}$ (Refer to the output format).

12) **Pin 18 should be tied with AGND pins, not with system digital GND. Small resistor (approx. 1 ohm) and inductance 0.22 μH having small resistance are recommended to use between pin 17 and 18. See "Application Circuit".**

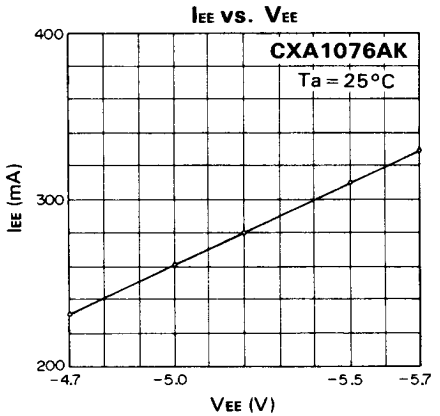
Fc (max) vs. V_{EE}



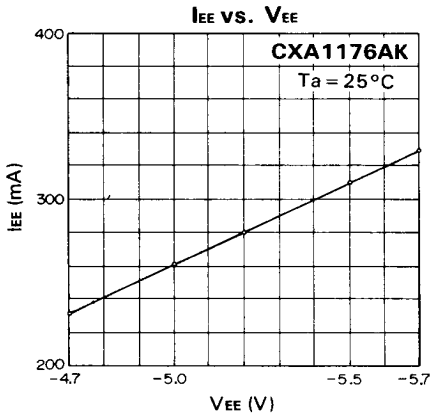
Fc (max) vs. V_{EE}



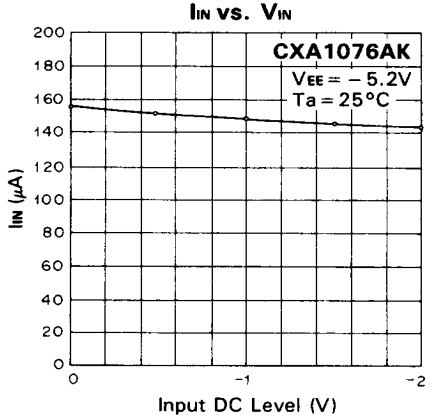
I_{EE} vs. V_{EE}



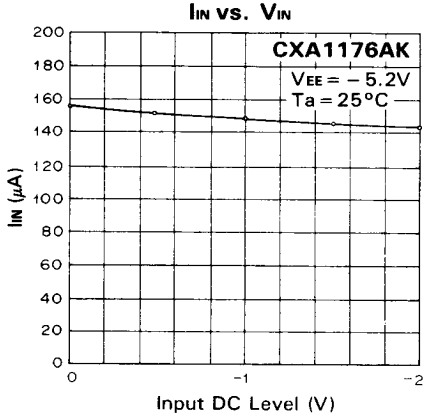
I_{EE} vs. V_{EE}



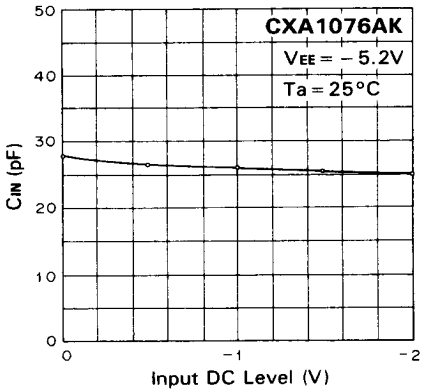
I_{IN} vs. V_{IN}



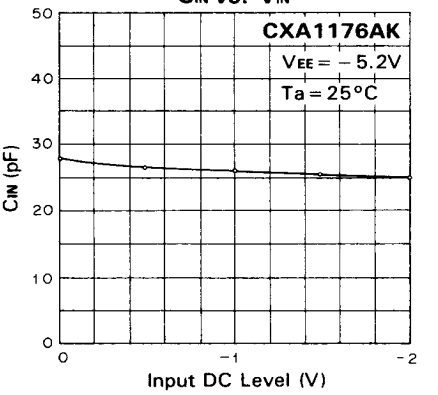
I_{IN} vs. V_{IN}



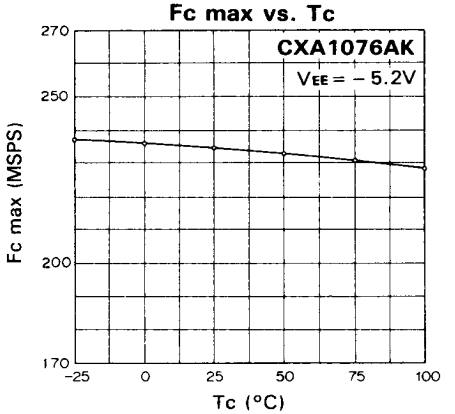
C_{IN} vs. V_{IN}



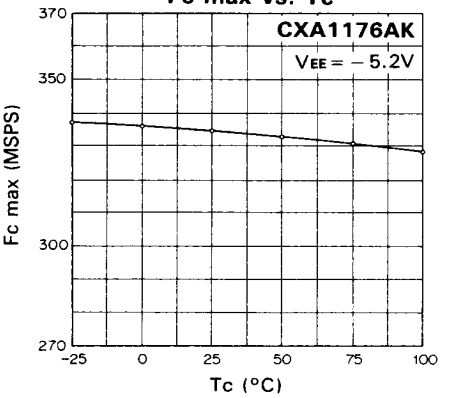
C_{IN} vs. V_{IN}



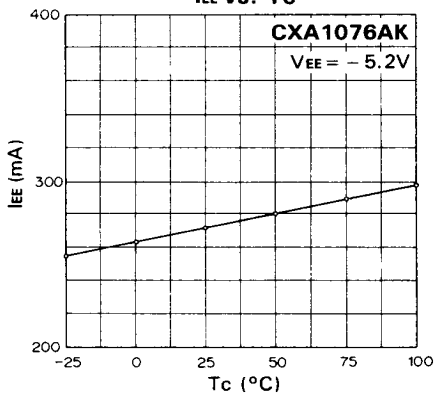
Fc max vs. Tc



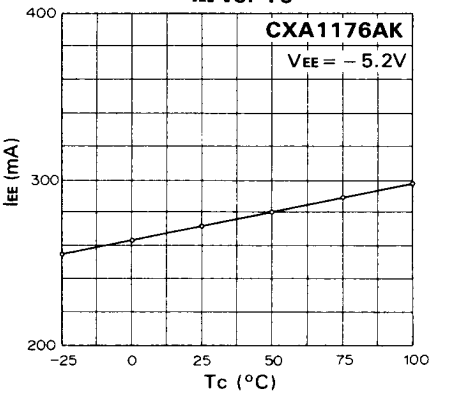
Fc max vs. Tc

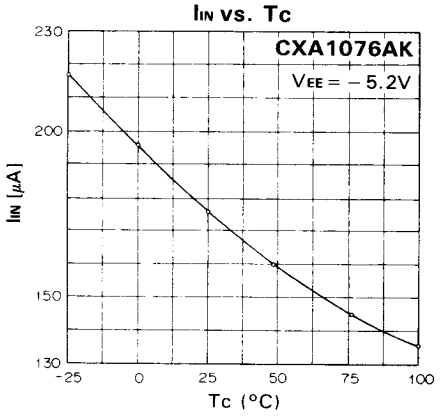


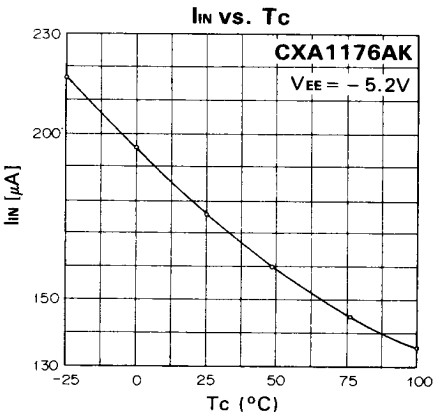
I_{EE} vs. Tc

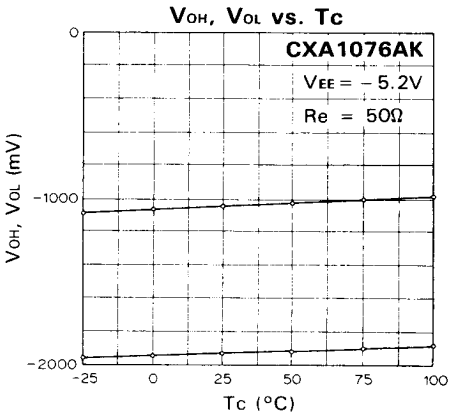


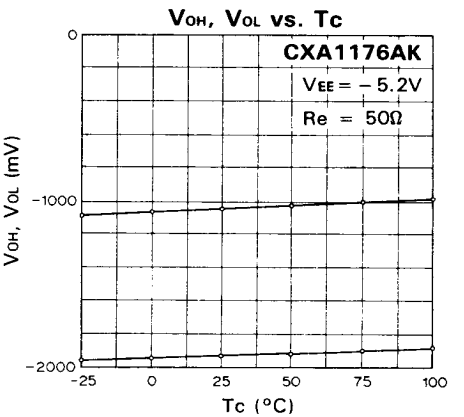
I_{EE} vs. Tc

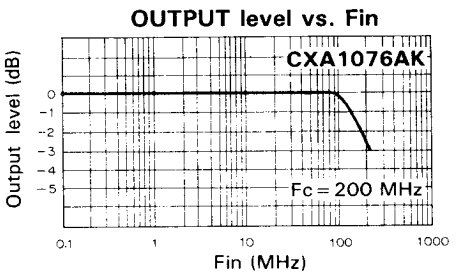






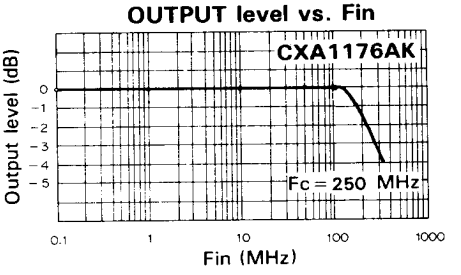






VEE = −5.2V Ta = 25°C Vin = FS

Preliminary

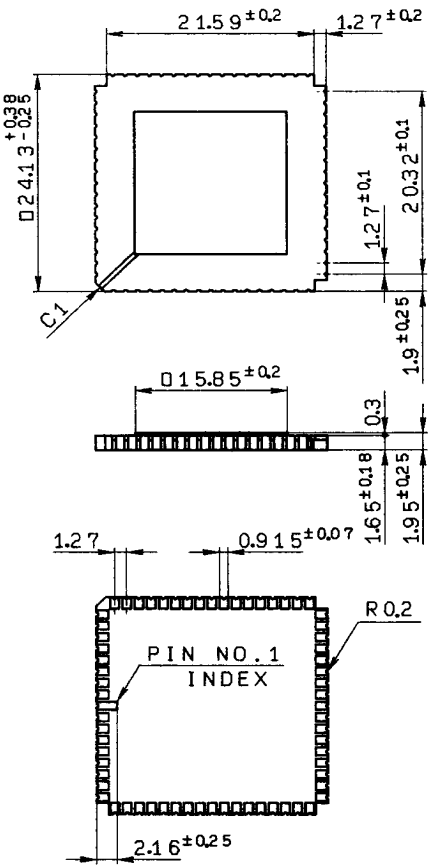


VEE = −5.2V Ta = 25°C Vin = FS

Preliminary

Package Outline Unit: mm

68 pin LCC (Ceramic) 3.7 g



LCC-68C-01