AT28MC020

T-46-13-27

2

2 Megabit (256K x 8) Paged CMOS E²PROM Module

Preliminary

Features

- Fast Read Access Time - 150ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80mA Active Current
  - 5mA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

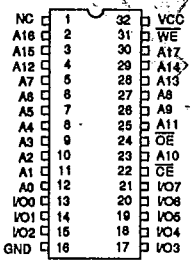
Description

The AT28MC020 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its two megabit of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 5mA.

The AT28MC020 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28MC020 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

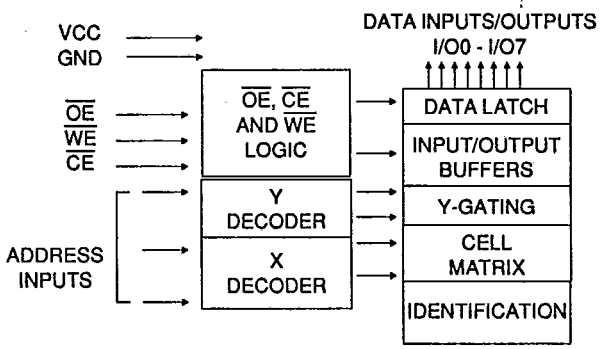
Pin Configurations



Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

T-46-13-27

Block Diagram



Device Operation

READ: The AT28MC020 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28MC020 allows one to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A17 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC020 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28MC020 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28MC020 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V (typical) the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28MC020. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to Vcc +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28MC020-15	AT28MC020-20	AT28MC020-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

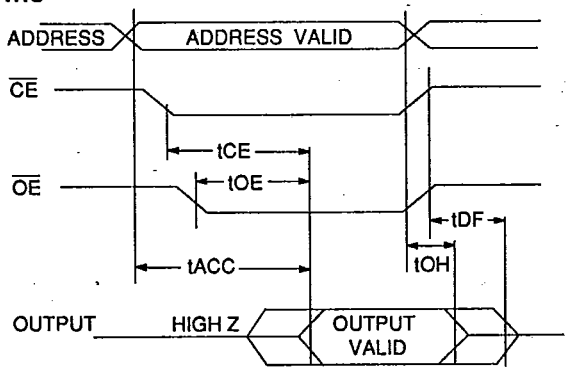
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to Vcc + 1V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to Vcc		20	µA
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$=Vcc-.3V to Vcc + 1V		5	mA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$=2.0V to Vcc + 1V		8	mA
I_{CC}	Vcc Active Current	f=5MHz; I_{OUT}=0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA	2.4		V

A.C. Read Characteristics

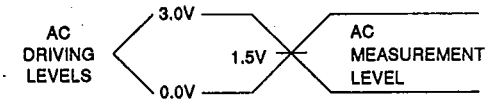
Symbol	Parameter	AT28MC020-15 Min	AT28MC020-15 Max	AT28MC020-20 Min	AT28MC020-20 Max	AT28MC020-25 Min	AT28MC020-25 Max	Units
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



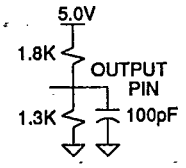
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

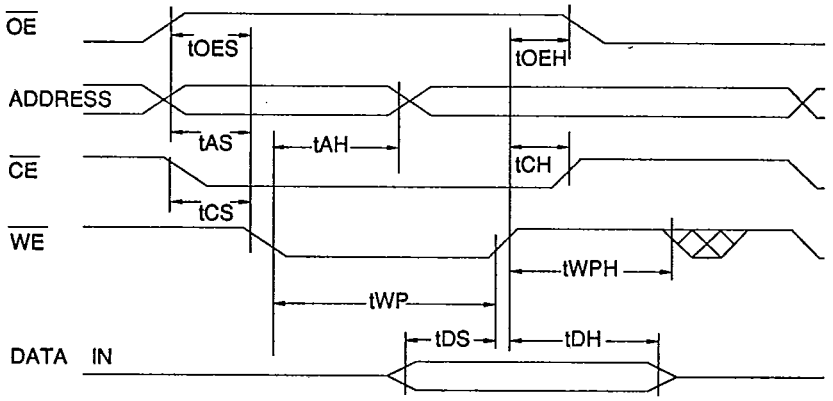
	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0V
C_{OUT}	20	40	pF	V_{OUT} = 0V

A.C. Write Characteristics

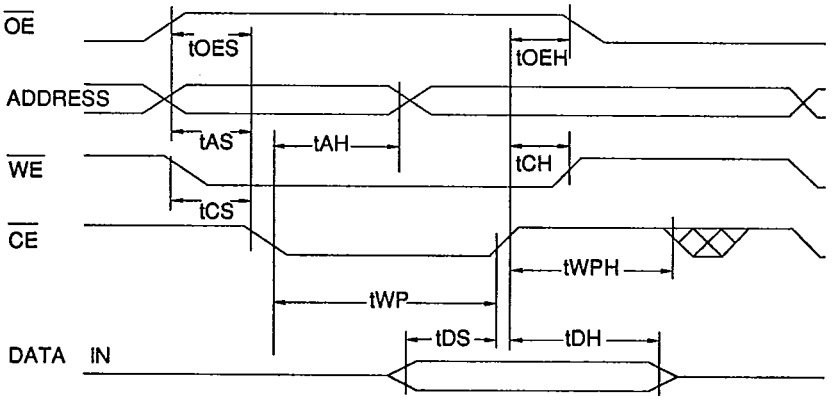
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled



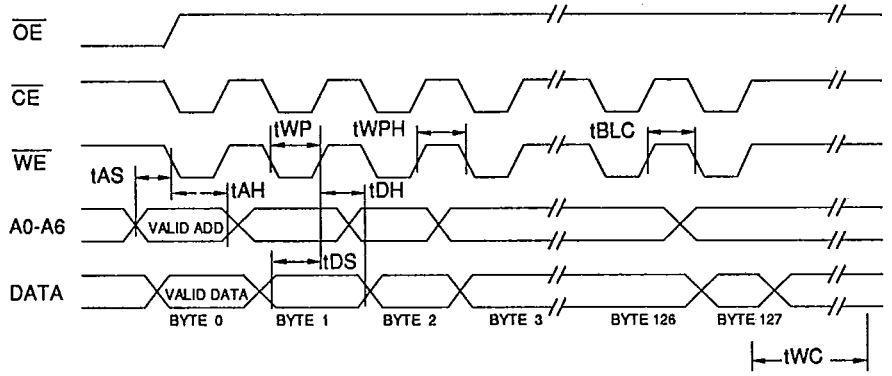
T-46-13-27

Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

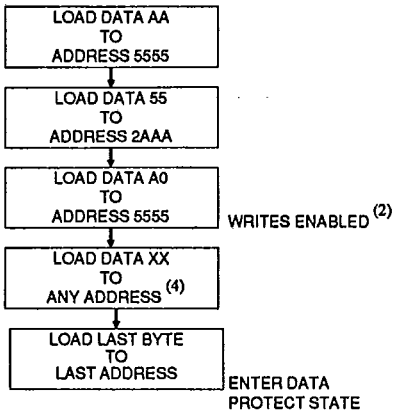
Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

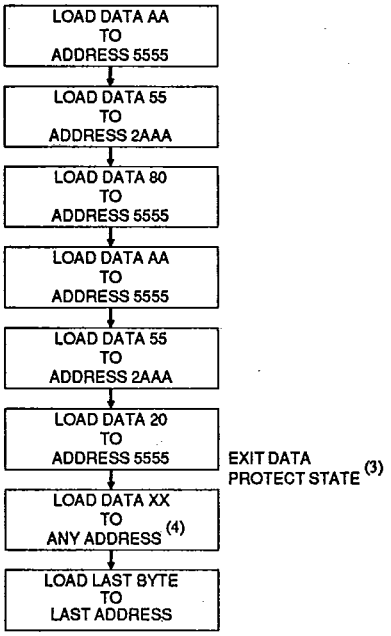


Notes: A7 through A17 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1,5,6]

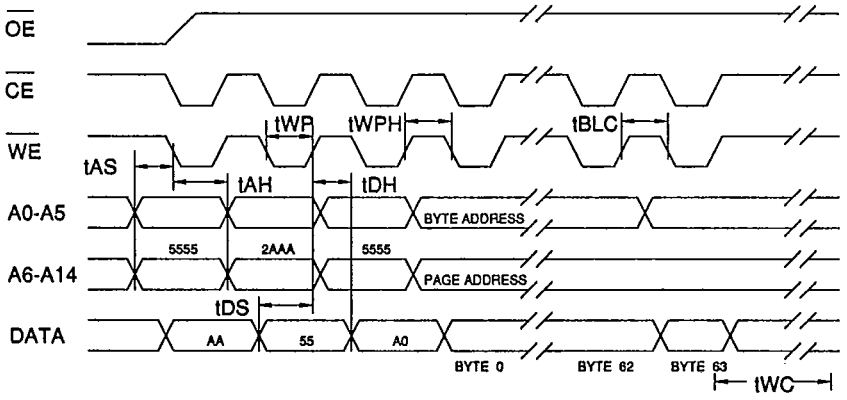


Software Data Protection Disable Algorithm [1,5,6]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A17 must address page to be written.
6. The quadrant determined by A17 acts independently.

Software Protected Program Cycle Waveform



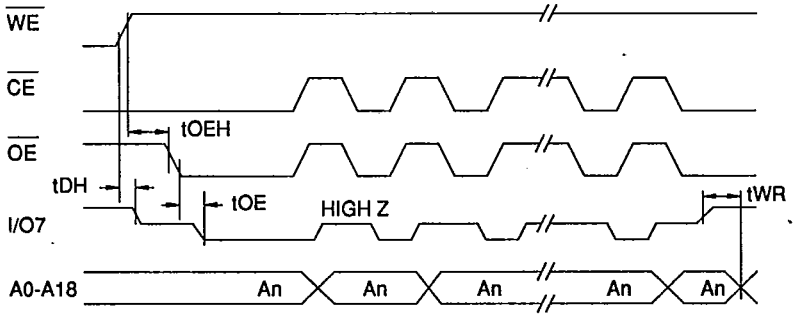
Notes: A6 through A17 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
A17 must address the desired quadrant while writing the software data protection code.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms



Ordering Information

tACC (ns)	ICC (mA) Active	ICC (mA) Standby	Ordering Code	Package	Operation Range
150	80	0.5	AT28MC020-15MC AT28MC020-15ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC020-15MC AT28MC020-15ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC020-15MM AT28MC020-15ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC020-15MMB AT28MC020-15ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)
200	80	0.5	AT28MC020-20MC AT28MC020-20ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC020-20MI AT28MC020-20ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC020-20MM AT28MC020-20ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC020-20MMB AT28MC020-20ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)
250	80	0.5	AT28MC020-25MC AT28MC020-25ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC020-25MI AT28MC020-25ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC020-25MM AT28MC020-25ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC020-25MMB AT28MC020-25ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)

Package Type	
32M2	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)