CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

PRELIMINARY
IDT7030SA/LA
IDT7040SA/LA

FEATURES:

- High-speed access
  - —Military: 25/35/45ns (max.)
  - —Commercial: 20/25/35ns (max.)
- Low-power operation
  - —IDT7030/40SA
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - —IDT7030/40LA
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- MASTER IDT7030 easily expands data bus width to 16-or-more-bits using SLAVE IDT7040
- On-chip port arbitration logic (IDT7030 only)
- $\overline{\text{BUSY}}$ output flag on IDT7030; $\overline{\text{BUSY}}$ input on IDT7040
- $\overline{\text{INT}}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

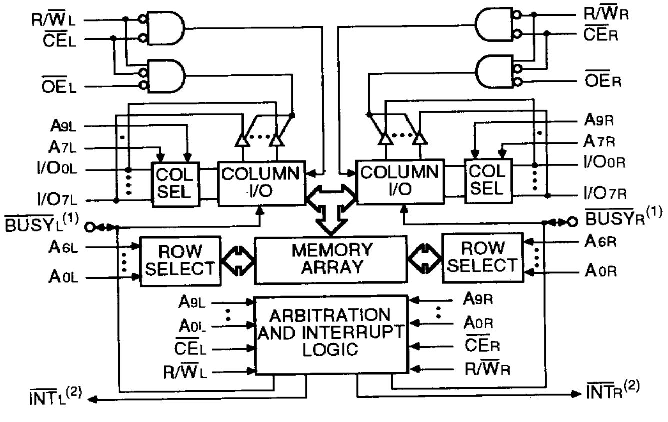
The IDT7030/IDT7040 are high speed 1K x 8 dual-port static RAMs. The IDT7030 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7040 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/ SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{\text{CE}}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7030/IDT7040 devices are packaged in 48-pin sidebraze or plastic DIPs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2690 drw 01

NOTES:
1. IDT7030 (MASTER): $\overline{\text{BUSY}}$ is open drain output and requires pullup resistor.
   IDT7040 (SLAVE): $\overline{\text{BUSY}}$ is input.
2. Open drain output: requires pullup resistor.

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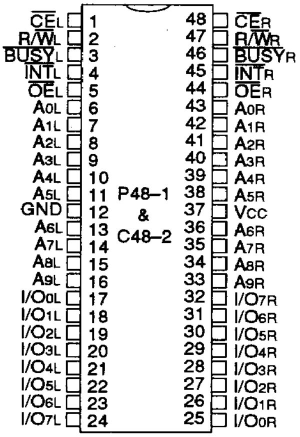
PIN CONFIGURATIONS



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DIP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2690 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2690 tbl 04

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2690 tbl 02

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2690 tbl 03

6-2-2

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7030SA IDT7040SA Min.	Max.	IDT7030LA IDT7040LA Max.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4.0mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2690 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7030 x 20[2] 7040 x 20[2]		7030 x 25 7040 x 25		7030 x 35 7040 x 35		7030 x 45[3] 7040 x 45[3]		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	125	300	125	290	125	285	mA
				LA	—	—	125	240	125	230	125	225	
			Com'l.	SA	125	265	125	260	125	250	—	—	
				LA	125	215	125	210	125	200	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX}[4]	Mil.	SA	—	—	30	80	30	80	30	80	mA
				LA	—	—	30	60	30	60	30	60	
			Com'l.	SA	30	65	30	65	30	65	—	—	
				LA	30	45	30	45	30	45	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	80	195	80	185	80	180	mA
				LA	—	—	80	160	80	150	80	145	
			Com'l.	SA	80	180	80	175	80	165	—	—	
				LA	80	145	80	140	80	130	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil.	SA	—	—	1.0	30	1.0	30	1.0	30	mA
				LA	—	—	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	—	—	
				LA	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f=f_{MAX}[4]	Mil.	SA	—	—	70	185	70	175	70	170	mA
				LA	—	—	70	150	70	140	70	135	
			Com'l.	SA	70	175	70	170	70	160	—	—	
				LA	70	140	70	135	70	125	—	—	

2690 tbl 06

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.
7. At V_{CC}≤2.0V input leakages are undefined.

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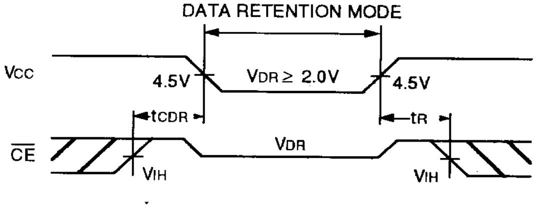
6-2-3

DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7030LA/IDDT7040LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$		2.0	—	0	V
I_{CCDR}	Data Retention Current	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Mil.	—	100	4000	μA
			Com'l.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2690 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2690 tbl 08

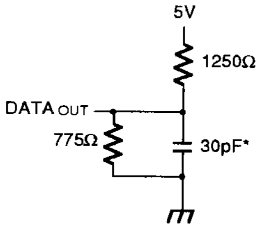


Figure 1. Output Load

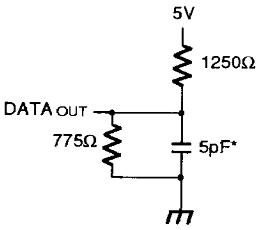


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

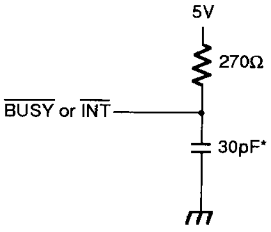


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

2690 drw 04

* Including scope and jig

6-2-4

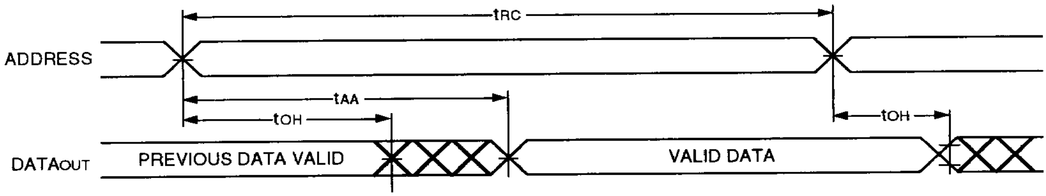
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	7030 x 20(2) 7040 x 20(2)		7030 x 25 7040 x 25		7030 x 35 7040 x 35		7030 x 45(3) 7040 x 45(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
t_{AOE}	Output Enable Access Time	—	10	—	12	—	25	—	30	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
t_{LZ}	Output Low Z Time(1,4)	0	—	0	—	0	—	0	—	ns
t_{HZ}	Output High Z Time(1,4)	—	8	—	10	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	—	50	ns

2690 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1,2,4)

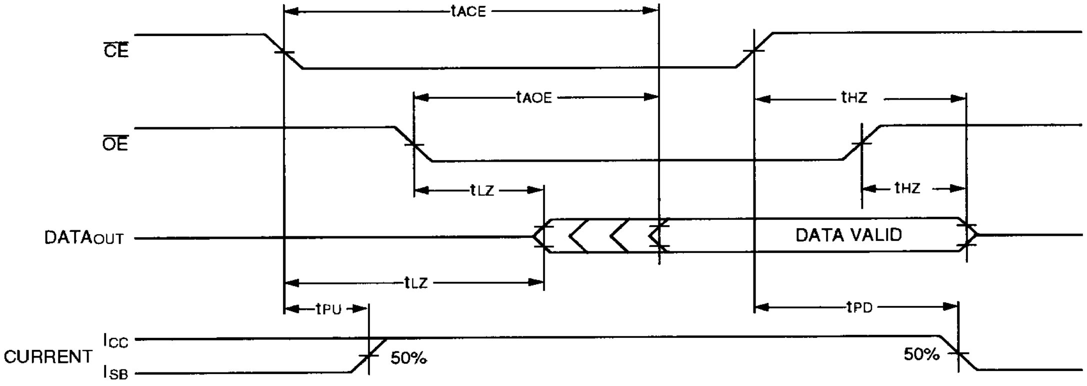


2690 drw 05

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

6-2-5

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1,3)



2690 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(7)

Symbol	Parameter	7030 x 20[2] 7040 x 20[2]		7030 x 25 7040 x 25		7030 x 35 7040 x 35		7030 x 45[3] 7040 x 45[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time[5]	20	—	25	—	35	—	45	—	ns
t_{EW}	Chip Enable to End of Write	15	—	20	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width[6]	15	—	20	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	10	—	12	—	20	—	20	—	ns
t_{HZ}	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z[1,4]	—	8	—	10	—	15	—	20	ns
t_{OW}	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	ns

NOTES:

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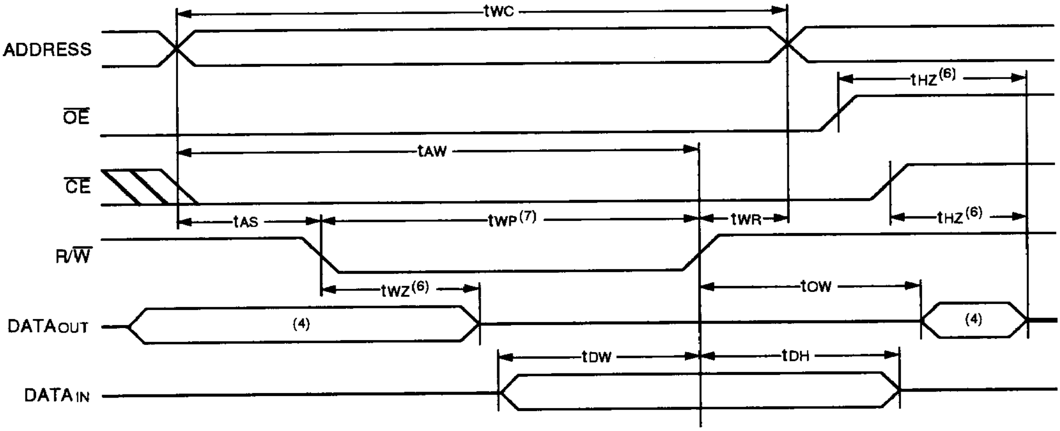
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, t_{WC} = t_{BAA} + t_{WP}.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (SA or LA).

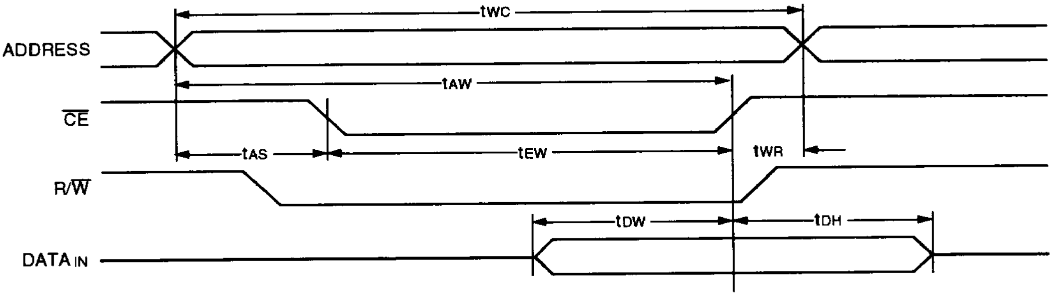
6-2-6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2690 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2690 drw 08

NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

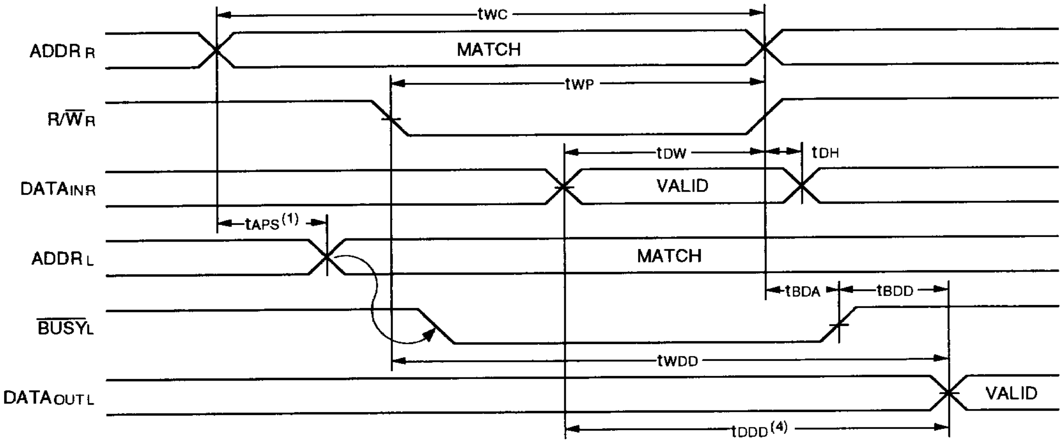
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE$^{(8)}$

Symbol	Parameter	7030 x 20$^{(1)}$ 7040 x 20$^{(1)}$		7030 x 25 7040 x 25		7030 x 35 7040 x 35		7030 x 45$^{(2)}$ 7040 x 45$^{(2)}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing (For Master IDT7030 Only)										
t_{BAA}	$\overline{\text{BUSY}}$ Access Time to Address	—	20	—	25	—	35	—	35	ns
t_{BDA}	$\overline{\text{BUSY}}$ Disable Time to Address	—	20	—	20	—	30	—	35	ns
t_{BAC}	$\overline{\text{BUSY}}$ Access Time to Chip Enable	—	20	—	20	—	30	—	30	ns
t_{BDC}	$\overline{\text{BUSY}}$ Disable Time to Chip Enable	—	20	—	20	—	25	—	25	ns
t_{WDD}	Write Pulse to Data Delay$^{(3)}$	—	50	—	50	—	60	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay$^{(3)}$	—	35	—	35	—	45	—	55	ns
t_{APS}	Arbitration Priority Set-up Time$^{(4)}$	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{\text{BUSY}}$ Disable to Valid Data$^{(5)}$	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7040 Only)										
t_{WB}	Write to $\overline{\text{BUSY}}$ Input$^{(6)}$	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{\text{BUSY}}$$^{(7)}$	12	—	15	—	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay$^{(9)}$	—	50	—	50	—	60	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay$^{(9)}$	—	35	—	35	—	45	—	55	ns

2690 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{\text{BUSY}}$ (For Master IDT7030 only)".
4. To ensure that the earlier of the two ports wins.
5. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD}-t_{WP} (actual) or t_{DDD}-t_{DW} (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (for Slave IDT7040 Only)".

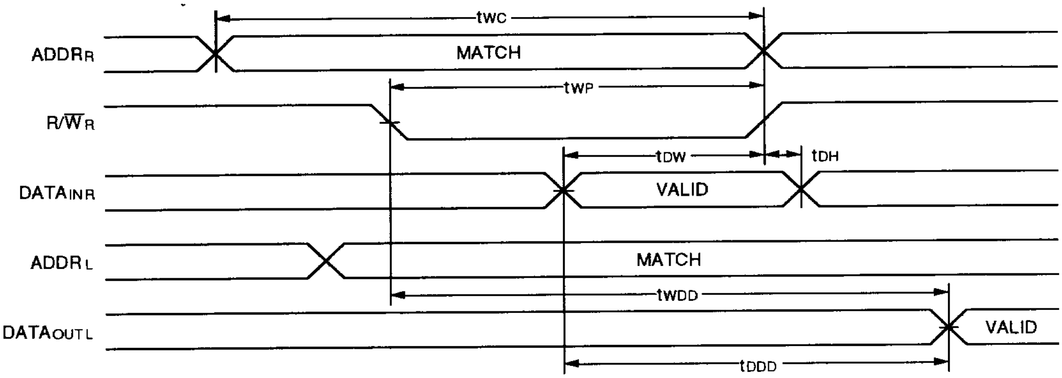
TIMING WAVEFORM OF READ WITH $\overline{\text{BUSY}}$(1,2,3) (FOR MASTER IDT7030 ONLY)



2690 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{\text{OE}}$ at LO for the reading port.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1,2,3) (FOR SLAVE IDT7040 ONLY)



NOTES:
1. Assume $\overline{\text{BUSY}}$ input at HI for the writing port, and $\overline{\text{OE}}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

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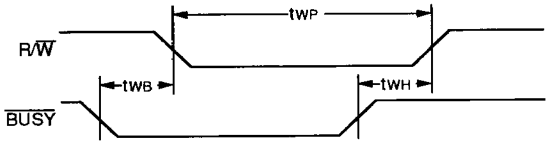
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7040 ONLY)

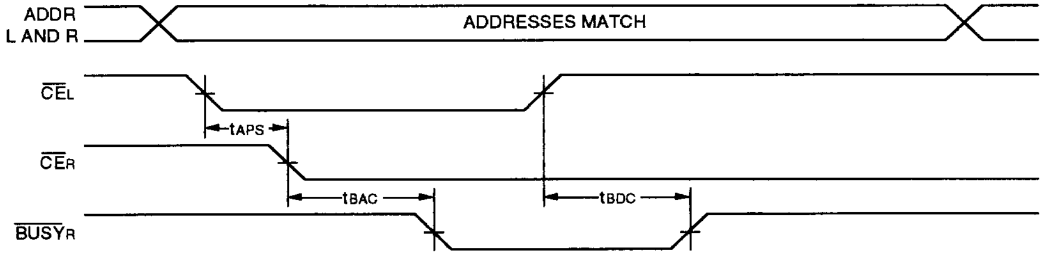


2690 drw 11

6-2-9

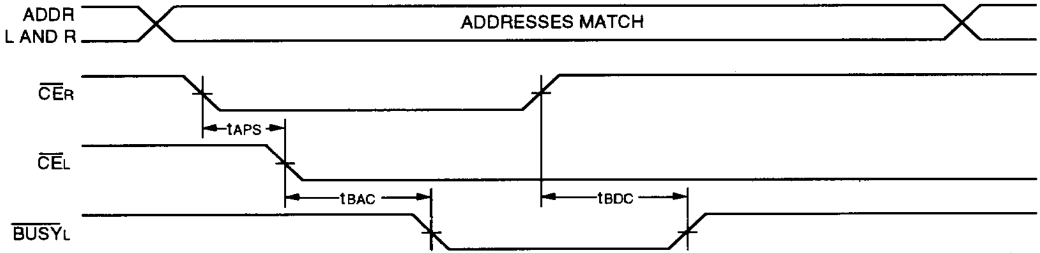
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7030 ONLY)

$\overline{CE}_L$ VALID FIRST:



2690 drw 12

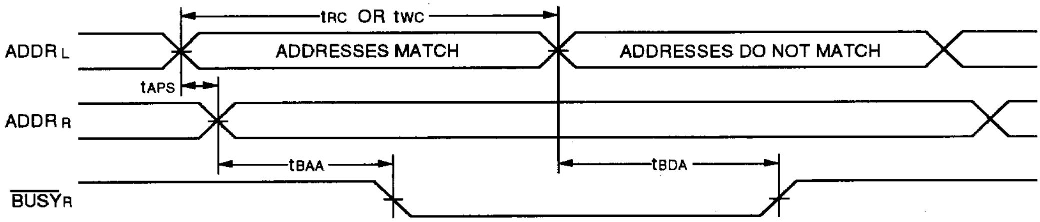
$\overline{CE}_R$ VALID FIRST:



2690 drw 13

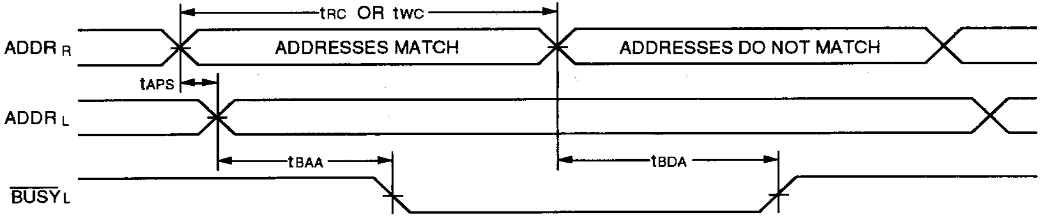
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1) (FOR MASTER IDT7030 ONLY)

LEFT ADDRESS VALID FIRST:



2690 drw 14

RIGHT ADDRESS VALID FIRST:



2690 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

6-2-10

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(3)

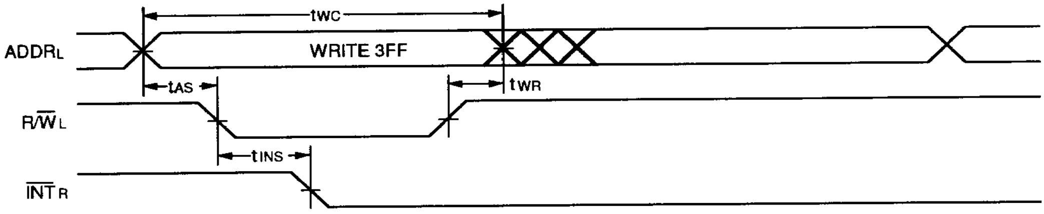
Symbol	Parameter	7030 x 20(1) 7040 x 20(1) Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45(2) 7040 x 45(2) Min.	Max.	Unit
Interrupt Timing										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	35	—	40	ns
tINR	Interrupt Reset Time	—	20	—	25	—	35	—	40	ns

2690 tbl 12

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (SA or LA).

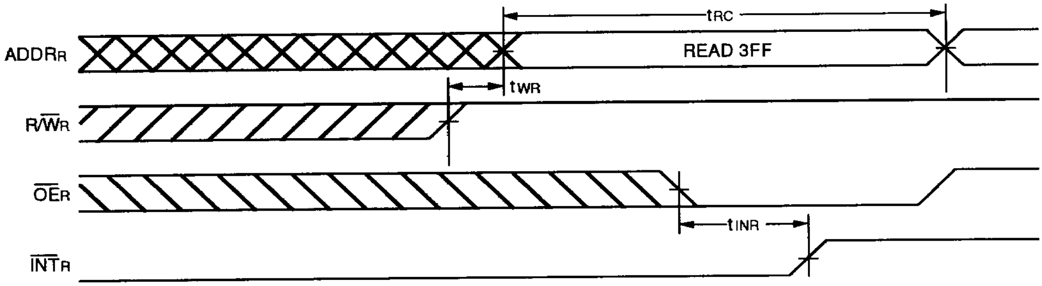
TIMING WAVEFORM OF INTERRUPT MODE(1,2)

LEFT SIDE SETS $\overline{\text{INT}}_R$:



2690 drw 16

RIGHT SIDE CLEARS $\overline{\text{INT}}_R$:



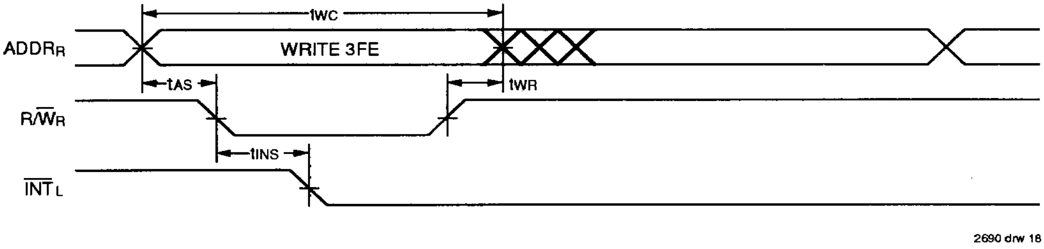
2690 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{\text{INT}}_L$ and $\overline{\text{INT}}_R$ are reset (high) during power up.

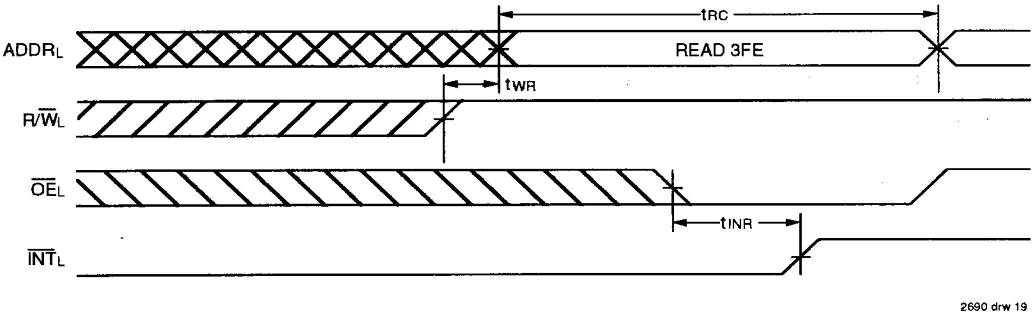
6-2-11

TIMING WAVEFORM OF INTERRUPT MODE(1,2)

RIGHT SIDE SETS $\overline{\text{INT}}_L$:

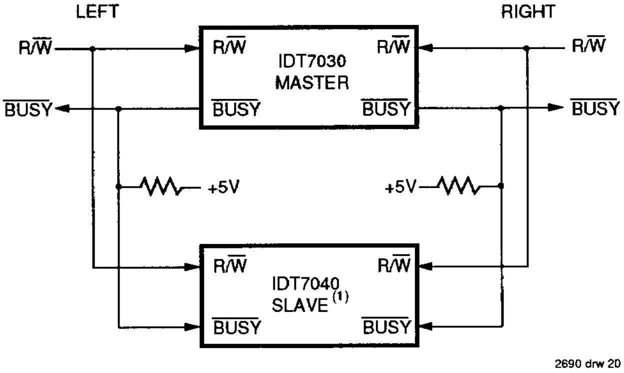


LEFT SIDE CLEARS $\overline{\text{INT}}_L$:



NOTES:
1. $\overline{\text{CE}}_L = \overline{\text{CE}}_R = V_{IL}$
2. $\overline{\text{INT}}_R$ and $\overline{\text{INT}}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT7040 (SLAVE). $\overline{\text{BUSY}}$-IN inhibits write in IDT7040 (SLAVE).

6-2-12

FUNCTIONAL DESCRIPTION

The IDT7030/IDT7040 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7030/IDT7040 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{\text{OE}}$). In the read mode, the port's $\overline{\text{OE}}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{\text{INT}}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{\text{INT}}$L) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE (HEX). Likewise, the right port interrupt flag ($\overline{\text{INT}}$R) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{\text{INT}}$R) the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{\text{BUSY}}$ flag will be set for the delayed port.

The $\overline{\text{BUSY}}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{\text{BUSY}}$ flag. $\overline{\text{BUSY}}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the port that has $\overline{\text{BUSY}}$ set LOW. The delayed port will have access when $\overline{\text{BUSY}}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{\text{CE}}$, on-chip control logic arbitrates between $\overline{\text{CE}}$L and $\overline{\text{CE}}$R for access; or (2) if the $\overline{\text{CE}}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{\text{BUSY}}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{\text{BUSY}}$L while another acitivates its $\overline{\text{BUSY}}$R signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMS must be delayed, until after the $\overline{\text{BUSY}}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{\text{BUSY}}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{\text{BUSY}}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL$^{(4)}$

Left or Right Port$^{(1)}$				Function
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory $^{(2}$
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port $^{(3)}$
H	L	H	Z	High Impedance Outputs

NOTES:
2690 tbl 13

1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG$^{(1,4)}$

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L$^{(2)}$	Set Right INTR Flag
X	X	X	X	X	X	L	L	3FF	H$^{(3)}$	Reset Right INTR Flag
X	X	X	X	L$^{(3)}$	L	L	X	3FE	X	Set Left INTL Flag
X	L	L	3FE	H$^{(2)}$	X	X	X	X	X	Reset Left INTL Flag

NOTES:
2690 tbl 14

1. Assume $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

TABLE II – ARBITRATION$^{(1,2)}$

Left Port		Right Port		Flags$^{(1)}$		Function
$\overline{CE}_L$	$A_{0L}-A_{9L}$	$\overline{CE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠A0R-A9R	L	≠A0L-A9L	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	=A0R-A9R	LL5R	=A0L-A9L	H	L	L-Port Wins
RL5L	=A0R-A9R	RL5L	=A0L-A9L	L	H	R-Port Wins
LW5R	=A0R-A9R	LW5R	=A0L-A9L	H	L	Arbitration Resolved
LW5R	=A0R-A9R	LW5R	=A0L-A9L	L	H	Arbitration Resolved

NOTES:
2690 tbl 15

1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH. LV5R = Left Address Valid ≥ 5ns before right address. RV5L = Right Address Valid ≥ 5ns before left address. Same = Left and Right Addresses match within 5ns of each other. LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$. RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$. LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

6-2-14