DESCRIPTION

This family is a 16M bit dynamic RAM organized 4,194,304 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended data out mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60, 70 or 80ns) and refresh cycle(2K ref. or 4K ref.) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Extended data out operation
- Read-modify-write Capability
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- JEDEC standard pinout
- 24/26-pin Plastic SOJ (300mil)
  24/26-pin Plastic TSOP-II (300mil)
- Single power supply of 3.3V ± 0.3V
- Early write or output enable controlled write

- Max. Active power dissipation

Speed	2K refresh	4K refresh
60	432mW	324mW
70	360mW	288mW
80	324mW	252mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	18ns	30ns
80	80ns	20ns	35ns

- Refresh cycle

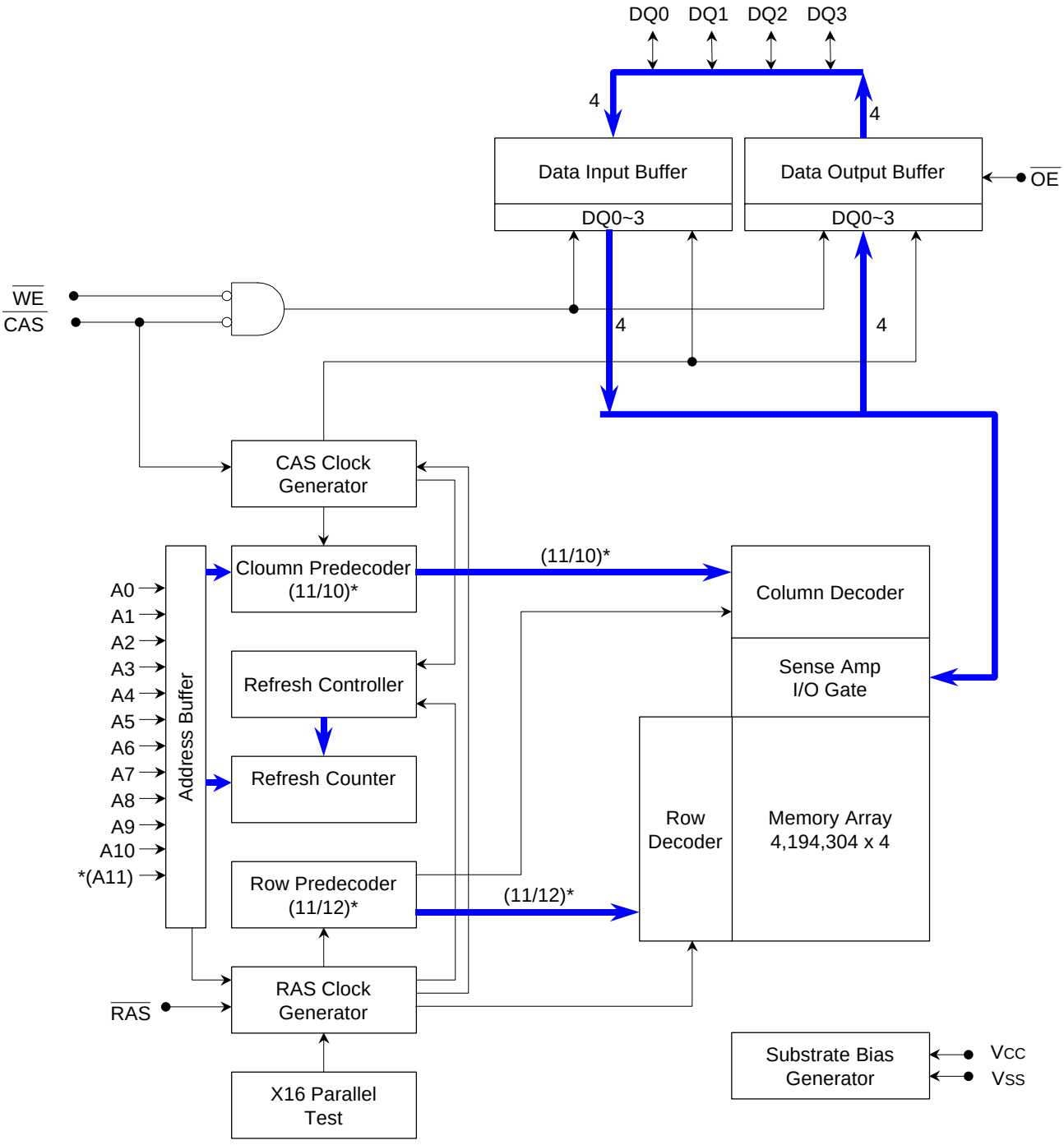
Part number	Refresh	Normal	SL-part
HY51V17404C	2K	32ms	256ms
HY51V16404C	4K	64ms	

ORDERING INFORMATION

Part Name	Refresh	Power	Package
HY51V17404CJ	2K		24/26Pin SOJ
HY51V17404CSLJ	2K	SL-part	24/26Pin SOJ
HY51V17404CT	2K		24/26Pin TSOP-II
HY51V17404CSLT	2K	SL-part	24/26Pin TSOP-II
HY51V16404CJ	4K		24/26Pin SOJ
HY51V16404CSLJ	4K	SL-part	24/26Pin SOJ
HY51V16404CT	4K		24/26Pin TSOP-II
HY51V16404CSLT	4K	SL-part	24/26Pin TSOP-II

*SL : Low power with self refresh

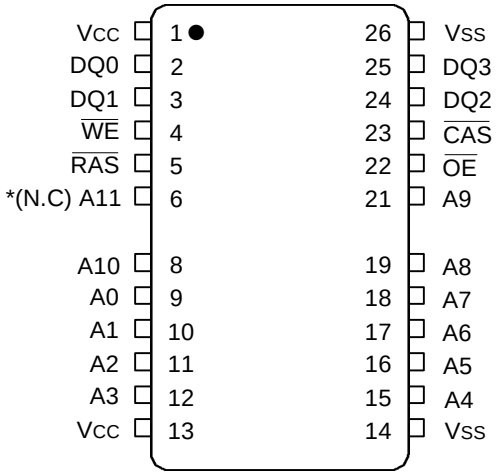
FUNCTIONAL BLOCK DIAGRAM



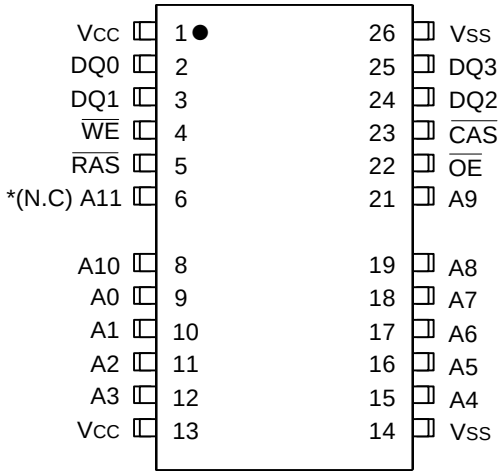
*(A11) for 4K refresh part

(2K Refresh / 4K Refresh)*

PIN CONFIGURATION (Marking Side)



24/26Pin Plastic SOJ (300mil)



24/26Pin Plastic TSOP-II (300mil)

(N.C)* : For 2K refresh product

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A11	Address Input (4K Refresh Product)
A0~A10	Address Input (2K Refresh Product)
DQ0~DQ3	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTIC

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current (Any input)	$V_{SS} \le V_{IN} \le V_{CC}$ + 0.3 All other pins not under test = V_{SS}	-10	10	µA
I_{LO}	Output Leakage Current (Any input)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS & /CAS at V_{IH}	-10	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA	2.4	-	V

DC CHARACTERISTICS

(T_A = 0°C to 70°C , V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max. Current		Unit
				2K Ref	4K Ref	
I_{CC1}	Operating Current	/RAS, /CAS Cycling t_{RC} = $t_{RC(min.)}$	60 70 80	120 100 90	90 80 70	mA
I_{CC2}	LVTTL Standby Current	/RAS, /CAS ≥ V_{IH} Other inputs ≥ V_{SS}	 SL-part	1 1	1 1	mA
I_{CC3}	/RAS-only Refresh Current	/RAS Cycling,/CAS = V_{IH} t_{RC} = $t_{RC(min.)}$	60 70 80	120 100 90	90 80 70	mA
I_{CC4}	EDO mode Current	/CAS Cycling, /RAS = V_{IL} t_{HPC} = $t_{HPC(min.)}$	60 70 80	110 90 80	80 70 60	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	 SL-part	500 200	500 200	µA µA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V t_{RC} = $t_{RC(min.)}$	60 70 80	120 100 90	90 80 70	mA
I_{CC7}	Battery Back-up Current (SL-part)	t_{RC}=125µs (2K Ref), 62.5µs (4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE = V_{CC} - 0.2V Address = Vcc-0.2V or 0.2V DQ0~DQ3 = Vcc-0.2, 0.2V or Open	tRAS ≤ 300ns	300	300	µA
			tRAS ≤ 1µs	500	500	
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I_{CC7}		300	300	µA

Note

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{HPC}).
2. Specified values are obtained with output unloaded.
3. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} within one EDO mode cycle time t_{HPC}.
4. Only /RAS(max.) = 1µs is applied to refresh of battery backup but tRAS(max.) = 10µs is to applied to normal functional operation.
5. Icc5(max.) = 200µA, Icc7 and Icc8 are applied to SL-part only.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 3.3V ± 0.3V , V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random read or write cycle time	104	-	124	-	144	-	ns	
t_{RWC}	Read-modify-write cycle time	137	-	160	-	187	-	ns	
t_{HPC}	EDO mode cycle time	25	-	30	-	35	-	ns	2
t_{HPRWC}	EDO mode read-modify-write cycle time	70	-	78	-	90	-	ns	2
t_{RAC}	Access time from /RAS	-	60	-	70	-	80	ns	5,6,7
t_{CAC}	Access time from /CAS	-	15	-	18	-	20	ns	5,6
t_{AA}	Access time from column address	-	30	-	35	-	40	ns	5,7
t_{CPA}	Access time from column precharge	-	35	-	40	-	45	ns	5
t_{CLZ}	/CAS to output low impedance	3	-	3	-	3	-	ns	5
t_{CEZ}	Output buffer turn-off delay from /CAS	3	15	3	18	3	20	ns	8
t_T	Transition time(rise and fall)	2	50	2	50	2	50	ns	3
t_{RP}	/RAS precharge time	40	-	50	-	60	-	ns	
t_{RAS}	/RAS pulse width	60	10K	70	10K	80	10K	ns	
t_{RASP}	/RAS pulse width(EDO mode)	60	200K	60	200K	70	200K	ns	
t_{RSH}	/RAS hold time	15	-	18	-	20	-	ns	
t_{CSH}	/CAS hold time	45	-	50	-	55	-	ns	
t_{CAS}	/CAS pulse width	11	10K	14	10K	17	10K	ns	
t_{RCD}	/RAS to /CAS delay time	20	45	20	52	20	60	ns	6
t_{RAD}	/RAS to column address delay time	15	30	15	35	17	40	ns	7
t_{CRP}	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	11
t_{CP}	/CAS precharge time	10	-	12	-	12	-	ns	
t_{ASR}	Row address set-up time	0	-	0	-	0	-	ns	
t_{RAH}	Row address hold time	10	-	10	-	12	-	ns	
t_{ASC}	Column address set-up time	0	-	0	-	0	-	ns	
t_{CAH}	Column address hold time	10	-	15	-	15	-	ns	
t_{RAL}	Column address to /RAS lead time	30	-	35	-	40	-	ns	
t_{RCS}	Read command set-up time	0	-	0	-	0	-	ns	
t_{RCH}	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	9
t_{RRH}	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	9
t_{WCH}	Write command hold time	10	-	10	-	15	-	ns	
t_{WP}	Write command pulse width	10	-	10	-	15	-	ns	
t_{RWL}	Write command to /RAS lead time	12	-	12	-	17	-	ns	
t_{CWL}	Write command to /CAS lead time	12	-	12	-	17	-	ns	

AC CHARACTERISTICS

Continued

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tDS	Data-in set-up time	0	-	0	-	0	-	ns	10
tDH	Data-in hold time	10	-	10	-	10	-	ns	10
tREF	Refresh period(2048 cycles)	-	32	-	32	-	32	ms	
	Refresh period(4096 cycles)	-	64	-	64	-	64	ms	
	Refresh period(SL-part)	-	256	-	256	-	256	ms	
tWCS	Write command set-up time	0	-	0	-	0	-	ns	11
tCWD	/CAS to /WE delay time	34	-	40	-	44	-	ns	11
tRWD	/RAS to /WE delay time	79	-	92	-	104	-	ns	11
tAWD	Column address to /WE delay time	49	-	57	-	64	-	ns	11
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	
tCHR	/CAS hold time(CBR cycle)	10	-	10	-	10	-	ns	
tRPC	/RAS to /CAS precharge time	5	-	5	-	5	-	ns	
tCPT	/CAS precharge time(CBR counter test)	20	-	25	-	25	-	ns	
tROH	/RAS hold time referenced to /OE	10	-	10	-	10	-	ns	
tOEA	/OE access time	-	15	-	18	-	20	ns	
tOED	/OE to data delay time	15	-	18	-	20	-	ns	
tOEZ	Output buffer turn-off delay time from /OE	3	15	3	18	3	20	ns	8
tOEH	/OE command hold time	15	-	18	-	20	-	ns	
tCPWD	/WE delay time from /CAS precharge	54	-	62	-	69	-	ns	11
tRHCP	/RAS hold time from /CAS precharge	35	-	40	-	45	-	ns	
tWRP	/WE to /RAS precharge time(CBR cycle)	10	-	10	-	10	-	ns	
tWRH	/WE to /RAS hold time(CBR cycle)	10	-	10	-	10	-	ns	
tRASS	/RAS pulse width(self refresh)	100K	-	100K	-	100K	-	ns	
tRPS	/RAS Precharge Time (Self refresh)	110	-	130	-	150	-	ns	
tCHS	/CAS Hold Time (Self refresh)	-50	-	-50	-	-50	-	ns	
tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
tREZ	Output Buffer Turn Off Delay Time from /RAS	3	15	3	18	3	20	ns	
tWEZ	Output Buffer Turn Off Delay Time from /WE	3	15	3	18	3	20	ns	
tWED	/WE to Data Delay Time	15	-	18	-	20	-	ns	
tOEP	/OE Precharge Time	5	-	5	-	5	-	ns	
tWPE	/WE Pulse Width (EDO cycle)	5	-	5	-	5	-	ns	
tOCH	/OE to /CAS Hold Time	5	-	5	-	5	-	ns	
tCHO	/CAS Hold Time to /OE	5	-	5	-	5	-	ns	

TEST MODE

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tRC	Random read or write cycle time	109	-	129	-	149	-	ns	
tRWC	Read-modify-write cycle time	142	-	165	-	192	-	ns	
tHPC	EDO mode cycle time	30	-	35	-	40	-	ns	2
tHPRWC	EDO mode read-modify-write cycle time	75	-	83	-	95	-	ns	2
tRAC	Access time from /RAS	-	65	-	75	-	85	ns	5,6,7
tCAC	Access time from /CAS	-	20	-	23	-	25	ns	5,6
tAA	Access time from column address	-	35	-	40	-	45	ns	5,7
tCPA	Access time from column precharge	-	40	-	45	-	50	ns	5
tRAS	/RAS pulse width	65	10K	75	10K	85	10K	ns	
tRASP	/RAS pulse width(EDO mode)	65	200K	75	200K	85	200K	ns	
tRSH	/RAS hold time	20	-	23	-	25	-	ns	
tCSH	/CAS hold time	50	-	55	-	60	-	ns	
tCAS	/CAS pulse width	16	10K	19	10K	22	10K	ns	
tRAL	Column address to /RAS lead time	35	-	40	-	45	-	ns	
tCWD	/CAS to /WE delay time	39	-	45	-	49	-	ns	11
tRWD	/RAS to /WE delay time	84	-	97	-	109	-	ns	11
tAWD	Column address to /WE delay time	54	-	62	-	69	-	ns	11
tOEA	/OE access time	-	20	-	23	-	25	ns	
tOED	/OE to data delay Time	20	-	23	-	25	-	ns	
tOEH	/OE command hold time	20	-	23	-	25	-	ns	
tCPWD	/WE delay time from /CAS precharge	59	-	67	-	74	-	ns	11

In test mode, data are written into 16 sectors (each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4sectors connected to one DQ pin are equal (all `1`s or `0`s), the DQ pin indicates a `1`. If they are not equal, the DQ indicates a `0`. The 4Mx4 DRAM can be tested in the same way as a 1Mx4 DRAM is tested.

/WE (when in /CAS-before-/RAS cycle) puts the 4Mx4 DRAM into Test Mode and a /CAS-before-/RAS or a /RAS-only refresh cycle put it back into Normal Mode. /WE (when in /CAS-before-/RAS cycle) shall be used for the refresh operation in the test mode. The test mode function reduces test time(1/4 in case of N test pattern).

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. $t_{ASC} \geq t_{CP}$(min), assume t_T=2ns.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA=0 to 70¡ ℃) is assured.
5. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 1TTL loads and 100pF.
6. Operation within the $t_{RCD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
7. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
8. t_{WEZ}, t_{REZ}, t_{CEZ} and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. If /RAS goes to high before /CAS high going,the open circuit condition of the output is achieved by /CAS high going. If /CAS goes to high before /RAS high going,the open circuit condition of the output is achieved by /RAS high going.

CAPACITANCE

(T_A = 25°C, V_{CC} =3.3V ± 0.3V, V_{SS} = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Input Capacitance (A0~A11)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input / Output Capacitance (DQ0~DQ3)	-	7	pF