GET-30749, Revision C

NEC Corporation
Tamagawa Plant
1753,Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa, 211-8666

Specification Control Drawing of Grade L GaAs Devices for Satellite Applications

Prepared on: September 28, 2000

Prepared by: Masahito Kushima

Masahito Kushima

Assistant Manager
Compound Semiconductor Department
Compound Semiconductor Device Division
IC & Discrete Operations Unit

Approved by: Yasuo Saitoh

Yasuo Saitoh

Manager
Compound Semiconductor Department
Compound Semiconductor Device Division
IC & Discrete Operations Unit

Approved by: Akira Mochizuki

Akira Mochizuki

Manager
Reliability & Quality Control Department
Compound Semiconductor Device Division
IC & Discrete Operations Unit

Table of Content

Introduction

NEC has decided to introduce a new reliability grade for satellite applications, Grade L microwave semiconductors.

The emerging markets of commercial satellites for satellite-based digital communications require cost reduction and fast delivery. To comply with such requests, Grade L devices with reduced screening, inspection to MIL-PRF-19500 are available. This is accomplished by eliminating non-value added tests and is supported by NEC' outstanding quality record in high reliability devices.

1.0 Scope

This Drawing establishes the requirements for GaAs Devices for use in commercial satellite communications. The devices are generally suitable for use in high reliability space applications.

2.0 Applicable Documents

The following documents of this issue in effect on date of invitation for bits or requests for quotation form a part of this drawing to extent specified herein.

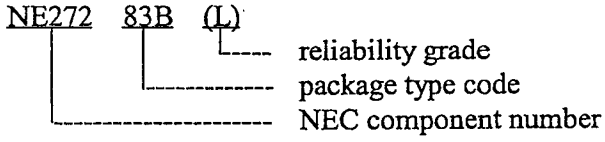
MIL-STD-750	Military Standard, Test Methods for Semiconductor Devices
MIL-STD-883	Test Methods and Procedure for Microelectronics
GET-30484	Internal Visual Inspection (Low Noise GaAs FET)
GET-30447	Internal Visual Inspection (GaAs MMIC)

3.0 Requirements/Specifications

3.1 Available Parts Number List

Available part numbers are shown in Table 1.

The NEC part number consists of NEC component number, package type code, reliability grade, as shown in the following example:



3.2 Absolute Maximum Ratings

Absolute maximum ratings shall be as satisfied in Table 2.

3.3 Design and Construction

Design and Construction shall be as satisfied in Table 3.

3.4 Performance

The performance, Group A test shall be as specified in Table 4.

3.5 Package Outline

The package outline shall be as specified in Fig.1.

3.6 Chip Drawing

The chip drawing shall be as specified in Fig.2.

3.7 Marking (Packaged Devices)

Marking shall consist of NEC's name or symbol and part number as a minimum. Parts numbers for marking are showing in Table 1 and Fig.1.

4.0 Quality Assurance Provisions

4.1 Processing Flow Diagrams ---- Chips and Packaged Devices

The quality assurance provisions shall be in accordance with Processing Flow Diagrams, Fig.3.

4.2 Preconditioning

Devices supplied to this Drawing shall be subjected to and pass the screening tests according to Table 5.

Grade L devices are characterized by the following items;

a. Internal visual (Pre-Seal) inspection and Final Inspection (Data Review Prior to shipment) are not applicable.

b. Group B Tests (Lot Acceptance Tests) are not applicable. Wafer Acceptance Tests (WAT) are performed every wafer at one time. Test samples are not shipped.

c. Test Report is optional, any other option is not applicable.

4.3 Electrical Performance, Delta Parameter and Criteria

The performance requirements shall be as specified in Table 4. Unless otherwise specified, the operating parameters apply for all specified operating environmental conditions, and over the full specified operating temperature range. High and low temperature test is not applicable.

4.4 Documentation Submittal

The following data shall accompany the parts shipment.

a. Shipping Document includes
   - Customer's purchase order number.
   - NEC's name and part number.
   - Lot identification code.
   - Quantity shipped.

b. Certificate of Conformance

c. Serial Number List (Packaged Device)

d. Test Report (Option) includes
   - Summary sheet
   - Bond pull test data
   - Group A test data
   - Power burn-in delta data

5.0 Preparation For Delivery

5.1 Packaging

Each devise shall be individually packaged in separate or separable containers. The individual component containers (unit packages) shall provide adequate protection from contamination and physical damage encountered in normal handling and storage.

5.2 Marking

Marking shall consists of the following:

a. Carriers containing chips:
   - NEC's name or symbol.
   - NEC's part number.
   - Customer's purchase order number.
   - Wafer lot identification code.

b. Unit packages
   - NEC's name or symbol.
   - NEC's part number.
   - Serial number (Unit package)
   - Customer's purchase order number.
   - Wafer lot identification code.
   - Inspection lot identification code (Unit package)

Table 1 Available Parts Number and Marking

Part Number	Rank	Function	Form	Package	Marking
NE24283B(L)	—	Low Noise HJ FET	packaged	83B	242
NE24200(L)	—		chip	—	———
NE27283B(L)	—		packaged	83B	272
NE27200(L)	—		chip	—	———
NE23383B(L)	—		packaged	83B	233
NE23300(L)			chip	—	———
NE29200(L)	—		chip	—	292
NE67483B(L)	—	Low Noise MES FET	packaged	83B	674
	N				
	M				
	L				
NE67400(L)	—		chip	—	———
	N				
	M				
	L				
uPG100B(L)	—	MMIC - Wide Band Amplifier	packaged	T-31	G100, Lot Code
uPG100P(L)	—		chip	—	———
uPG101B(L)	—		packaged	T-31	G101, Lot Code
uPG101P(L)	—		chip	—	———

Table 2-1 Absolute Maximum Ratings(Ta=25°C)

Part No.	Parameter		Symbol	Ratings	Unit
NE242	Drain to Source Voltage		VDS	4.0	V
NE272	Gate to Drain Voltage		VGD	-3.0	V
NE233	Gate to Source Voltage		VGS	-3.0	V
	Drain Current		ID	IDSS	mA
	RF Input(CW)		Pin	+15	dBm
	Total Power Dissipation	Packaged	Ptot	165	mW
		Chip		200	mW
	Thermal resistance	Packaged	Rth	350	°C/W
		Chip		260	°C/W
	Channel Temperature		Tch	175	°C
	Storage Temperature		Tstg	-65 to +175	°C
NE29200	Drain to Source Voltage		VDS	4.0	V
	Gate to Drain Voltage		VGD	-3.0	V
New	Gate to Source Voltage		VGS	-3.0	V
	Drain Current		ID	IDSS	mA
	RF Input(CW)		Pin	+0	dBm
	Total Power Dissipation		Ptot	200	mW
	Thermal resistance		Rth	260	°C/W
	Channel Temperature		Tch	175	°C
	Storage Temperature		Tstg	-65 to +175	°C
NE674	Drain to Source Voltage		VDS	5.0	V
	Gate to Drain Voltage		VGD	-6.0	V
	Gate to Source Voltage		VGS	-5.0	V
	Drain Current		ID	IDSS	mA
	RF Input(CW)		Pin	+15	dBm
	Total Power Dissipation	Packaged	Ptot	270	mW
		Chip		400	mW
	Thermal Resistance	Packaged	Rth	450	°C/W
		Chip		190	°C/W
	Channel Temperature		Tch	175	°C
	Storage Temperature		Tstg	-65 to +175	°C

Table 2-2 Absolute Maximum Ratings(Ta=25°C)

Part No.	Parameter	Symbol	Ratings	Unit
uPG100	Drain Voltage	VDD	+8.0	V
	Gate Voltage	VGG	-8.0	V
	Input Voltage	Vin	-3.0 to +0.6	V
	Input Power	Pin	+15	dBm
	Total Power Dissipation	Ptot	1.5	W
	Operating (Case) Temperature	Tc	-65 to +125	°C
	Storage Temperature	Tstg	-65 to +175	°C
uPG101	Drain Voltage	VDD	+10.0	V
	Gate Voltage	VGG	-8.0	V
	Input Voltage	Vin	-5.0 to +0.6	V
	Input Power	Pin	+15	dBm
	Total Power Dissipation	Ptot	1.5	W
	Operating (Case) Temperature	Tc	-65 to +125	°C
	Storage Temperature	Tstg	-65 to +175	°C

Table 3 Design and Construction

Part No.	Construction, Material	
NE242 NE272 NE233 NE674 NE292	Semiconductor Material	GaAs
	Source and Drain Metallization	Ni/AuGe/Au
	Gate Metallization	Ti/Al
	Bonding Pad Metallization	Ti/Pt/Au
	Back Side Metal	Ti/Pt/Au
	Glassivation	SiN
Packaged Device	Die-attach Material	AuSn
	Lid Seal	AuSn
	Bonding Wire	Au, 20um ϕ
	Package Material	Al_2O_3
	Package Lid	Al_2O_3
	Lead Material	Alloy 42(Ni/Au Plated)
uPG100 uPG101	Semiconductor Material	GaAs
	Source and Drain Metallization	Ni/AuGe
	Gate Metallization	WSi
	Bonding Pad Metallization	Ti/Pt/Au
	Back Side Metal	Ti/Pt/Au
	Glassivation	SiN
Packaged Device	Die-attach Material	AuSn
	Lid Seal	AuSn
	Bonding Wire	Au, 30um ϕ
	Package Material	Al_2O_3
	Package Lid	Al_2O_3
	Lead Material	Cu clad Fe (Ni/Au Plated)

Table 4-1 Electrical Characteristics, Delta Parameters and Criteria(Low Noise FET)

Ta=25°C

Part No.	Parameter	Test Condition	Limits		units	Delta Limits
			Min.	Max.		
NE24283B(L) NE24200(L)	IDSS	VDS=2V,VGS=0V	15	70	mA	±10%
	gm	VDS=2V,IDS=10mA	45	-	mS	±10%
	Vp	VDS=2V,IDS=100uA	-2.0	-0.2	V	±10%
	IGSO	VGS=-3V,IDS=0A	-	10	uA	+100nA or +100%*
	NF	VDS=2V,IDS=10mA, f=12GHz	-	0.70	dB	- (Group A only)
	Ga		10.0	-	dB	- (Group A only)
NE27283B(L) NE27200(L)	IDSS	VDS=2V,VGS=0V	20	90	mA	±10%
	gm	VDS=2V,IDS=10mA	45	-	mS	±10%
	Vp	VDS=2V,IDS=100uA	-2.0	-0.2	V	±10%
	IGSO	VGS=-3V,IDS=0A	-	10	uA	+100nA or +100%*
	NF	VDS=2V,IDS=10mA, f=12GHz	-	0.55	dB	- (Group A only)
	Ga		11.0	-	dB	- (Group A only)
NE23383B(L) NE23300(L)	IDSS	VDS=2V,VGS=0V	15	80	mA	±10%
	gm	VDS=2V,IDS=10mA	45	-	mS	±10%
	Vp	VDS=2V,IDS=100uA	-2.0	-0.2	V	±10%
	IGSO	VGS=-3V,IDS=0A	-	10	uA	+100nA or +100%*
	NF	VDS=2V,IDS=10mA, f=12GHz	-	1.0	dB	- (Group A only)
	Ga		9.5	-	dB	- (Group A only)
NE67483B(L) NE67400(L)	IDSS	VDS=3V,VGS=0V	20	120	mA	±10%
		Rank N	20	50	mA	±10%
		Rank M	50	80	mA	±10%
		Rank L	80	120	mA	±10%
	gm	VDS=3V,IDS=10mA	20	-	mS	±10%
	Vp	VDS=3V,IDS=100uA	-3.5	-0.5	V	±10%
	IGSO	VGS=-3V,IDS=0A	-	10	uA	+100nA or +100%*
	NF	VDS=3V,IDS=10mA, f=12GHz	-	1.6	dB	- (Group A only)
	Ga		8.5	-	dB	- (Group A only)

*whichever is greater

Table 4-2 Electrical Characteristics, Delta Parameters and Criteria(Low Noise FET)

Ta=25°C

Part No.	Parameter	Test Condition	Limits		units	Delta Limits
			Min,	Max		
NE29200(L)	IDSS	VDS=2V,VGS=0V	15	70	mA	±10%
	gm	VDS=2V,IDS=10mA	40	-	mS	±10%
	Vp	VDS=2V,IDS=100uA	-2.0	-0.2	V	±10%
	IGSO	VGS=-3V,IDS=0A	-	10	uA	+100nA or +100%*
	NF	VDS=2V,IDS=10mA,	-	0.45	dB	- (Group A only)
	Ga	f=12GHz	12.0	-	dB	- (Group A only)

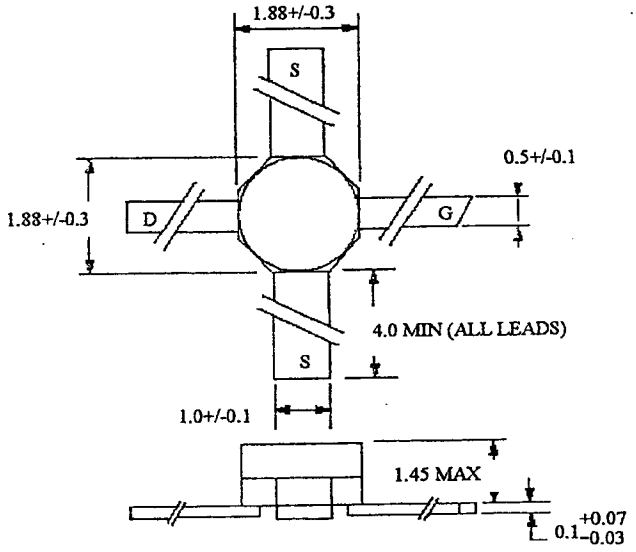
*whichever is greater

Table 4-3 Electrical Characteristics, Delta Parameters and Criteria(MMIC - Amplifier)

Ta=25°C

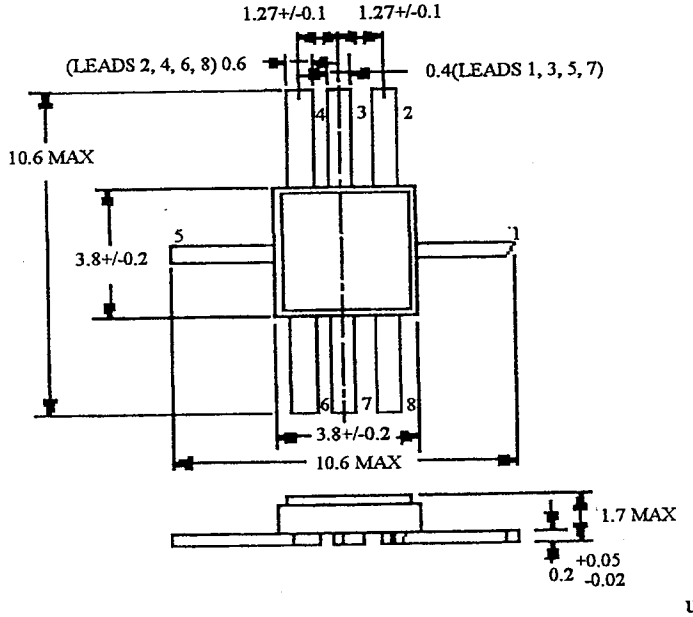
Part No.	Parameter	Test Condition	Limits		units	Delta Limits
			Min,	Max		
UPG100B(L) UPG100P(L)	IDD	VDD=+5.0V,	30	60	mA	±10%
	IGG	VGG=-5.0V	-	1.5	mA	-
	Gp	VDD=+5.0V, VGG=-5.0V f=0.05 to 3.0GHz* ZS=ZL=50 Ω	14	-	dB	- (Group A only)
	Delta Gp		-	±1.5	dB	- (Group A only)
	P1dB		+3	-	dBm	- (Group A only)
	NF		-	3.5	dB	- (Group A only)
	RLin		7	-	dB	- (Group A only)
	RLout		7	-	dB	- (Group A only)
	ISOL		30	-	dB	- (Group A only)
UPG101B(L) UPG101P(L)	IDD	VDD=VOUT=+8.0V,	70	140	mA	±10%
	IGG	VGG=-5.0V	-	3.0	mA	-
	Gp	VDD=VOUT=+8.0V, VGG=-5.0V f=0.05 to 3.0GHz* ZS=ZL=50 Ω	12	-	dB	- (Group A only)
	Delta Gp		-	±1.5	dB	- (Group A only)
	P1dB		+16	-	dBm	- (Group A only)
	NF		-	7.0	dB	- (Group A only)
	RLin		6	-	dB	- (Group A only)
	RLout		6	-	dB	- (Group A only)
	ISOL		30	-	dB	- (Group A only)

** measurements @1.0, 1.5, 2.0, 2.5, 3.0GHz.



units in mm

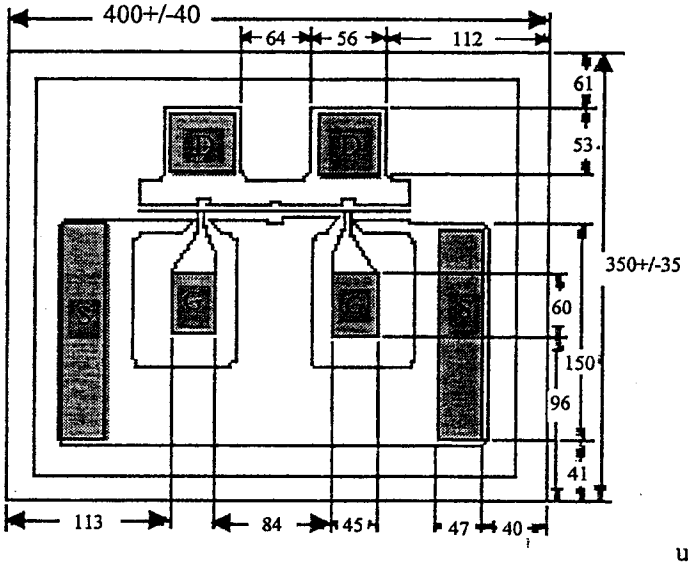
Fig.1-1 Package Outline - 83B



PIN CONNECTIONS
1.INPUT
2.GND
3.VGG
4.GND
5.OUTPUT
6.GMD
7.VDD
8.GND

units in mm

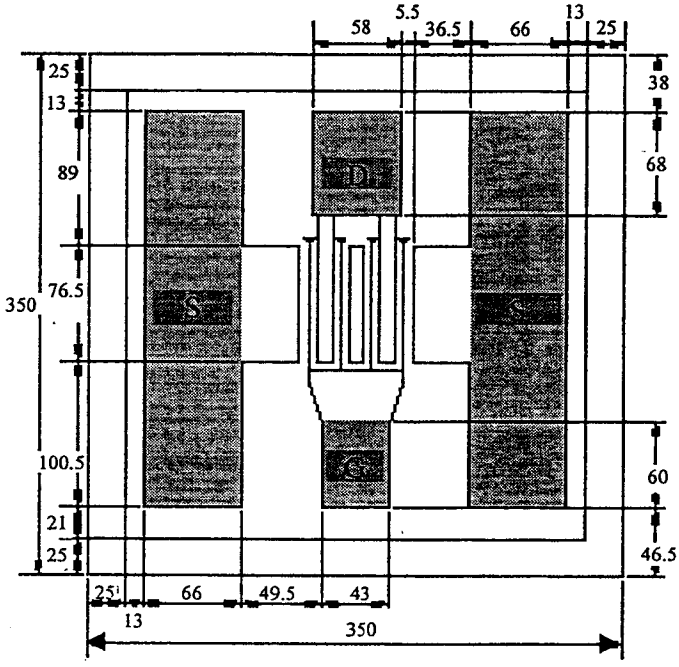
Fig.1-2 Package Outline - T-31



units in um

chip thickness=140um+/-10um

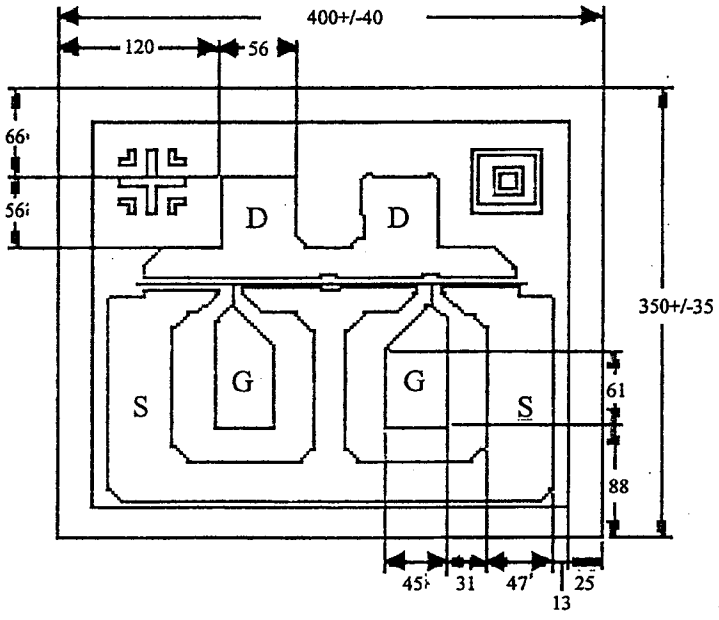
Fig.2-1 Chip Outline - NE24200



units in um

chip thickness=140um+/-10um

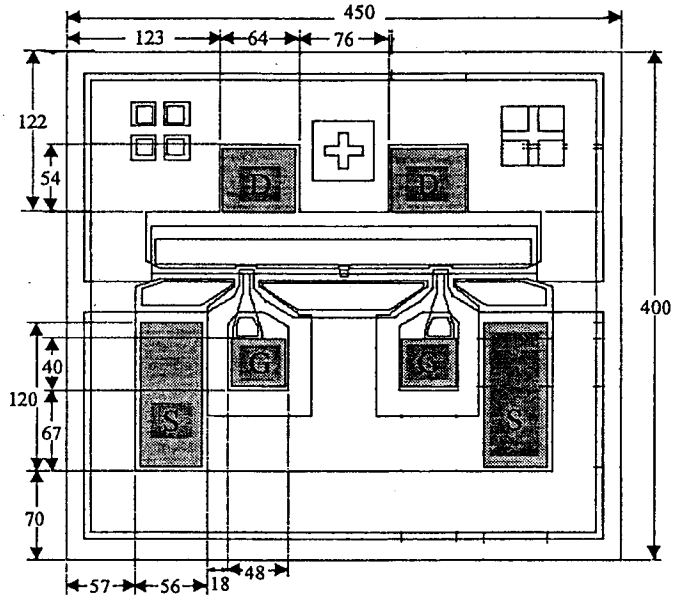
Fig.2-2 Chip Outline - NE27200



units in um

chip thickness=140um+/-10um

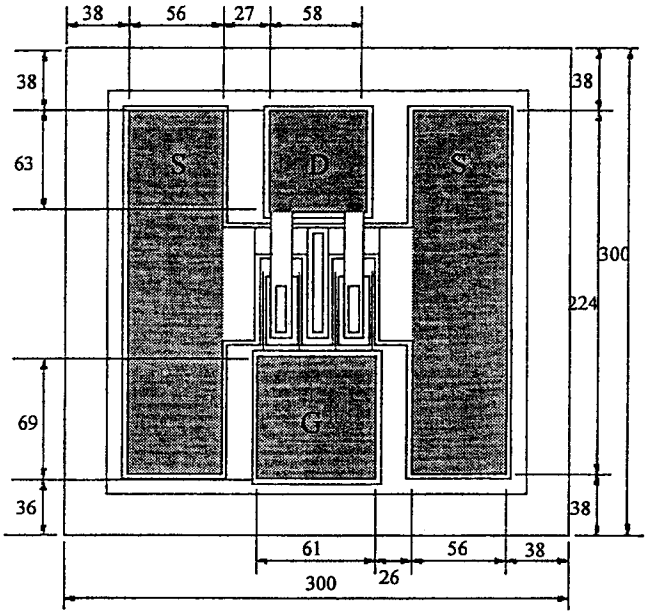
Fig.2-3 Chip Outline - NE23300



units in um

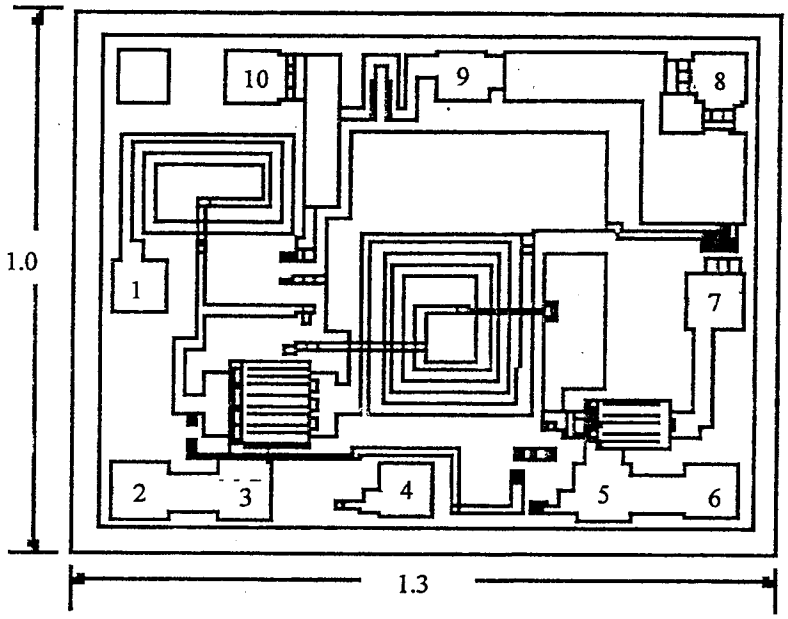
chip thickness=140um+/-10um

Fig.2-4 Chip Outline - NE67400



chip thickness=140um+/-10um

Fig.2-5 Chip Outline - NE29200

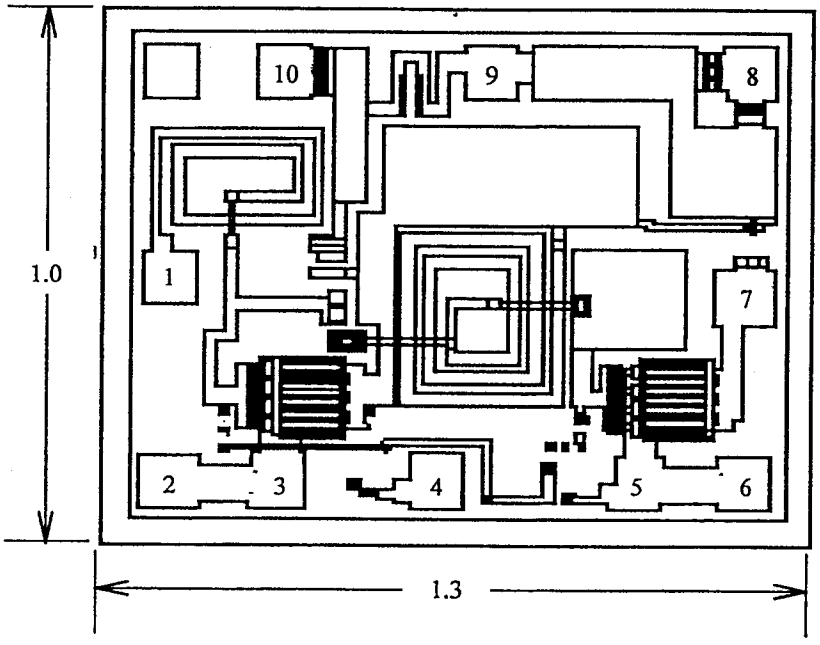


1.INPUT
2.GND
3.GND
4.VGG
5.GND
6.GND
7.OUTPUT
8.GND
9.VDD
10.GND

units in mm

chip thickness=140um+/-10um, bonding pad size : 100um x 100um

Fig.2-6 Chip Outline - uPG100P



1.INPUT
2.GND
3.GND
4.VGG
5.GND
6.GND
7.OUTPUT
8.GND
9.VDD
10.GND

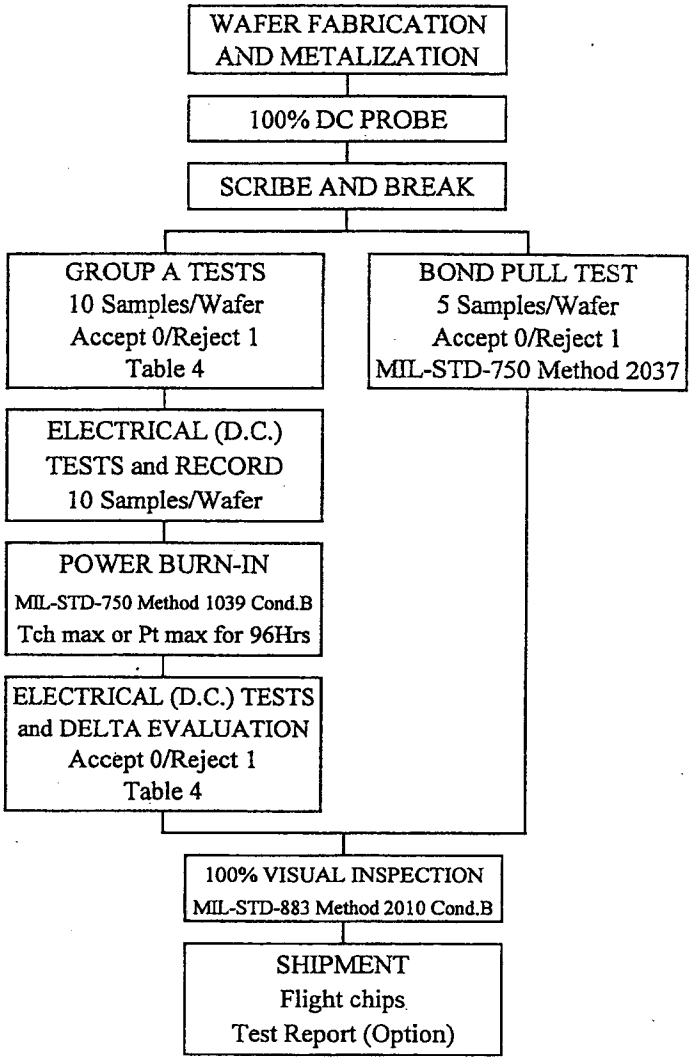
Units in mm

chip thickness=140um+/-10um, bonding pad size : 100um x 100um

Fig.2-7 Chip Outline - uPG101P

Low Noise GaAs FETs - Chips
Processing Flow Diagrams

Grade L

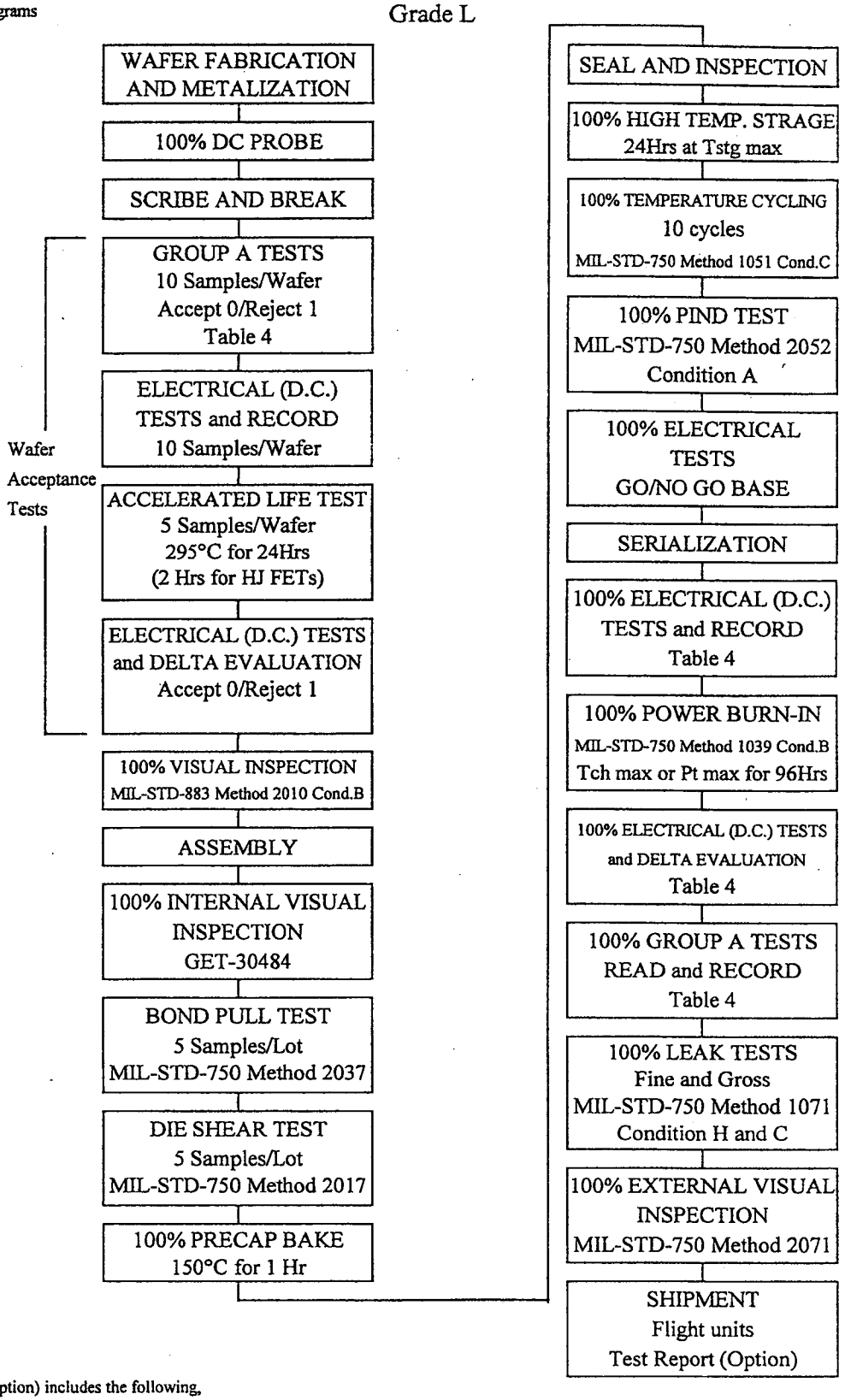


Note : Test Report(Option) includes the following,
- --- Summary Sheet
- --- Bond Pull Test Data
- --- Group A Test Data
- --- Power Burn-in Delta Data

Fig.3-1
Processing Flow Diagrams
Low Noise GaAs FETs - Chips

Low Noise GaAs FETs - Packaged Devices
Processing Flow Diagrams

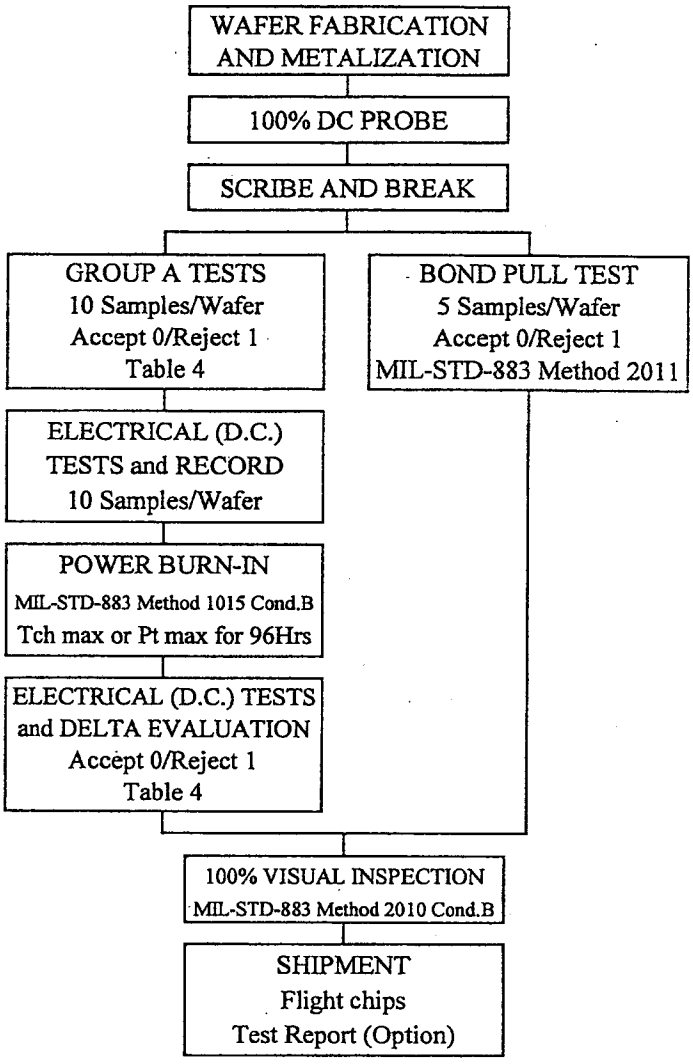
Grade L



Note : Test Report(Option) includes the following,
- Summary Sheet
- Bond Pull Test Data
- Group A Test Data
- Power Burn-in Delta Data

Fig.3-2
Processing Flow Diagrams
Low Noise GaAs FETs - Packaged Devices

Grade L

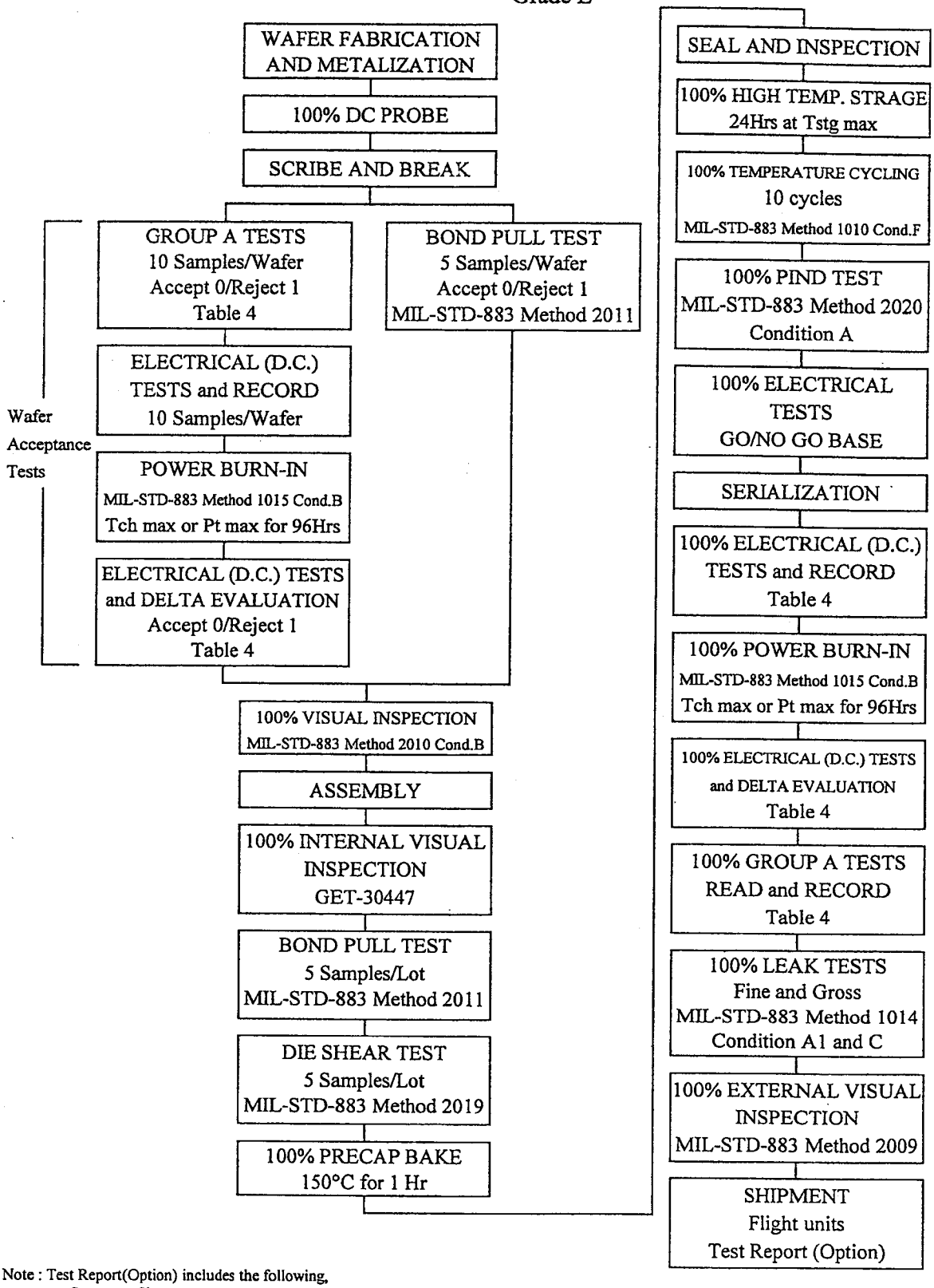


Note : Test Report(Option) includes the following,
- Summary Sheet
- Bond Pull Test Data
- Group A Test Data
- Power Burn-in Delta Data

Fig.3-3
Processing Flow Diagrams
GaAs MMICs - Chips

GaAs MMICs - Packaged Devices
Processing Flow Diagrams

Grade L



Note : Test Report(Option) includes the following,
- --- Summary Sheet
- --- Bond Pull Test Data
- --- Group A Test Data
- --- Power Burn-in Delta Data

Fig.3-4
Processing Flow Diagrams
GaAs MMICs - Packaged Devices

Table 5-1 Preconditioning and Screening for GaAs FET

Examination or Test	MIL-STD-750 METHOD	Condition	Reliability Grade
			GRADE L
Internal Visual(Precap) Inspection	2072	NEC Specification GET-30484(LN)	100%
Bond Strength	2037	Record Data	n=5
Die Shear	2017	Record Data	n=5*
Precap Bake		1 Hr at 150°C	100%
High Temperature Storage	1032	24Hrs min. at Tstg max.	100%
Temperature Cycling	1051	Condition C, 10cycles	100%
PIND	2052	Condition A, PDA in accordance with MIL-PRF-19500	100%
Electrical Test(Go/No Go)			100%
Serialization			100%
Electrical Test		Table 4, Record Data	100%
Power Burn-in	1039	Condition B, Tch max or Pt max. 96Hrs min for GRADE L	100%
Electrical Test		Table 4, Record Data	100%
Group A Test		Table 4, Record Data	100%
Leak Fine Gross	1071	Condition H Condition C	100%
External Visual Inspection	2071		100%

* Bond Strength samples are used for Die Shear Test.

Table 5-2 Preconditioning and Screening for GaAs MMIC

Examination or Test	MIL-STD-883 METHOD	Condition	Reliability Grade
			GRADE L
Internal Visual(Precap) Inspection	2010	NEC Specification GET-30447(MMIC)	100%
Bond Strength	2011	Record Data	n=5
Die Shear	2019	Record Data	n=5*
Precap Bake		1 Hr at 150 °C	100%
High Temperature Storage	1008	24Hrs min. at Tstg max.	100%
Temperature Cycling	1010	Condition F, 10cycles	100%
PIND	2020	Condition A, PDA in accordance with MIL-PRF-19500	100%
Electrical Test(Go/No Go)			100%
Serialization			100%
Electrical Test		Table 4, Record Data	100%
Power Burn-in	1015	Condition B, Tch max or Pt max. 96Hrs min for GRADE L	100%
Electrical Test		Table 4, Record Data	100%
Group A Test		Table 4, Record Data	100%
Leak Fine Gross	1014	Condition A1 Condition C	100%
External Visual Inspection	2009		100%

* Bond Strength samples are used for Die Shear Test.

RECORD OF REVISIONS

APPENDIX 1/2

TITLE	Specification Control Drowing of Grade L GaAs Devices for Satellite Applications	HEADING NUMBER	GET-30749

Rev.	REMARKS ON REVISION	
-	* Initial release.	DATE: July 16, 1998 DEPT.: CSD, CSDD MADE BY: M.Kushima / CHKD BY: / APP.BY: F.Emori SIGNATURE OF APPROVAL R&QC: / / A.Mochizuki: / /
A	* Added the following IDSS Rank on NE67483B(L) and NE67400(L), Rank N : 20mA- 50mA, Rank M : 50mA- 80mA Rank L : 80mA-120mA * Corrected Table 5-2 Method Numbers on page 20 as follows, (1)Internal Visual(Precap) Imspection, Methd 2010 (2)PIND, Method 2020 * Corrected MIL-S-19500 to MIL-PRF-19500 on Table 5-1 and 5-2.	DATE: October 19, 1998 DEPT.: CSD, CSDD MADE BY: M.Kushima / CHKD BY: / APP.BY: F.Emori SIGNATURE OF APPROVAL R&QC: / / A.Mochizuki: / /
B	* Added uPG101B(L),uPG101P(L),uPG501B(L),uPG501P(L), uPG503B(L),uPG503P(L),uPG506B(L) and uPG506P(L).	DATE: December 8, 1998 DEPT.: CSD, CSDD MADE BY: M.Kushima / CHKD BY: / APP.BY: F.Emori SIGNATURE OF APPROVAL R&QC: / / A.Mochizuki: / /

RECORD OF REVISIONS

APPENDIX 2/2

TITLE	Specification Control Drowing of Grade L GaAs Devices for Satellite Applications	HEADING NUMBER	GET-30749

Rev.	REMARKS ON REVISION
C	* Added NE29200 (L).
	* Changed the delta criteria of NE674 as follows,
	Delta IDSS = from +/ - 15% to +/ - 10%
	Delta Vp = from +/ - 15% to +/ - 10%
	* Deleted uPG501B(L),uPG501P(L), uPG503B(L), uPG503P(L),
	uPG506B(L) and uPG506P(L).
	* Corrected Alloy42(Ni/Au Plated) to Cu clad Fe (Ni/Au Plated)
	on Lead Material of uPG100, uPG101 of Table 3.

DATE	September 28, 2000	
DEPT.	CSD, CSDD	
MADE BY	CHKD BY	APP.BY
M. Kusakina		Yasuo Saitoh
SIGNATURE OF APPROVAL		
R&QC		