240 Channel Segment Driver for Dot matrix STN Liquid Crystal Display with Low Voltage Drive

EM65H134

Contents

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GeneralDescription

The EM65H134 is a 240-channel segment LCD driver LSI, Which drives a dot matrix STN liquid crystal display at low power. The EM65H134 operates with a low 5V LCD drive voltage and a low 3V logic voltage. The EM65H134 includes shadowing correction circuit in order to improve image quality. The EM65H134 is packaged in a fine pitch slim TCP(slim type carrier package) technology, it is deal for substantially decreasing the size of LCD module frame.

Feature

- Duty cycle: Up to 1/300
- LCD drive voltage: 3.5 to 5.5 V
- 240 LCD drive circuits
- Operating voltage: 2.7 to 5.5 V
- Eight data bits
- Shift clock speed
  —25 MHz max/3 V
  —40 MHz max/5 V
- Shadowing correction circuit
- Display-off function
- Slim-TCP
  —Output lead pitch: 70μm
  —User area: 5.5mm
- Automatic generation of the chip enable signal
- Standby function

Applications

- PDA
- Dictionary
- Message display product

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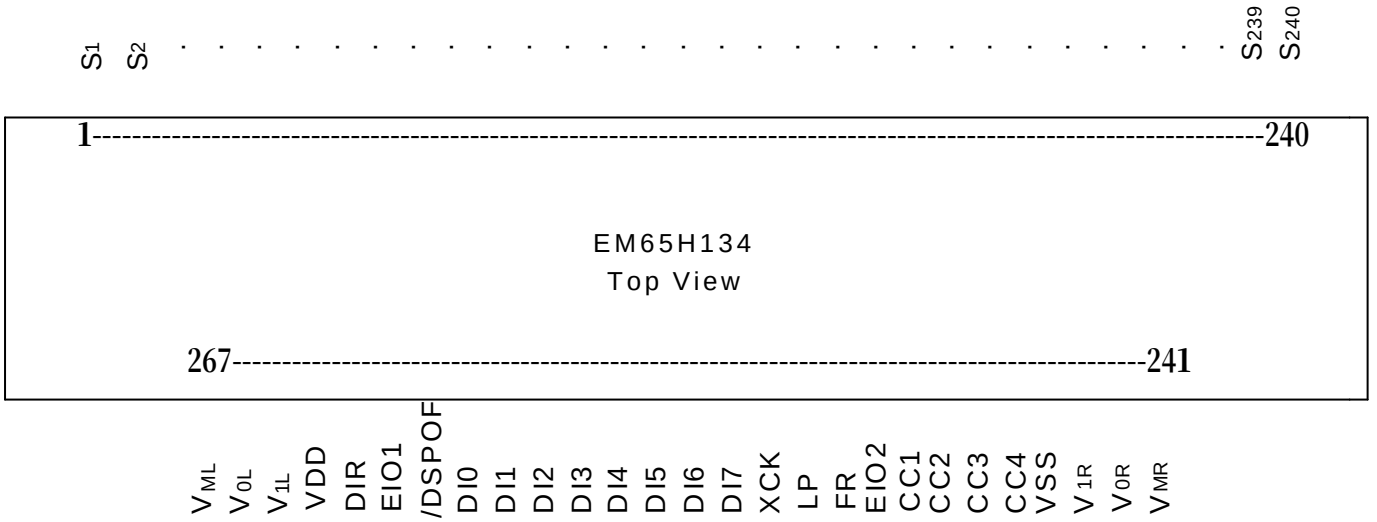
PinConfiguration



Note: The pin configuration is LSI chip, not TCP.

Figure1. Pin configuration

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FunctionalBlockDiagram

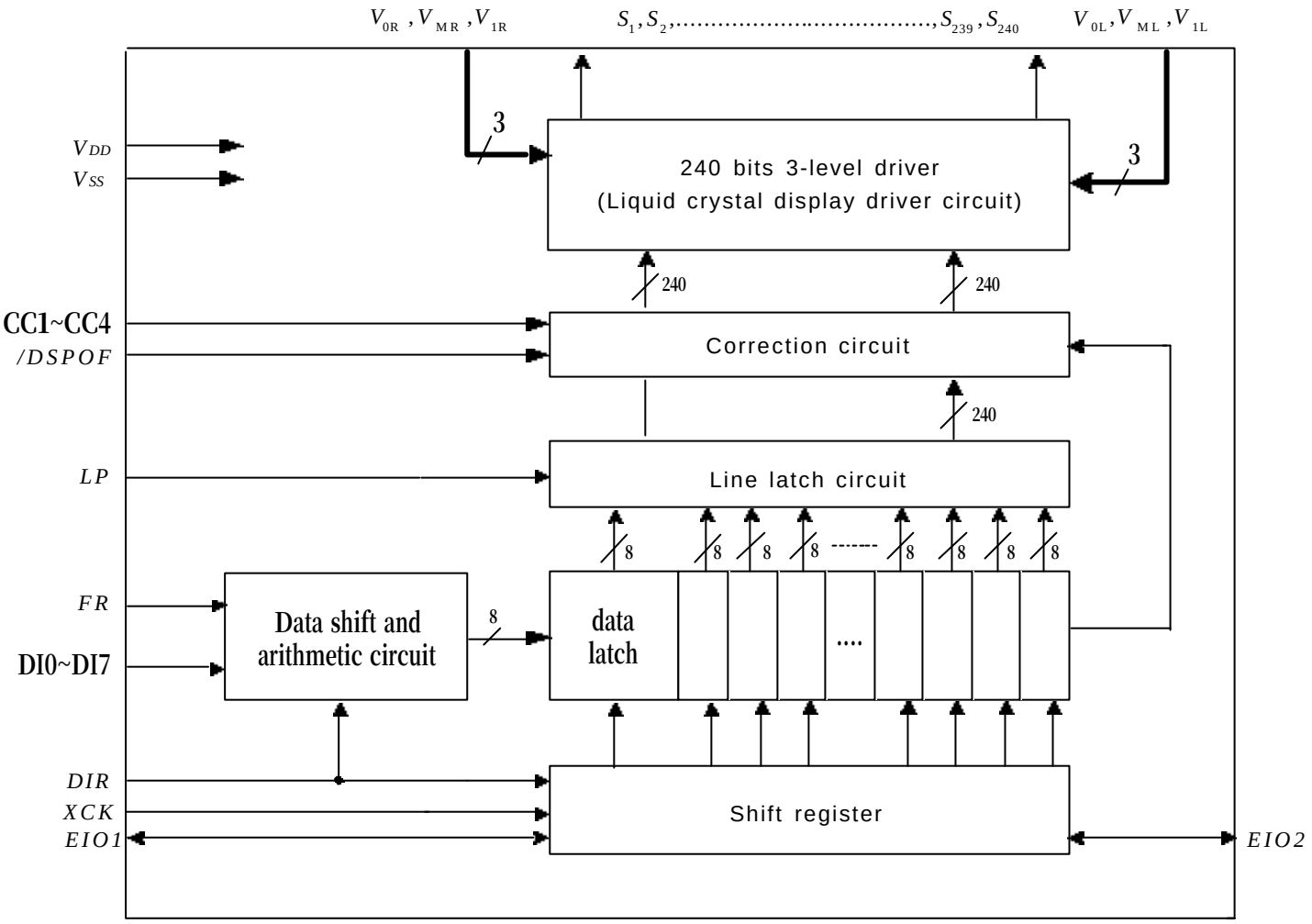

Figure 2. Block diagram

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Pin Descriptions

Table1 pin description

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>V_{DD}</td><td>264</td><td>I</td><td>Power Supply</td><td>Power supply for internal logic connects to +2.7 to +5.5V</td></tr>
<tr><td>V_{SS}</td><td>244</td><td>I</td><td>GND</td><td>Connect to Ground</td></tr>
<tr><td>V_{0R}, V_{0L}
V_{MR}, V_{ML}
V_{1R}, V_{1L}</td><td>266,242
267,241
256,243</td><td>I</td><td>Power Supply</td><td>Power supply for LCD driver level
Ensure that the voltage are set such that $V_1<V_M<V_0$, $V_M=0.5(V_0-V_1)$</td></tr>
<tr><td>$DI_0 – DI_7$</td><td>260 t0
253</td><td>I</td><td>Controller</td><td>Input for display data
input data into 8 pins $DI_0 – DI_7$</td></tr>
<tr><td>XCK</td><td>252</td><td>I</td><td>Controller</td><td>Clock signal for taking display data
Data is read on the falling of the clock pulse</td></tr>
<tr><td>LP</td><td>251</td><td>I</td><td>Controller</td><td>Latch signal for display data
Data is latched on the falling edge of the clock pulse</td></tr>
<tr><td>FR</td><td>250</td><td>I</td><td>Controller</td><td>AC signal for LCD driver
Input a frame inversion signal</td></tr>
<tr><td>DIR</td><td>263</td><td>I</td><td>Controller</td><td>Directional selection for reading display data
<table>
<tr><th>DIR</th><th>Data read direction</th></tr>
<tr><td>H</td><td>S_{240} to S_1</td></tr>
<tr><td>L</td><td>S_1 to S_{240}</td></tr>
</table></td></tr>
<tr><td>/DSPOF</td><td>261</td><td>I</td><td>Controller</td><td>When the signal is low, the output ($S_1 – S_{240}$) of LCD drive be set to level V_M</td></tr>
<tr><td>EIO_1, EIO_2</td><td>262,249</td><td>I/O</td><td>Controller</td><td>Input/output for chip selection
In output state, the output pin must connect to input pin of next EM65H134
In input state, the input pin of the fist EM65H134 must connect to Vss, the other input pin must connect to the output pin of previous EM65H134.
<table>
<tr><th>DIR</th><th>EIO_1</th><th>EIO_2</th></tr>
<tr><td>H</td><td>output</td><td>input</td></tr>
<tr><td>L</td><td>input</td><td>output</td></tr>
</table></td></tr>
</table>

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Table1 pin description (continous)

CC1	248	I		Rising crosstalk correction signal.The V1 level output is reset to VM level when CC1 is high.
CC2	247	I		Falling crosstalk correction signal.The V0 level output is reset to VM level when CC2 is high.
CC3	246	I		Waveform distortion non-selected (black) data correction signal.The present output pin (non-selected)and the next output pin (non-selected) are reset to the VM level when CC3 is high.
CC4	245	I		Waveform distortion selected (white) data correction signal.The present output pin (selected)and the next output pin (selected) are reset to the VM level when CC4 is high.
S_1-S_{240}	1 to 240	O		LCD driver output. One of two levels is output according to the combination of the FR signal and display data, when /DSPOF is in V_{DD}

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FUNCTIONDESCRIPTIONS

- Shift Register

The 30-bit shift register generate latch signal for data latch circuit at the falling edge of XCK signal. The shift direction is selected by DIR signal.

- Data Latch

It latches the data on the 8 bits data bus(DI0 to DI7) and output the data to line latch. It is controlled by shift register.

- Line Latch

All 240 bits, which have been read into the data latch are simultaneously latched at the falling edge of the LP signal then output to the correction circuit and 3-level driver.

- 3-level Driver

Drive LCD panel from driver output pins, selecting one of three levels (V_0, V_M, V_1) based on the line latch data, correction circuit(CC1 to CC4) and /DSPOF.

-Correction Circuit

This circuit corrects the shadowing volume.

1.The circuit compares the crosstalk correction signals (CC1 and CC2) from the external circuits and present output, and determines whether the effective value is increased due to crosstalk. If the effective value is increased, the output level is reset to the VM level.

2.The circuit compares the output data to the next output data. If there are no data changes due to the waveform distortion correction signal (CC3 and CC4), the output level is reset to VM level.

The reset period can be adjusted by using CC1 to CC4. The correction needed depends on each output pin.

-Data Shift and Arithmetic Circuit

The data shifter shifts the destinations of data output when necessary. The arithmetic circuit performs operations for the data and FR signal.

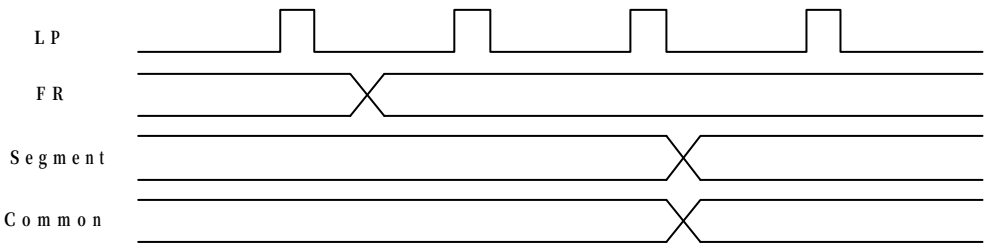

Figure 3. FR、LP、output timing

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Relation between FR、latch data、/DSPOF and output level

Table 2 LCD driver output voltage level

FR	Latch data	/DSPOF	Driver output voltage level
H	H	H	V_0
H	L	H	V_1
L	H	H	V_1
L	L	H	V_0
X	X	L	V_M

$V_{SS} \leqq V_1 < V_M < V_0$ H:V_{DD} L:V_{SS} X:Don't care

Relationship between the display data and driver output and data output destination

Table 3 Relationship between the display data and driver output

DIR	EIO1	EIO2	Data Input	Figure of clock						
				1st	**2nd**	**3rd**	…	**28th**	**29th**	**30th**
L	Input	Output	DI_0	S_8	S_{16}	S_{24}	…	S_{224}	S_{232}	S_{240}
			DI_1	S_7	S_{15}	S_{23}	…	S_{223}	S_{231}	S_{239}
			DI_2	S_6	S_{14}	S_{22}	…	S_{222}	S_{230}	S_{238}
			DI_3	S_5	S_{13}	S_{21}	…	S_{221}	S_{229}	S_{237}
			DI_4	S_4	S_{12}	S_{20}	…	S_{220}	S_{228}	S_{236}
			DI_5	S_3	S_{11}	S_{19}	…	S_{229}	S_{227}	S_{235}
			DI_6	S_2	S_{10}	S_{18}	…	S_{228}	S_{226}	S_{234}
			DI_7	S_1	S_9	S_{17}	…	S_{227}	S_{225}	S_{233}
H	Output	Input	DI_0	S_{233}	S_{225}	S_{217}	…	S_{17}	S_9	S_1
			DI_1	S_{234}	S_{226}	S_{218}	…	S_{18}	S_{10}	S_2
			DI_2	S_{235}	S_{227}	S_{219}	…	S_{19}	S_{11}	S_3
			DI_3	S_{236}	S_{228}	S_{220}	…	S_{20}	S_{12}	S_4
			DI_4	S_{237}	S_{229}	S_{221}	…	S_{21}	S_{13}	S_5
			DI_5	S_{238}	S_{230}	S_{222}	…	S_{22}	S_{14}	S_6
			DI_6	S_{239}	S_{231}	S_{223}	…	S_{23}	S_{15}	S_7
			DI_7	S_{240}	S_{232}	S_{224}	…	S_{24}	S_{16}	S_8

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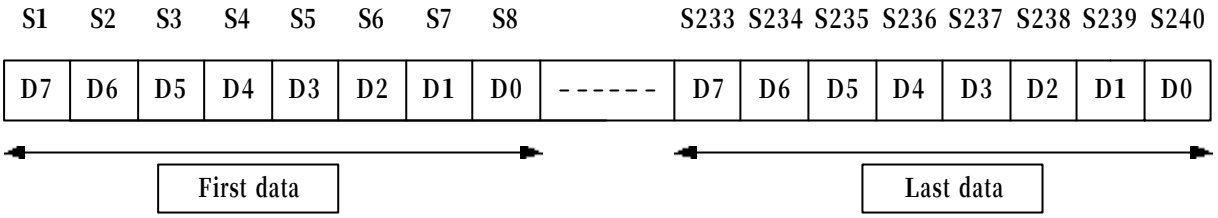
Data output destination

The direction of data latch and the chip enable input/output pin can be select by DIR signal.

DIR=VSS ,Enable input: EIO1 ,Enable output: EIO2



DIR=VDD ,Enable input: EIO2 ,Enable output: EIO1

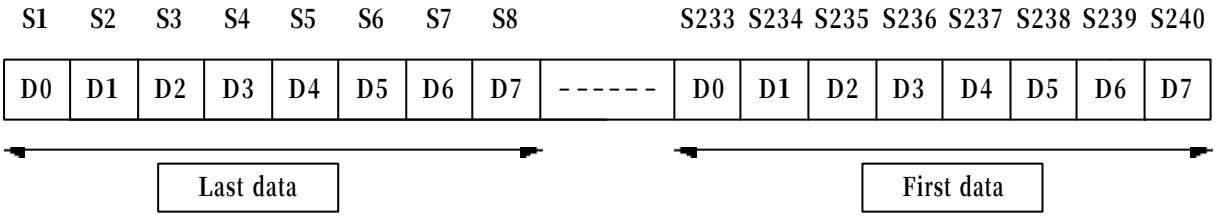


Figure 4. Data output destination

Operating timing

Figure 4 shows the 8-bit data-latch timing when DIR=GND; that is, when the EIO1 pin is a chip-enable input and the EIO2 pin is a chip-enable output. When SHL=$V_{cc,}$ the EIO1 pin is a chip-enable output and the EIO2 pin is a chip-enable input.

When a low chip-enable signal is input via the EIO1 pin, the EM65H134 is first released from the data-standby state, then, at the falling edge of the following XCK pulse, it is released entirely from the standby state and starts latching data.

It simultaneously latches eight bits of data at the falling edge of each XCK pulse. When it has latched 232 bits of data, it sets the EIO2 signal to low. When it has latched 240 bits of data, it automatically stops and enters the standby state, initiating the next EM65H134, provided its EIO2 pin is connected to the EIO1 pin of the next EM65H134.

The EM65H134 output one line of data from the S1 to S240 pins at the falling edge of each LP pulse. Data d1 is output from S1, and d240 from S240 when SHL=GND, and d1 is output from S240, and d240 from S1 when DIR= $V_{cc.}$

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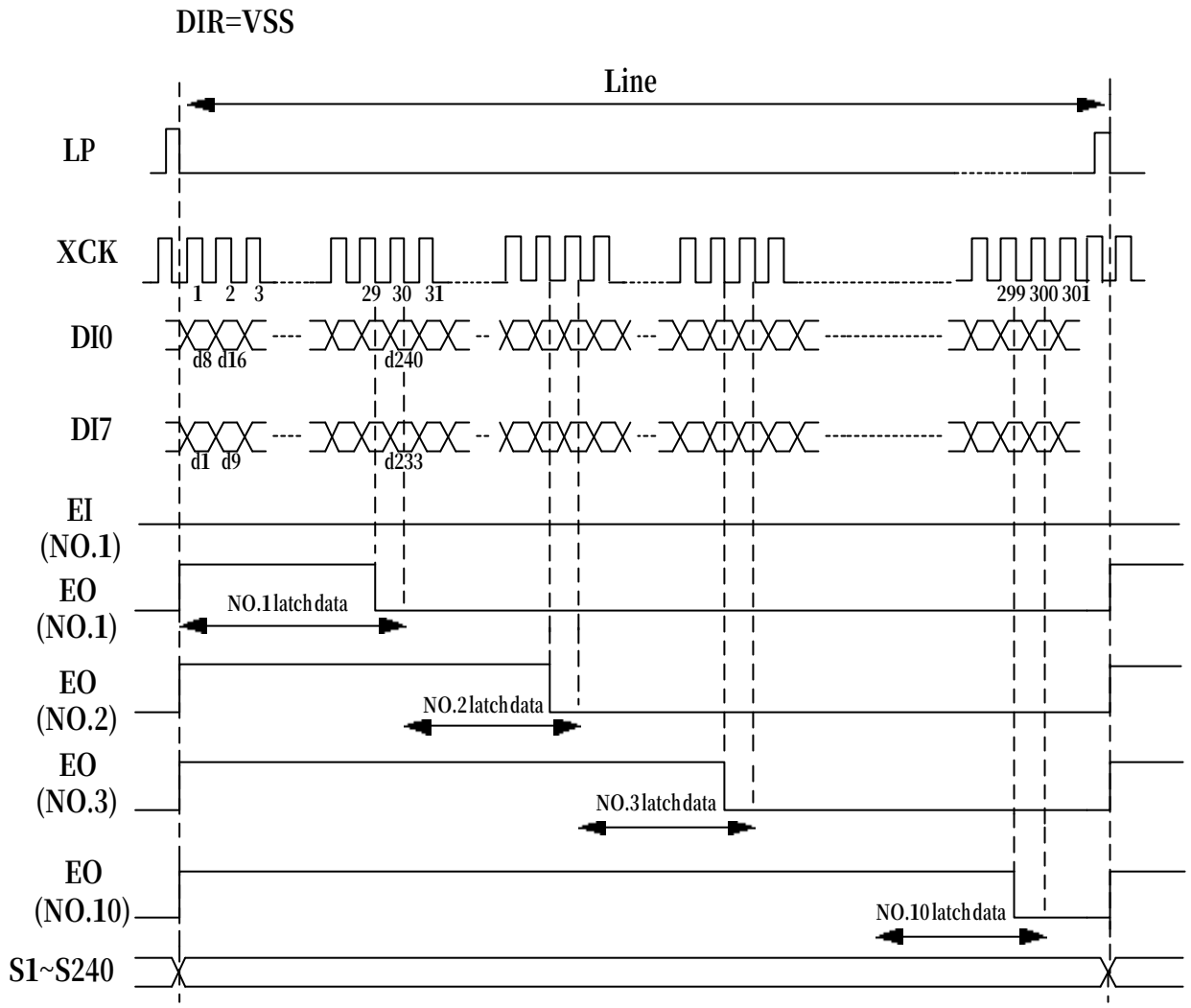

Figure 5. Data latch timing

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Correction circuit

The EM65H134 include shadowing correction circuits. There are two types of shadowing: one caused by crosstalk, and the other by waveform distortion. In both types, image quality can be improved by correction circuits CC1, CC2, CC3, and CC4.

(1) CC1 and CC2(Shadowing caused by crosstalk)

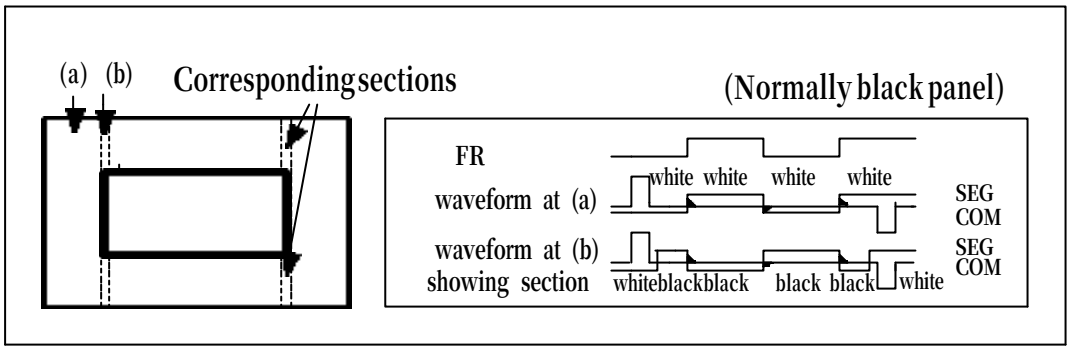

Figure 6. Shadowing caused by crosstalk

When a ruled line is displayed, noise occurs in the common VM level in the LCD panel due to the segment change of a solid background in FR reverse. This is because many segments display the solid background and are simultaneously changed, affecting the common VM level (creating crosstalk). The effective voltage for section (a) in the solid background becomes low. On the other hand, the effective voltage for section (b) becomes high. Shadowing occurs in the corresponding sections due to the different voltages.

The EM65H134s compare the crosstalk correction signals CC1 and CC2 and the present output, and determine whether the effective value is increased by the crosstalk. If increased, the output level is reset to the VM, which corrects the effective voltages in (a) and (b) and suppresses the shadowing. Figure 8 shows an example of the crosstalk-correction-signal external circuit. The basic potentials of a comparator (VM+△V and VM−△V') are corrected according to the shadowing level for output correction while CC1 and CC2 are high. CC1 corrects the rising crosstalk, and CC2 corrects the falling crosstalk.

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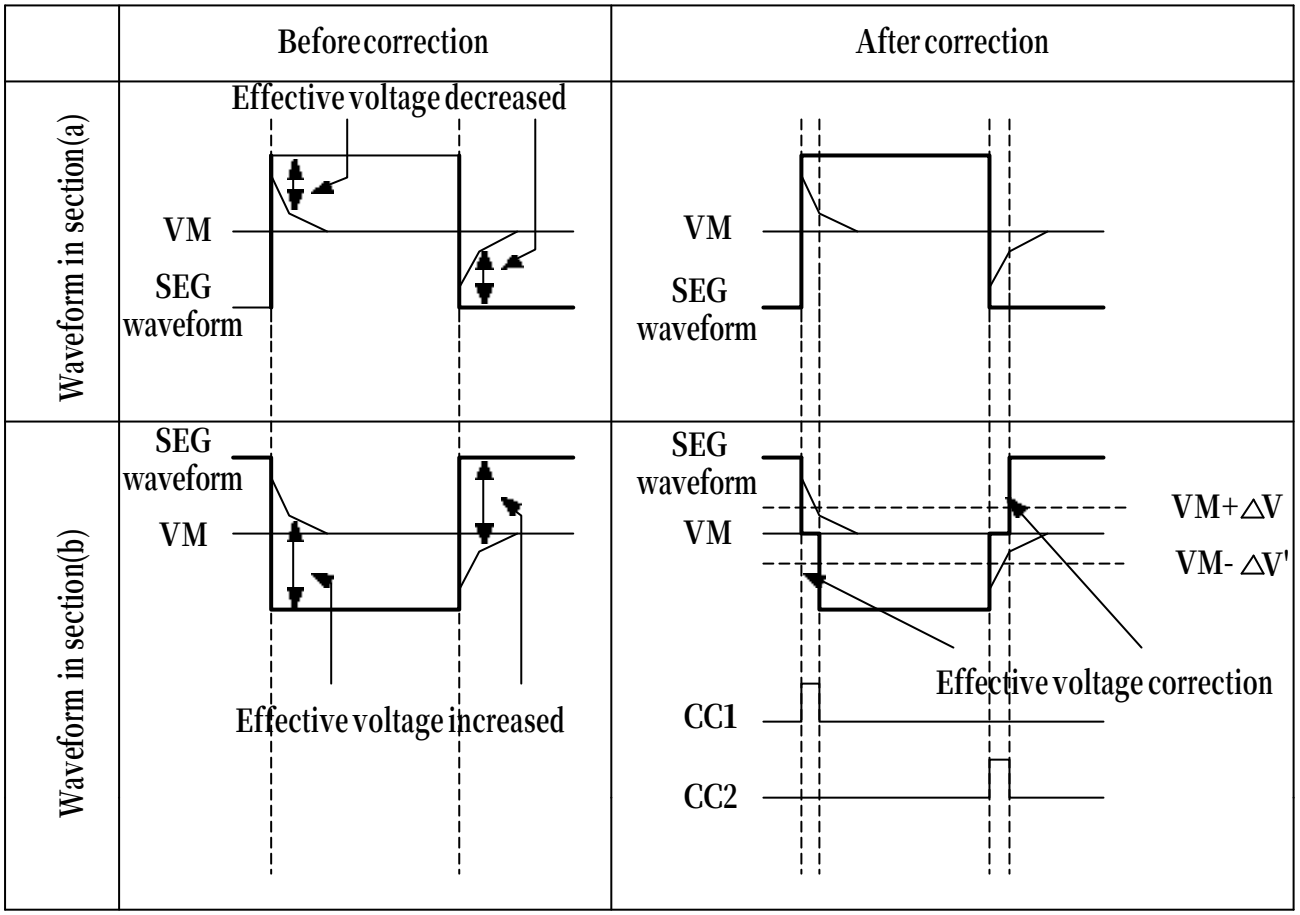

Figure 7. Effective voltage correction

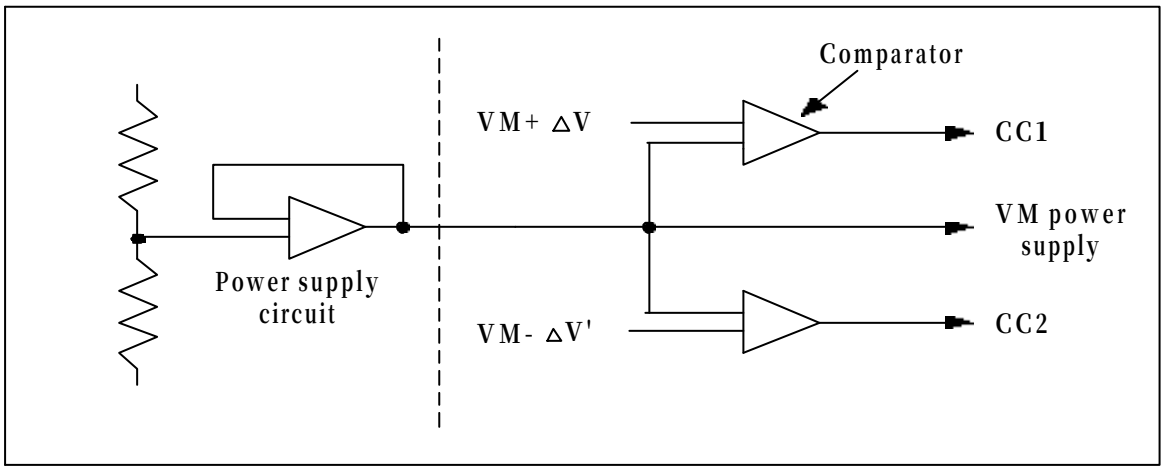

Figure8. CC1 and CC2 external circuit

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(2) CC3 and CC4(shadowing caused by waveform distortion)

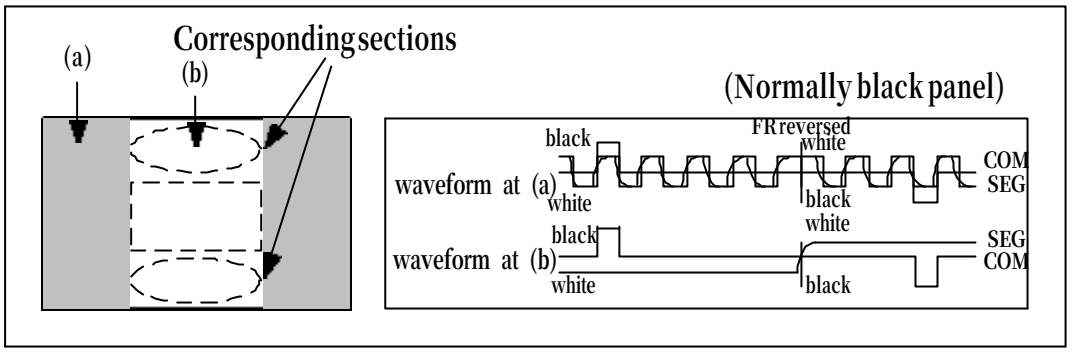

Figure 9. Shadowing caused by waveform distortion

When the background is displayed in grayscale (for example, in a checker pattern), many segment levels are changed in section (a) but not in section (b). The effective voltage for section (a) becomes low because distortion occurs in the segment output waveform due to driver or panel impedance. On the other hand, the effective voltage for section (b) becomes high because the waveform is changed only slightly. Shadowing occurs in the corresponding sections due to the different voltages.

The EM65H134 compare the present output data and the next output data. If the data is not changed, the output level is reset to the VM, which corrects the effective voltages in (a) and (b). The high width is corrected according to the shadowing level for output correction while CC3 and CC4 are high. CC3 corrects the non-selected output pin (black background), and CC4 corrects the selected output pin (white background).

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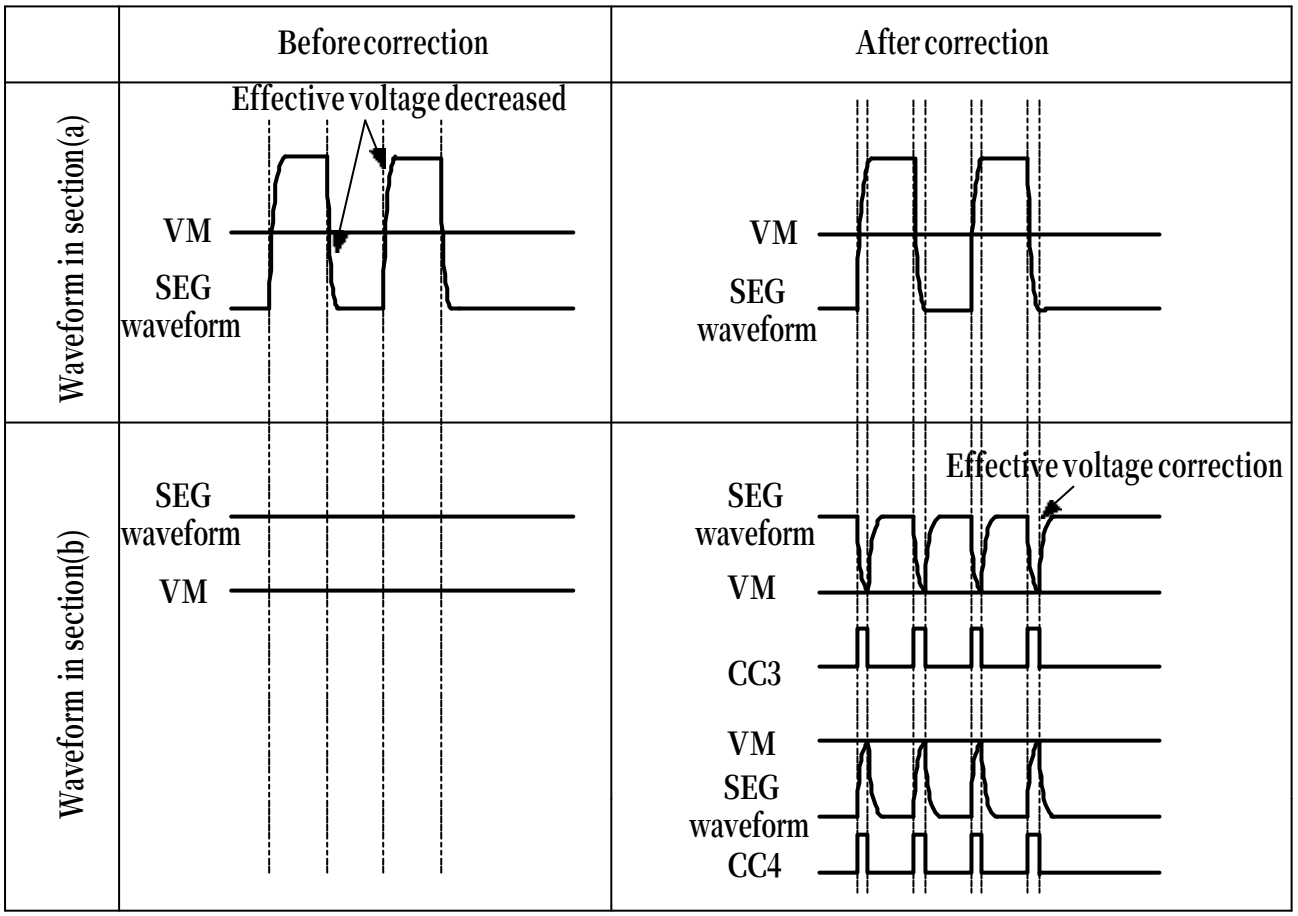

Figure 10. Effective voltage correction by waveform distortion

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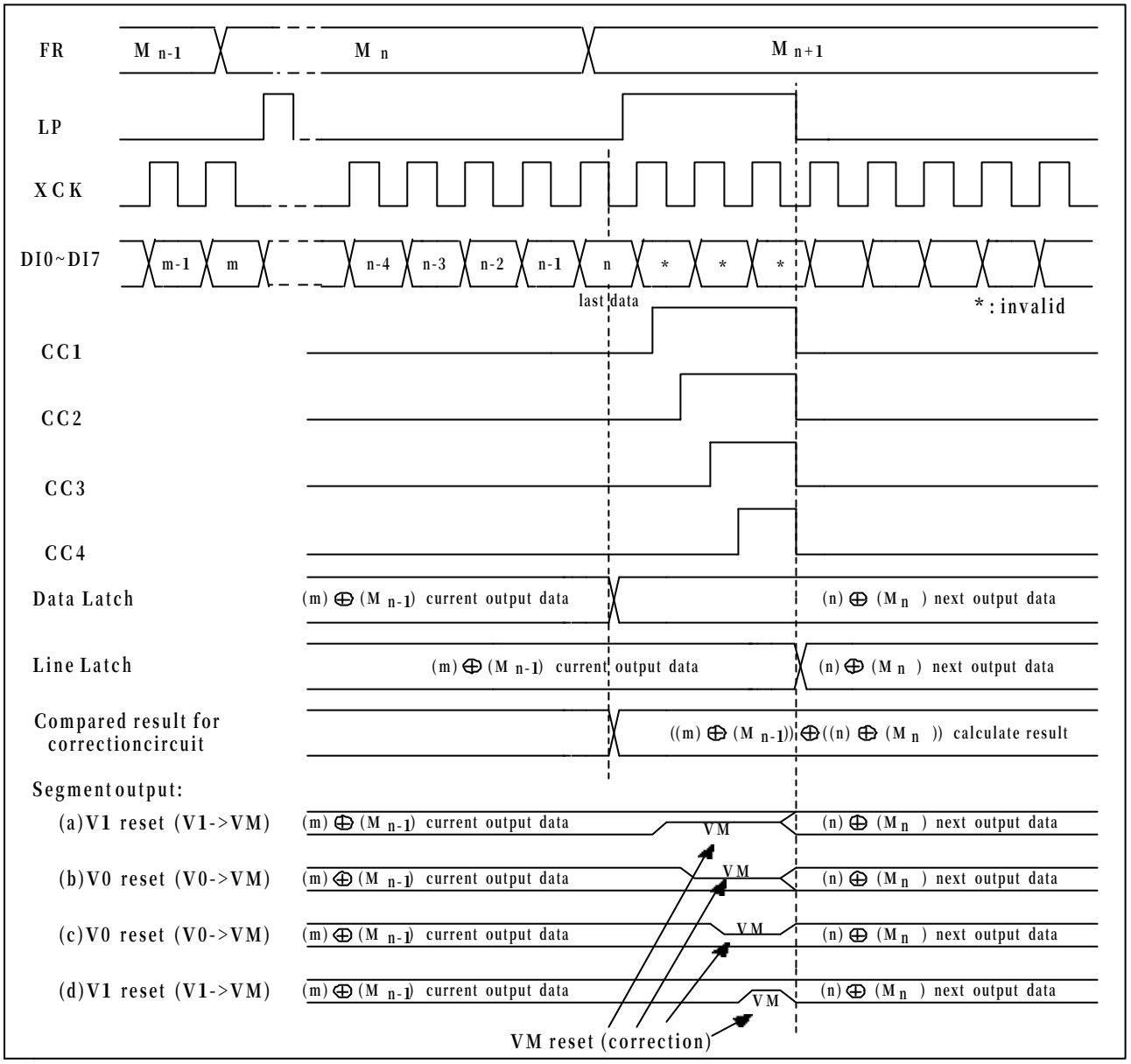

Figure 11. Compared result for correction circuit

The correction circuit compares the present output data (line latch) and the next output data (data latch). Depending on the compared result, the circuit resets the high width of CC3 to the VM for the output without a data change if the data is the non-selected output ((c) in figure 12). The circuit resets the high width of CC4 to the VM if the data is the selected output ((d) in figure 12). CC3 and CC4 are input after the last valid data is transferred. CC1 forcibly resets the V1 output to for the high width ((a) in the figure 12). CC2 forcibly resets the V0 output to VM for the high width ((b) in figure 12). Therefore, shadowing caused by waveform distortion is corrected with CC3 or CC4 (non-selected or selected), and shadowing caused by crosstalk is corrected with CC1 or CC2 (in the V0 or V1 direction).

Note: The high period from CC1 to CC4 should be matched with the shadowing level.

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AbsoluteMaximumratings

Table 4 absolute maximum ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Referenced to V_{SS} (0V)	V_{DD} *1,*2	-0.3 to +7.0	V
Supply voltage (2)	V_0		V_{0L}, V_{0R} *1,*2	-0.3 to +7.0	V
Input voltage(1)	V_{I1}		XCK, LP,DIR,FR, EIO_1, EIO_2, DI_{0-7},/DSPOF, CC1 to CC4 *1	-0.3 to V_{DD}+0.3	V
Input voltage(2)	V_{I2}		V_{ML},V_{MR},V_{1L},V_{1R} *1,*2	-0.3 to V_0+0.3	V
Operating temperature	T_{opr}			-30to +75	℃
Storage temperature	T_{stg}			-55 to +110	℃

Note：1. if the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within it's specified operating range for normal operation to prevent malfunctions or degraded reliabilility.

2. As show in figure11, user should conform to the following turn on/off sequence for the power and signal. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, the LSI reliability will be affected.

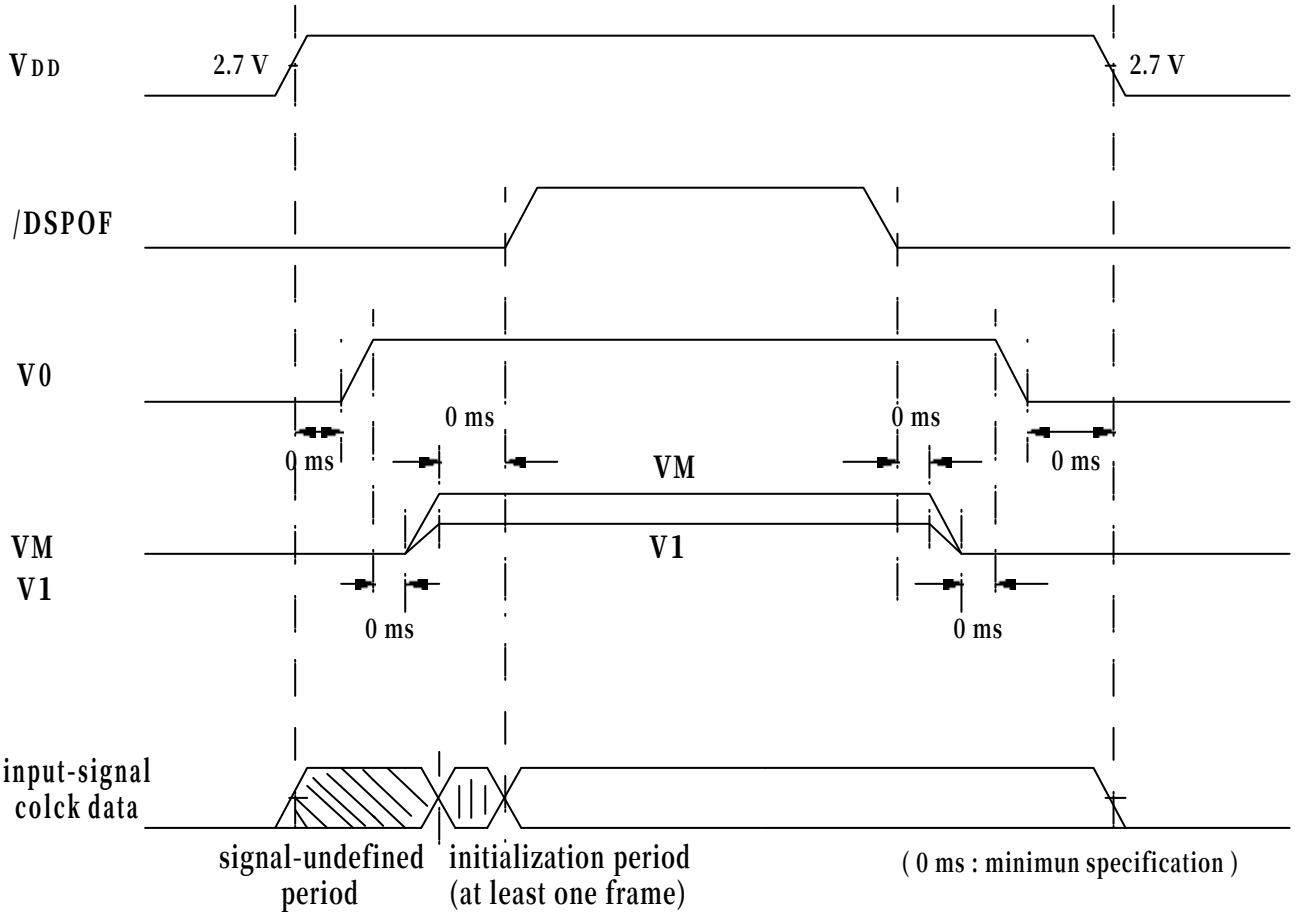

Figure 12. Turn on/off timing

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3. Turn on the power:

(1) Turn on the power in the order of GND-VDD, GND-V0, and VM/V1. THEN ground the /DSPOF pin.

(2) The LCD forcibly outputs the VM level by the DISPLAYOFF function.

(3) Even an input signal disturbed immediately after VDD is applied, the DISPLAYOFF function has priority.

(4) Input the specific signal to initialize the registers in the driver. The initialization period must be at lease one frame.

(5) The preparation for the normal display is completed. Apply the VDD level to the /DSPOF pin to cancel the DISPLAYOFF function. At this time, the level of pin V0, VM and V1 must rise to the specific potential.

4. Turn off the power:

The procedure is basically the reverse of that used to turn on the power.

(1) Ground the /DSPOF pin.

(2) Turn off the LCD power in the order of VM/V1 and GND-V0.

(3) Ground VDD and an input signal.

At this time, the level of pin V0, VM and V1 must fall to 0V. Since the DISPLAYOFF function stops when VDD fall to 0V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turn off or on.

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DCCHARACTERISTICS

Table 5 DC characteristics 1

(V_{SS} = GND=0V, V_{DD} = +2.7 to +4.5V, V_0 -Vss= 3.5 to 5.5V, T_a = -30~+75°C)

Parameter	Symbol	Conditions		Applicable pins	Min	Type	Max	Unit
Input voltage	V_{IH}			DI_0 -DI_7, XCK, LP,DIR,FR,EIO_1, EIO_2, /DSPOF, CC1 to CC4	0.7V_{DD}		V_{DD}	V
	V_{IL}				0		0.3V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current (1)	I_{IL1}	V_I=V_{DD} - V_{SS}		DI_0 -DI_7, XCK, LP, DIR, FR, MD, EIO_1, EIO_2, /DSPOF	-5		+5	uA
Input leakage current (2)	I_{IL2}	V_I=V_0 - V_{SS}		V_{ML},V_{MR},V_{1L},V_{1R}	-100		+100	uA
Output resistance	R_{ON} *1	I_{ON} = 150uA	V_{0R},V_{OL}	Y_1- Y_{240}		0.5	1.0	kΩ
			V_{MR},V_{ML}			1.0	2.0	
			V_{1R},V_{1L}			0.5	1.0	
Stand-by current	I_{STB} *2 *3	VI = V_{DD}	V_{DD}=3V f_{XCK}=25MHZ f_{LP}=100KHZ f_{FR}=4kHZ	V_{DD}		0.4	1.0	mA
Consumed current	I_{DD} *2 *3	VI = Vss		V_{DD}		1.0	6.0	mA
Consumed current	I_0 *2			V_{0L}, V_{0R}		0.4	1.0	mA

Table 6 DC characteristics 2

(V_{SS} =GND= 0V, V_{DD} = 4.5V to 5.5V, V_0 -Vss= 3.5 to 5.5V, T_a = -30~+75°C)

Parameter	Symbol	Conditions		Applicable pins	Min	Type	Max	Unit
Input voltage	V_{IH}			DI_0 -DI_7, XCK, LP,DIR,FR,EIO_1, EIO_2, /DSPOF, CC1 to CC4	0.7V_{DD}		V_{DD}	V
	V_{IL}				0		0.3V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current (1)	I_{IL1}	V_I=V_{DD} - V_{SS}		DI_0 -DI_7, XCK, LP, DIR, FR, MD, EIO_1, EIO_2, /DSPOF	-5		+5	uA
Input leakage current (2)	I_{IL2}	V_I=V_0 - V_{SS}		V_{ML},V_{MR},V_{1L},V_{1R}	-100		+100	uA
Output resistance	R_{ON} *1	I_{ON} = 150uA	V_{0R},V_{OL}	Y_1- Y_{240}		0.5	1.0	kΩ
			V_{MR},V_{ML}			1.0	2.0	
			V_{1R},V_{1L}			0.5	1.0	
Stand-by current	I_{STB} *2 *3	VI = V_{DD}	V_{DD}=5V f_{XCK}=40MHZ f_{LP}=160KHZ f_{FR}=6kHZ	V_{DD}		1.0	2.0	mA
Consumed current	I_{DD} *2 *3	VI = Vss		V_{DD}		3.0	15	mA
Consumed current	I_0 *2			V_{0L}, V_{0R}		0.4	2.0	mA

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Note : 1. Indicate the resistance between one of thwe pins Y1~Y240 and one of the voltage supply pins,when load current is applied to the Y pins. Defined under the following conditions:

V0-Vss = 5.5V; VM = (V0=V1)/2; V1 = Vss+1

V1 should be near the ground level, VM should be near the middle voltage between V1 and V0. V1should be within the range of △V = 2.5V0, which is the range within which R_{ON}, the LCD driver circuit's output impedance, is stable. See figure 13

2. Input and output are excluded. When a CMOS input is left floating, excess the current flows from the power supply through the input circuit. To avoid this, VIH and VIL must be used at VDD and Vss, respectively.

3. VI = enable input,. When DIR = Vss, VI = EIO1. When DIR = V_{DD} , VI = EIO2

4. The voltage of each signal is show in figure 14

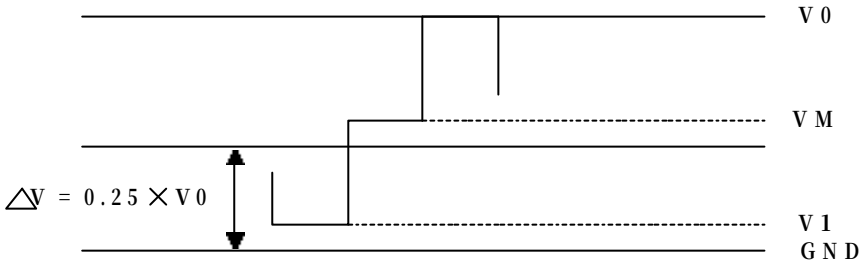

Figure 13.Relationship between driver output waveform and each level voltage

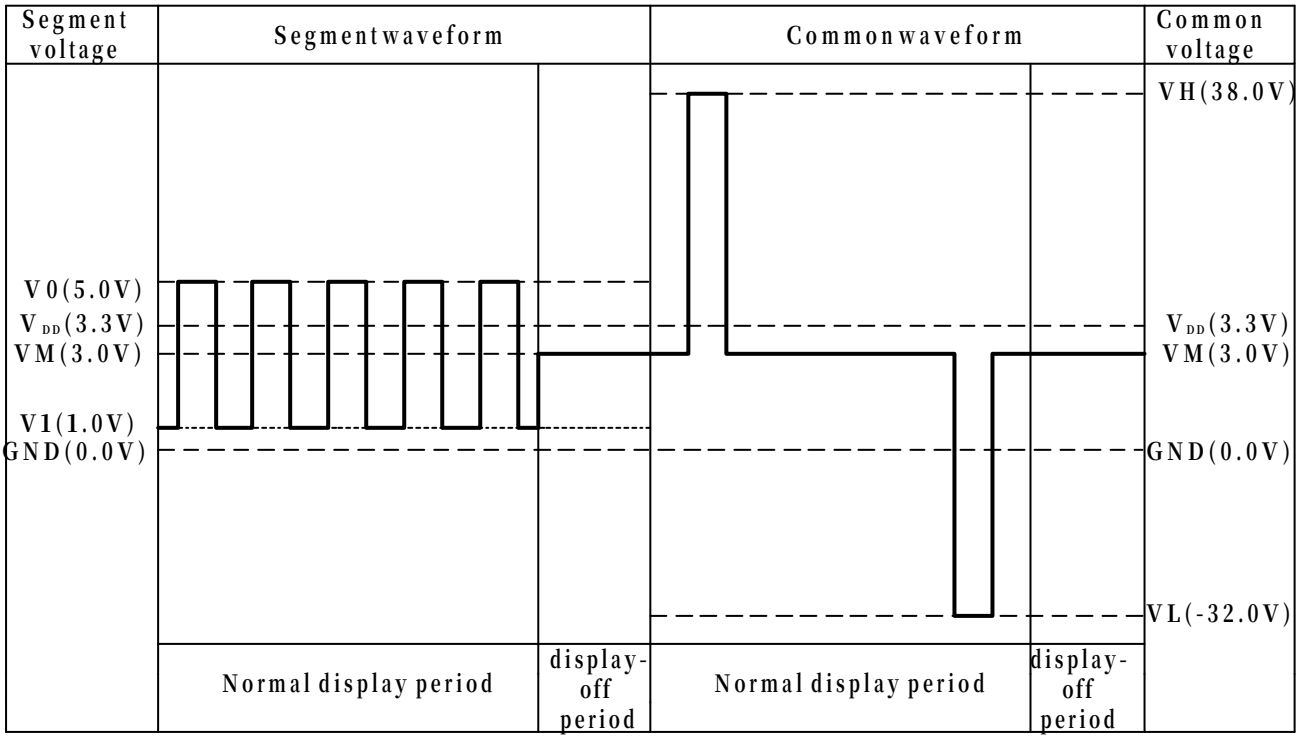

Figure 14. Signal voltage

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ACElectricalcharacteristic

Table 7 AC electrical characteristics 1

(V_{SS} = GND=0V, **V_{DD} = 2.7 to 4.5V**, V_0 -Vss= 3.5 to 5.5V, T_a = 30~75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period	T_{WCK}		40			ns
Shift clock “H” pulse width	T_{WCKH}		15			ns
Shift clock “L” pulse width	T_{WCKL}		15			ns
Data setup time	T_{DS}		10			ns
Data hold time	T_{DH}		10			ns
Latch pulse “H” pulse width	T_{WLPH}		30			ns
Shift and latch clock set up time	T_S		20			ns
Shift and latch clock hold time	T_H		50			ns
Shift and latch clock rise time	T_R				30	ns
Shift and latch clock fall time	T_F				30	ns
FR set up time	T_{FS}		20			ns
FR hold time	T_{FH}		20			ns
Output delay time	T_D	C_L=100pF			500	ns
CC setup time	T_{CCS}		20			ns
CC hold time	T_{CCH}		20			ns

Table 8 AC electrical characteristics 2

(V_{SS} =GND= 0V, **V_{DD} = 4.5 to 5.5V**, V_0 -Vss= 3.5 to 5.5V, T_a = 30~75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period	T_{WCK}		25			ns
Shift clock “H” pulse width	T_{WCKH}		10			ns
Shift clock “L” pulse width	T_{WCKL}		10			ns
Data setup time	T_{DS}		6			ns
Data hold time	T_{DH}		6			ns
Latch pulse “H” pulse width	T_{WLPH}		25			ns
Shift and latch clock set up time	T_S		20			ns
Shift and latch clock hold time	T_H		50			ns
Shift and latch clock rise time	T_R				20	ns
Shift and latch clock fall time	T_F				20	ns
FR set up time	T_{FS}		20			ns
FR hold time	T_{FH}		20			ns
Output delay time	T_D	C_L=100pF			500	ns
CC setup time	T_{CCS}		20			ns
CC hold time	T_{CCH}		20			ns

NOTES: 1. The load must be less than 10 pF between the EIO1 and EIO2 connections of the EM65H134s.

2. connect the load circuit as shown in figure 15.

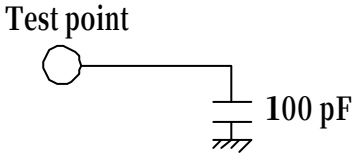

Figure 15. Load circuit for output delay time

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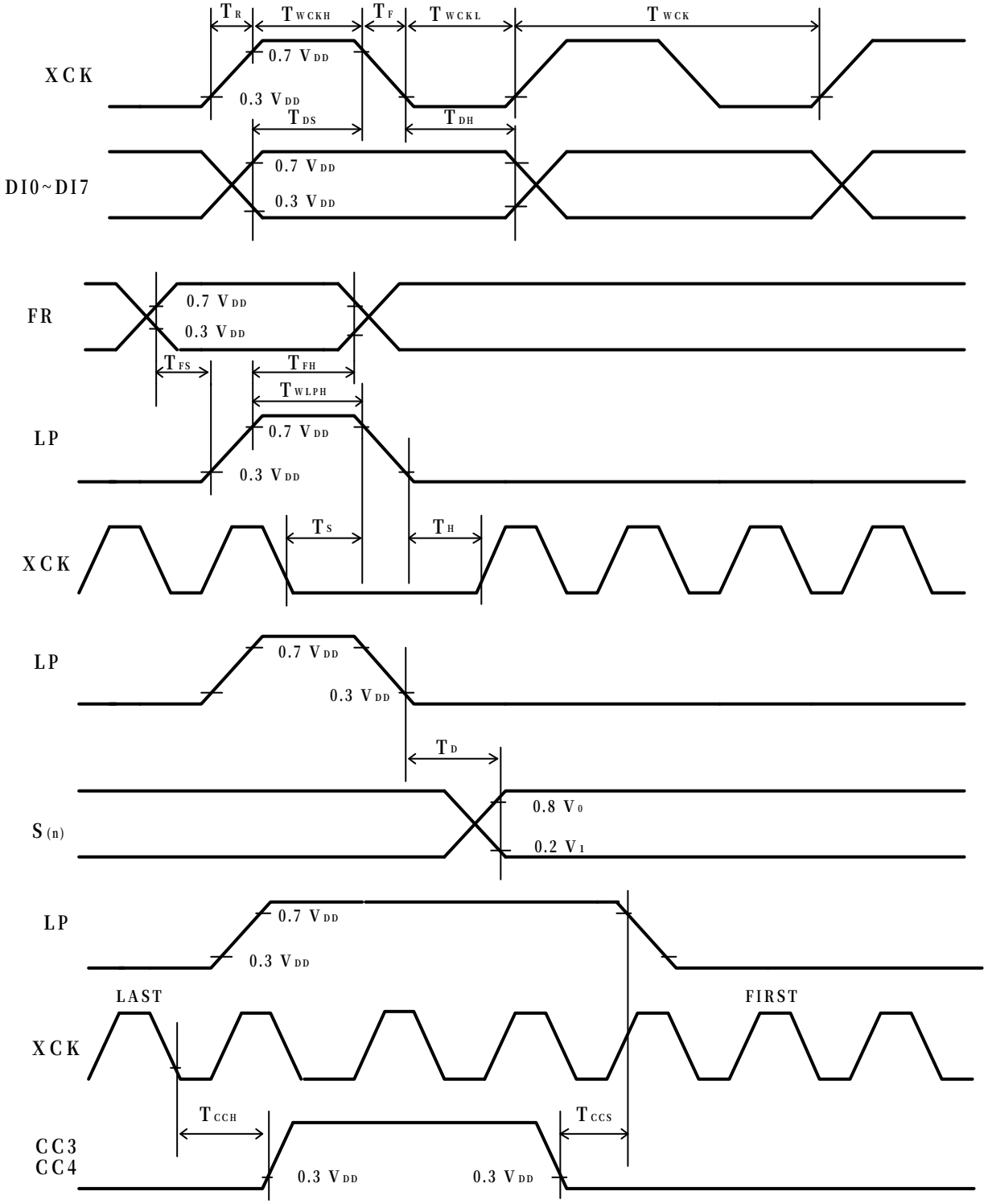
Timingdiagram



Correct the waveform by CC3 and CC4 after XCK fetches the last data.

Complete correction before data from the next line is output at the falling edge of LP.

Figure 16. AC characteristics

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Applicationcircuit

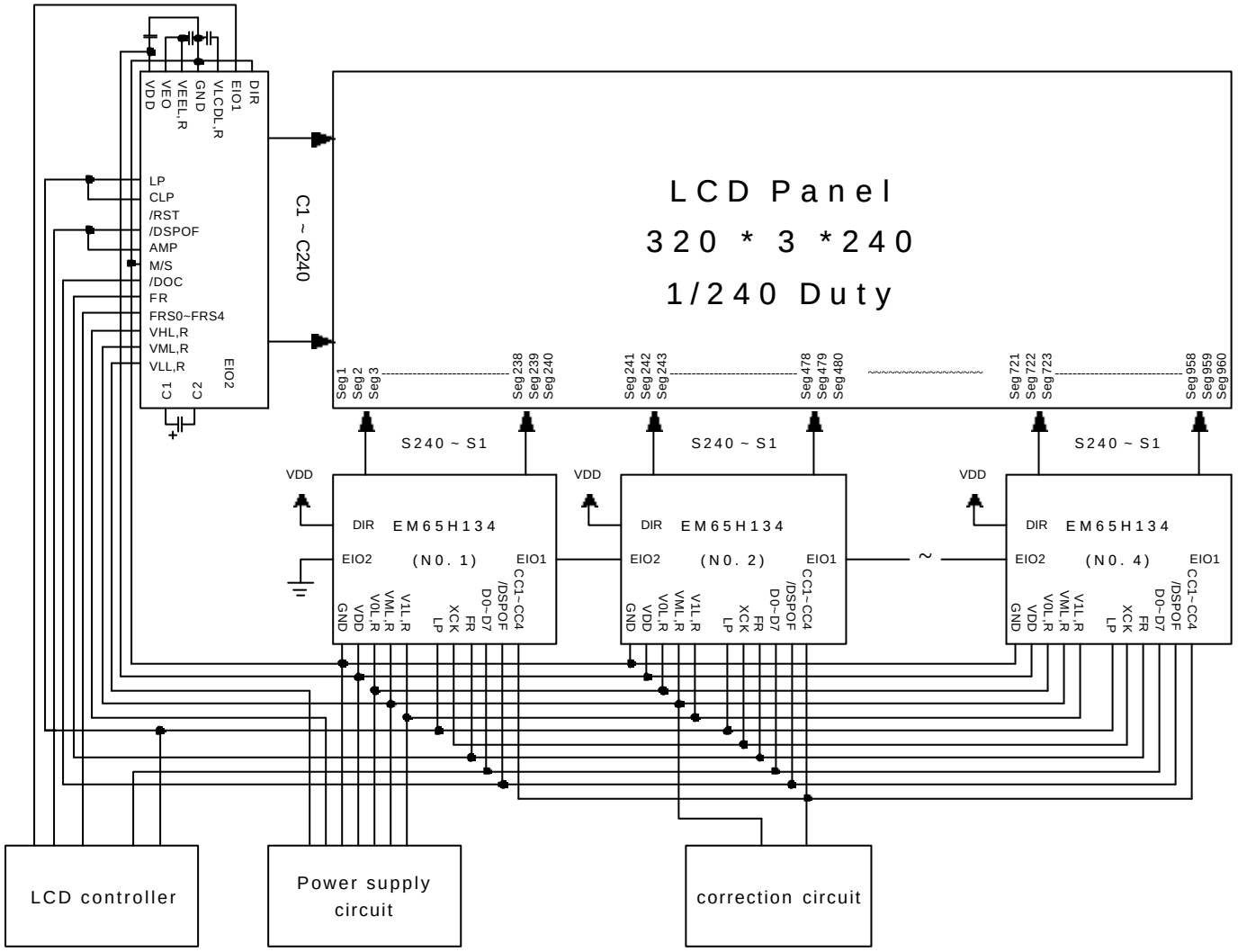

Figure 17. Application circuit

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