Preliminary

GENERAL DESCRIPTION

The EM65240 is a 240-channel LCD driver LSI used to drive large scale dot matrix LCD panels, like PDA, personal computers and workstations. Which is made by power CMOS high voltage process technology. Through the use of TCP technology, it is deal for substantially decreasing the size of LCD module frame. This product can function as a common and a segment driver, which is used for liquid crystal dot matrix display.

In common driver mode, it can be selected in single mode and dual mode by a mode pin (MD), data input/output pins are bi-directional, four data shift direction are pin selectable.
In segment driver mode, it can be selected 4-bit parallel input mode or 8-bit parallel input mode by a mode pin (MD).

FEATURES

Both common mode and segment mode

- Display duty application: up to 1/480 duty
- Supply voltage for the logic system: +2.5 to +5.5V
- Supply voltage for LCD driver: +15 to +42V
- Number of LCD driver outputs: 240
- Low output impedance
- Low power consumption
- CMOS silicon process (P-type Silicon substrate)
- 268 pin TCP (tape carrier package) package: EM65240U

Common mode

- Shift clock frequency: 4.0MHz (Max.) (V_{DD}=+2.5 to +5.5)
- Built-in 240 bits bi-directional shift register (divisible into 120bits*2)
- Available in a single mode or in a dual mode
- Data input/output pins are bi-directional, four data shift direction are pin selectable.
- Shift register circuit reset function when /DSPOF active

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Segment mode

- Shift clock frequency: 20MHz(Max.) (V_{DD}=+ 5V ± 10%)
  15MHz(Max.) (V_{DD}=+ 3.5V to + 4.5V)
  12MHz(Max.) (V_{DD}=+ 2.5V to + 3.0V)
- Adopts a data bus system
- 4-bits/8-bits parallel input mode are selected by MD pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select, causes the internal clock to be stopped by automatically counting 240 of input data
- Line latch circuit reset function when /DSPOF active

PIN CONFIGURATION

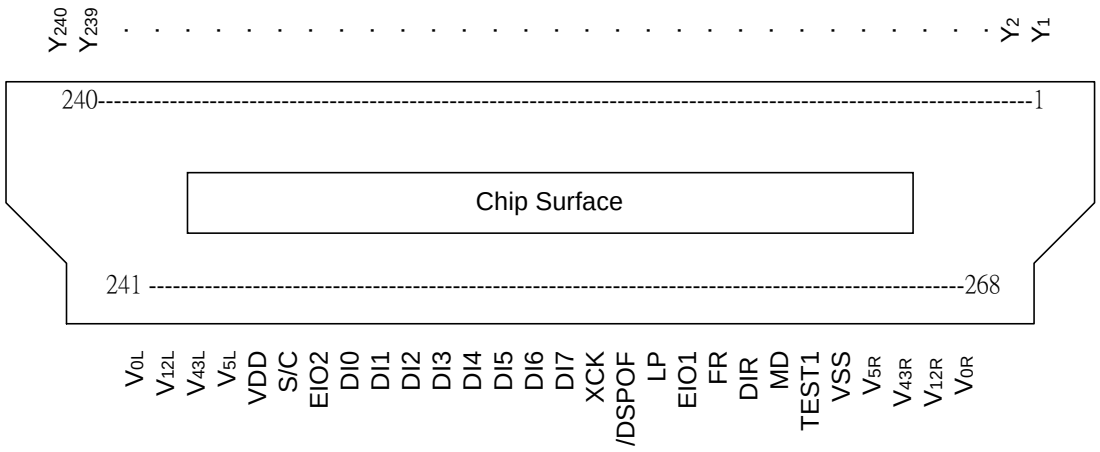

Figure1 pin configuration

Preliminary

Table 1 pin designation

Pin NO.	Symbol	I/O	Description
1 to240	$Y_1 – Y_{240}$	O	LCD driver output
241,268	V_{OL},V_{OR}	-	Power supply for LCD driver
242,267	V_{12L},V_{12R}	-	Power supply for LCD driver
243,266	V_{43L},V_{43R}	-	Power supply for LCD driver
244,265	V_{5L},V_{5R}	-	Power supply for LCD driver
245	V_{DD}	-	Power supply for logic system
246	S/C	I	Segment/common mode selection
247 259	EIO_2 EIO_1	I/O	Input /output for chip select or data of shift register
248 to 254 255	$DI_0 – DI_6$ DI_7	I	Display data input for segment mode Dual mode data input for common mode
256	XCK	I	Display data shift clock input for segment mode
257	/DSPOF	I	Control input for non-select output level
258	LP	I	Latch pulse input/shift clock input for shift register
260	FR	I	AC-converting signal input for LCD driver waveform
261	DIR	I	Display data shift direction selection
262	MD	I	Mode selection input
263	$TEST_1$	I	Test mode selection input
264	V_{SS}	-	Ground (0 V)

Preliminary

PIN DESCRIPTIONS

Segment mode

Table2 pin description of segment mode

Symbol	I/O	Connected to	Functions
V_{DD}	I	Power Supply	Power supply for internal logic connects to +2.5 to +5.5V
V_{SS}	I	GND	Connect to Ground
V_{0R} , V_{0L} V_{12R} , V_{12L} V_{34R} , V_{34L} V_{5R} , V_{5L}	I	Power Supply	Power supply for LCD driver level • Normally , the bias voltage used is set by resistor divider • Ensure that the voltage are set such that $V_{SS} \leqq V_5 < V_{34} < V_{12} < V_0$ • To further reduce the difference between the output waveforms of LCD driver output pin Y_1 and Y_{240} , externally connect V_{iR} and V_{iL} (i=0 , 12 , 34 , 5)
DI_0 – DI_7	I	Controller	Input for display data • In 4-bit parallel input mode , input data into 4 pins DI_0 – DI_3 • In 8-bit parallel input mode , input data into8 pins DI_0 – DI_7
XCK	I	Controller	Clock signal for taking display data Data is read on the falling of the clock pulse
LP	I	Controller	Latch signal for display data • Data is latched on the falling edge of the clock pulse
S/C	I	Controller	Selection of segment mode/common mode S/C: H = segment mode; L = common mode

Segment mode (continuous)

<table>
<tr><td>DIR</td><td>I</td><td>Controller</td><td>Directional selection for reading display data
<table>
<tr><th>DIR</th><th>Data read direction</th></tr>
<tr><td>L</td><td>Y_{240} to Y_1</td></tr>
<tr><td>H</td><td>Y_1 to Y_{240}</td></tr>
</table></td></tr>
<tr><td>/DSPOF</td><td>I</td><td>Controller</td><td>Control signal for output deselect level
• The input signal is level-shifted from logic voltage level to LCD driver voltage level ，and controls LCD drive circuit
• When the signal is low，the output (Y_1 – Y_{240}) of LCD drive be set to level V_5，the contents of line latch are reset，but read the display data in the data latch regardless of condition of /DSPOF
• When this signal return to high, the operation returns to the normal status.</td></tr>
<tr><td>FR</td><td>I</td><td>Controller</td><td>AC signal for LCD driver
• Input a frame inversion signal
• The LCD driver output voltage level can be set by line latch output signal and FR signal</td></tr>
<tr><td>MD</td><td>I</td><td>Controller</td><td>Mode selection
<table>
<tr><th>MD</th><th>Mode selection</th></tr>
<tr><td>H</td><td>4-bit parallel input</td></tr>
<tr><td>L</td><td>8-bit parallel input</td></tr>
</table></td></tr>
</table>

Segment mode (continuous)

<table>
<tr><td>EIO_1，EIO_2</td><td>I/O</td><td>Controller</td><td>Input/output for chip selection
• In output state，after 240-bit of data have been read ，set to “L” then set to “H”
• In input state ，the chip is selected when EI is set to “L”，then 240-bit of data have been read，the ship is deselected
<table>
<tr><td>DIR</td><td>EIO_1</td><td>EIO_2</td></tr>
<tr><td>H</td><td>input</td><td>output</td></tr>
<tr><td>L</td><td>output</td><td>input</td></tr>
</table>
</td></tr>
<tr><td>Y_1-Y_{240}</td><td>O</td><td></td><td>LCD driver output.
• One of four levels is output according to the combination of the FR signal and display data</td></tr>
<tr><td>$TEST_1$</td><td>I</td><td></td><td>Test mode selection
• during normal operation，connect to V_{SS}</td></tr>
</table>

Preliminary

Common mode

Table3 pin description of common mode

Symbol	I/O	Connected to	Functions
V_{DD}	I	Power supply	Power supply for internal logic connects to +2.5 to +5.5V
V_{SS}	I	GND	Connect to Ground
V_{0R},V_{0L} V_{12R},V_{12L} V_{34R},V_{34L} V_{5R},V_{5L}	I	Power supply	Power supply for LCD driver level • Normally，the bias voltage used is set by resistor divider • Ensure that the voltage are set such that $V_{SS} \leqq V_5 < V_{34} < V_{12} < V_0$ • To further reduce the difference between the output waveforms of LCD driver output pin Y_1 and Y_{240} ，externally connect V_{iR} and V_{iL} (i=0，12，34，5)
EIO_1， EIO_2	I/O		Data input/output shift for bi-directional shift register • When EIO1(EIO_2) is input，it will be pull-down • When EIO1(EIO_2) is output，it will not be pull-down DIR: H → EIO_1: input, EIO_2: output; DIR: L → EIO_1: output, EIO_2: input
LP	I	Controller	Shift clock for bi-directional shift register • Data is shifted on the falling edge of the clock
DIR	I	Controller	Directional selection of bi-directional shift register DIR: L → Y_{240} to Y_1; DIR: H → Y_1 to Y_{240}

Common mode (continuous)

/DSPOF	I	Controller	Control signal for output deselect level • The input signal is level-shifted from logic voltage level to LCD driver voltage level ，and controls LCD drive circuit • When the signal is low，the output (Y_1 – Y_{240}) of LCD drive be set to level V_5，the contents of shift register are reset not read • When this signal return to high, the operation returns to the normal status.
FR	I	Controller	AC signal for LCD drive • Input a frame inversion signal • The LCD driver output voltage level can be set by shift register output signal and FR signal
MD	I	Controller	Mode selection MD: H = Dual mode; L = Single mode
S/C	I	Controller	Selection of segment mode/common mode S/C: H = segment mode; L = common mode
DI_7	I	Controller	Dual mode data input • In dual mode，data can input from 121st bit
DI_0-DI_6	I	V_{SS} or V_{DD}	Not used
XCK	I	V_{SS} or open	Not used
Y_1-Y_{240}	O		LCD driver output. • One of four voltage levels is output according to the data of shift register and FR signal
$TEST_1$	I		Test mode select • during normal operation，connect to V_{SS}

Preliminary

BLOCK DIAGRAM

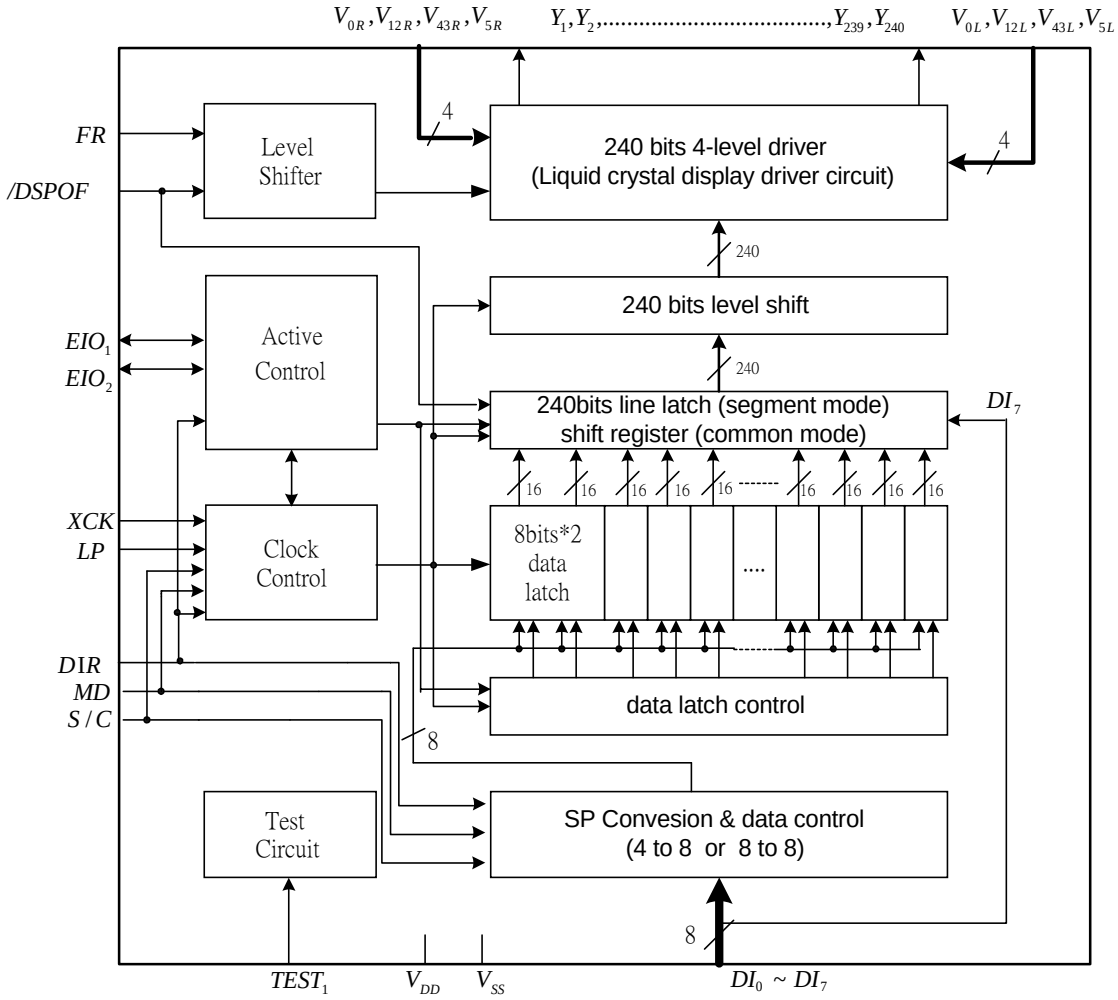

Figure 2 block diagram

FUNCTIONAL DESCRIPTIONS

. Active Control

In case of segment mode, controls the selection or deselection of the chip. Following a LP signal, and after the chip select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.

. SP Conversion & Data Control

In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bits parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

. Data Latch Control

In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.

. Data Latch

In case of segment mode, latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control, 240 bits of data are read in 30 sets of 8 bits.

. Line Latch / Shift Register

In case of segment mode, all 240 bits, which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.
In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.

. Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

. 4-level Driver

Drive the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and /DSPOF

. Control Logic

Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block.

Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is deselected. In case of common mode, controls the direction of data shift.

.Test Circuit

The circuit for the test. During normal operation, it doesn't act.

Relation between FR，Latch data ，/DSPOF and output level

Table 4 LCD driver output voltage level

(a) Segment mode

FR	Latch data	/DSPOF	Driver output voltage level
H	H	H	V_0
H	L	H	V_{12}
L	H	H	V_5
L	L	H	V_{43}
X	X	L	V_5

$V_{SS} \leqq V_5 < V_{43} < V_{12} < V_0$ H:V_{DD} L:V_{SS} X:Don't care

(b) Common mode

FR	Latch data	/DSPOF	Driver output voltage level
H	H	H	V_5
H	L	H	V_{12}
L	H	H	V_0
L	L	H	V_{43}
X	X	L	V_5

$V_{SS} \leqq V_5 < V_{43} < V_{12} < V_0$ H:V_{DD} L:V_{SS} X:Don't care

Relationship between the display data and driver output pin

Table 5 Relationship between the display data and driver output pin

(a)Segment mode (4-bit parallel mode)

MD	DIR	EIO_1	EIO_2	Data Input	Figure of clock						
					1_{st}	2_{nd}	3_{rd}	…	38_{th}	39_{th}	60_{th}
H	H	Input	Output	DI_0	Y_4	Y_8	Y_{12}	…	Y_{232}	Y_{236}	Y_{240}
				DI_1	Y_3	Y_7	Y_{11}	…	Y_{231}	Y_{235}	Y_{329}
				DI_2	Y_2	Y_6	Y_{10}	…	Y_{230}	Y_{234}	Y_{238}
				DI_3	Y_1	Y_5	Y_9	…	Y_{229}	Y_{233}	Y_{237}
H	L	Output	Input	DI_0	Y_{237}	Y_{233}	Y_{229}	…	Y_9	Y_5	Y_1
				DI_1	Y_{238}	Y_{234}	Y_{230}	…	Y_{10}	Y_6	Y_2
				DI_2	Y_{239}	Y_{235}	Y_{231}	…	Y_{11}	Y_7	Y_3
				DI_3	Y_{240}	Y_{236}	Y_{232}	…	Y_{12}	Y_8	Y_4

(b) Segment mode (8-bit parallel mode)

MD	DIR	EIO1	EIO2	Data Input	Figure of clock						
					1_{st}	2_{nd}	3_{rd}	…	28_{th}	29_{th}	30_{th}
L	H	Input	Output	DI_0	Y_8	Y_{16}	Y_{24}	…	Y_{224}	Y_{232}	Y_{240}
				DI_1	Y_7	Y_{15}	Y_{23}	…	Y_{223}	Y_{231}	Y_{239}
				DI_2	Y_6	Y_{14}	Y_{22}	…	Y_{222}	Y_{230}	Y_{238}
				DI_3	Y_5	Y_{13}	Y_{21}	…	Y_{221}	Y_{229}	Y_{237}
				DI_4	Y_4	Y_{12}	Y_{20}	…	Y_{220}	Y_{228}	Y_{236}
				DI_5	Y_3	Y_{11}	Y_{19}	…	Y_{229}	Y_{227}	Y_{235}
				DI_6	Y_2	Y_{10}	Y_{18}	…	Y_{228}	Y_{226}	Y_{234}
				DI_7	Y_1	Y_9	Y_{17}	…	Y_{227}	Y_{225}	Y_{233}
L	L	Output	Input	DI_0	Y_{233}	Y_{225}	Y_{217}	…	Y_{17}	Y_9	Y_1
				DI_1	Y_{234}	Y_{226}	Y_{218}	…	Y_{18}	Y_{10}	Y_2
				DI_2	Y_{235}	Y_{227}	Y_{219}	…	Y_{19}	Y_{11}	Y_3
				DI_3	Y_{236}	Y_{228}	Y_{220}	…	Y_{20}	Y_{12}	Y_4
				DI_4	Y_{237}	Y_{229}	Y_{221}	…	Y_{21}	Y_{13}	Y_5
				DI_5	Y_{238}	Y_{230}	Y_{222}	…	Y_{22}	Y_{14}	Y_6
				DI_6	Y_{239}	Y_{231}	Y_{223}	…	Y_{23}	Y_{15}	Y_7
				DI_7	Y_{240}	Y_{232}	Y_{224}	…	Y_{24}	Y_{16}	Y_8

(c) Common mode

MD	DIR	Data transfer direction	EIO_1	EIO_2	DI_7
H (Dual)	H	Y_1~Y_{120}	Input	Output	Input
		Y_{121}~Y_{240}			
	L	Y_{240}~ Y_{121}	Output	Input	Input
		Y_{120}~ Y_1			
L (Single)	H	Y_1~Y_{240}	Input	Output	X
	L	Y_{240}~ Y_1	Output	Input	X

H:V_{DD} L:V_{SS} X**:Don't care**

Connection example of plural segment driver

Case of DIR="L"

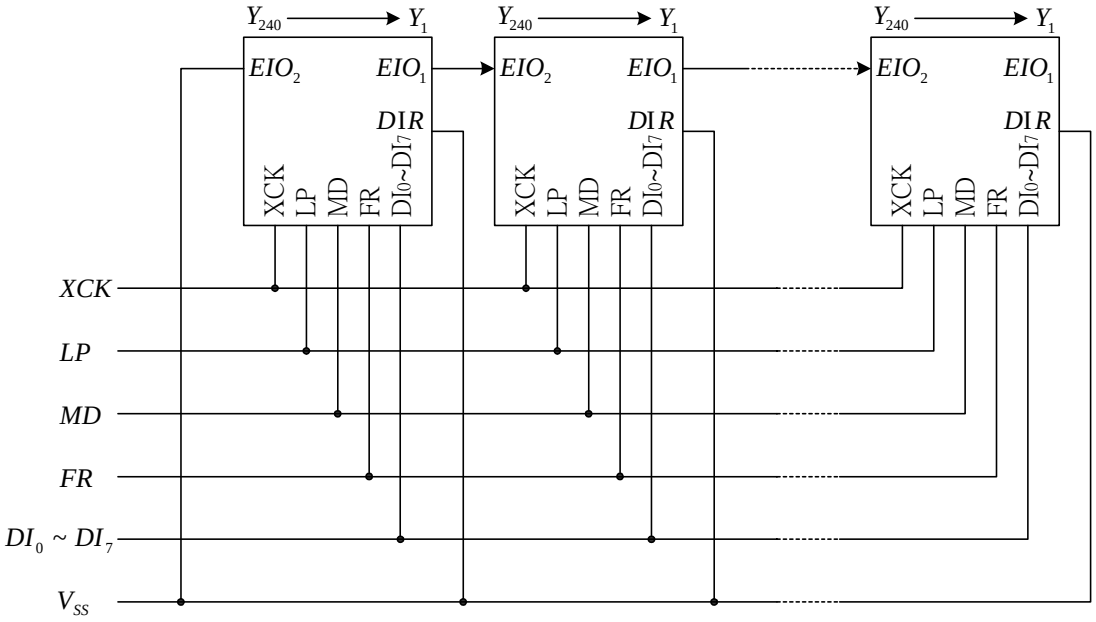

Figure 3 Segment mode of DIR="L"

Case of DIR="H"

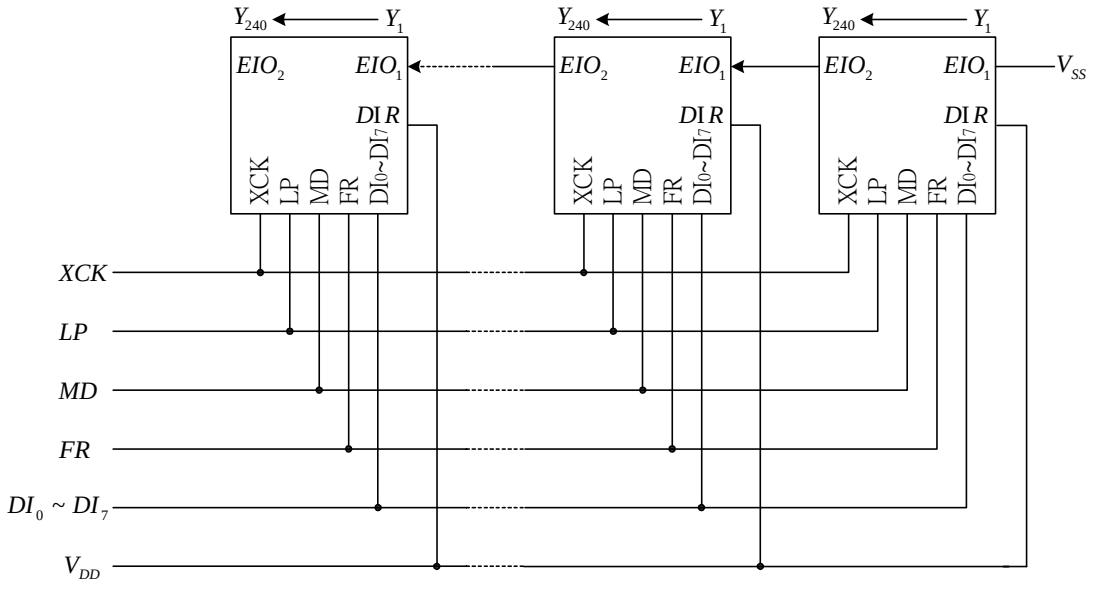

Figure 4 Segment mode of DIR="H"

Connection of plural common driver

Single mode DIR=”L”

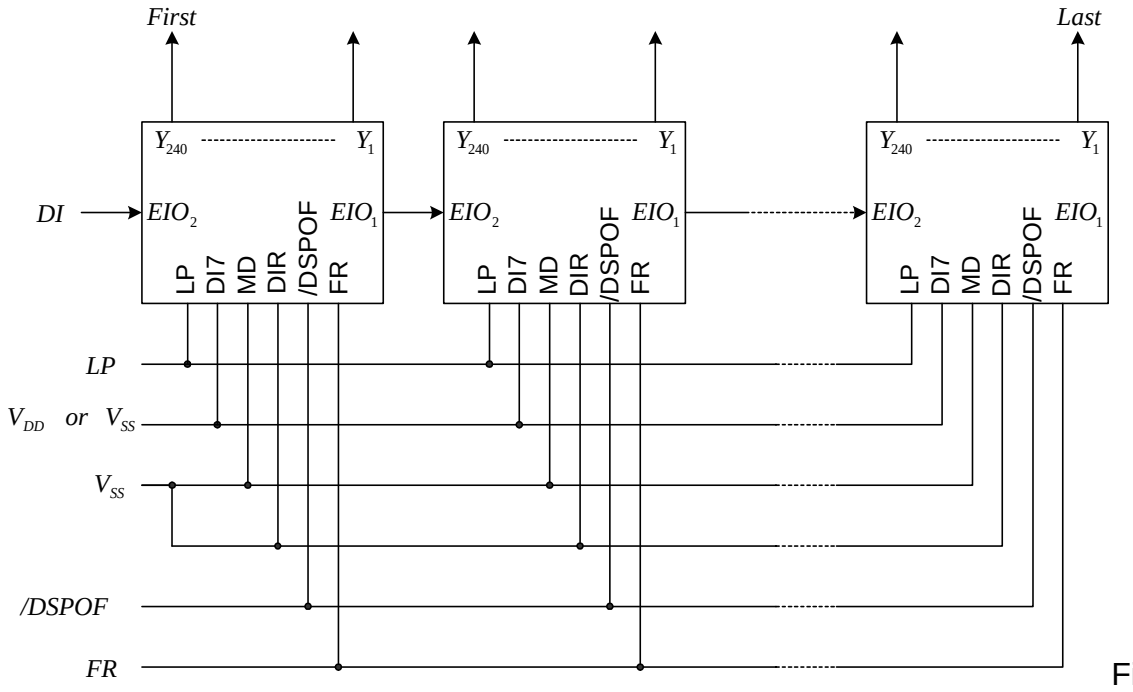

Figure 5 Single mode DIR=”L”

Single mode DIR=”H”

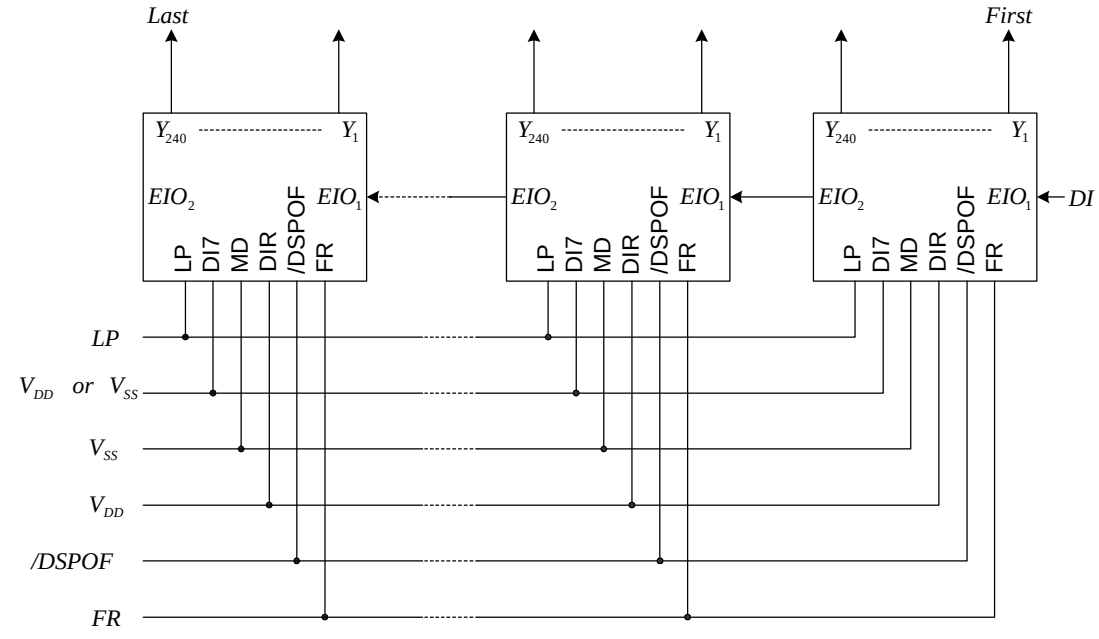

Figure 6 Single mode DIR=”H”

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Connection of plural common driver

Dual mode DIR="L"

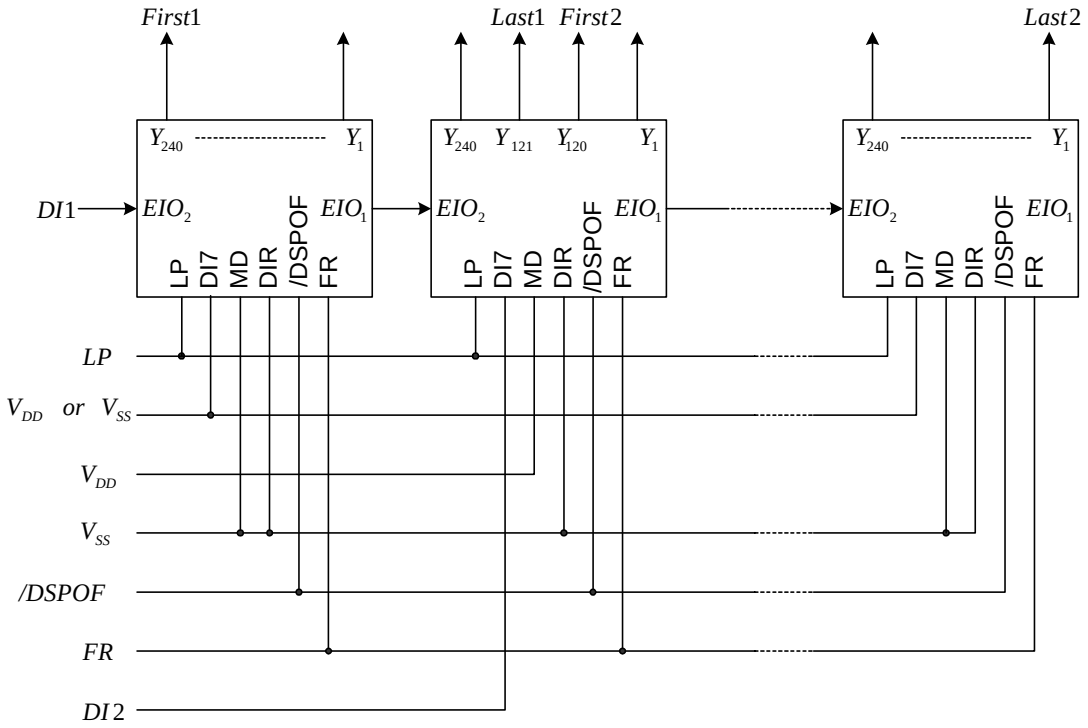


Figure 7 Dual mode DIR="L"

Dual mode DIR="H"

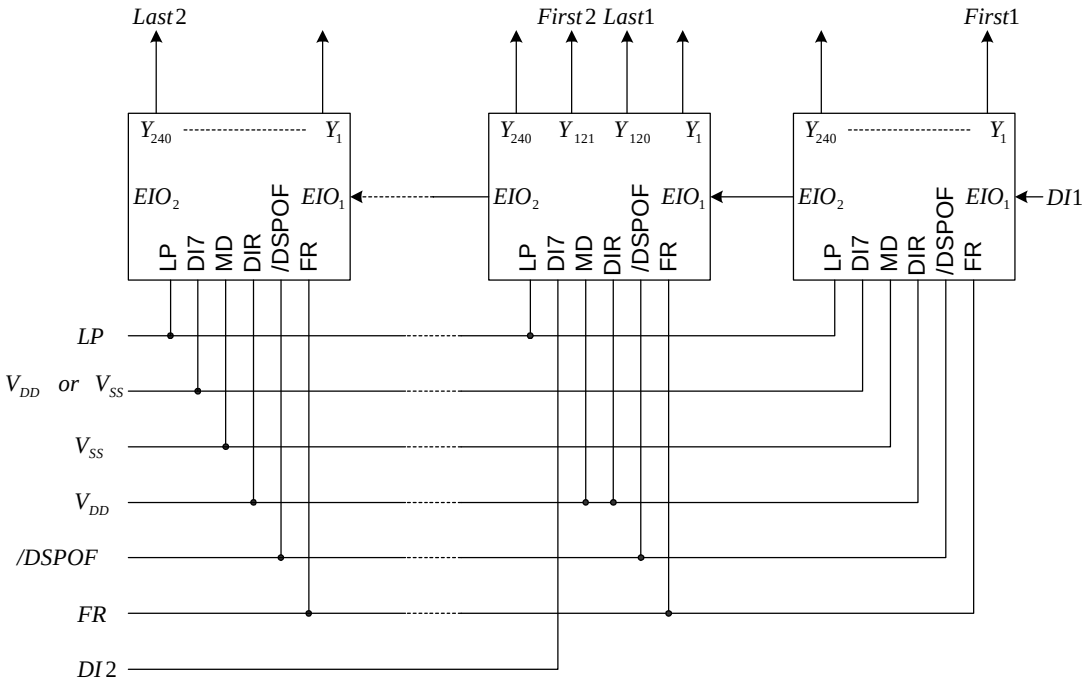
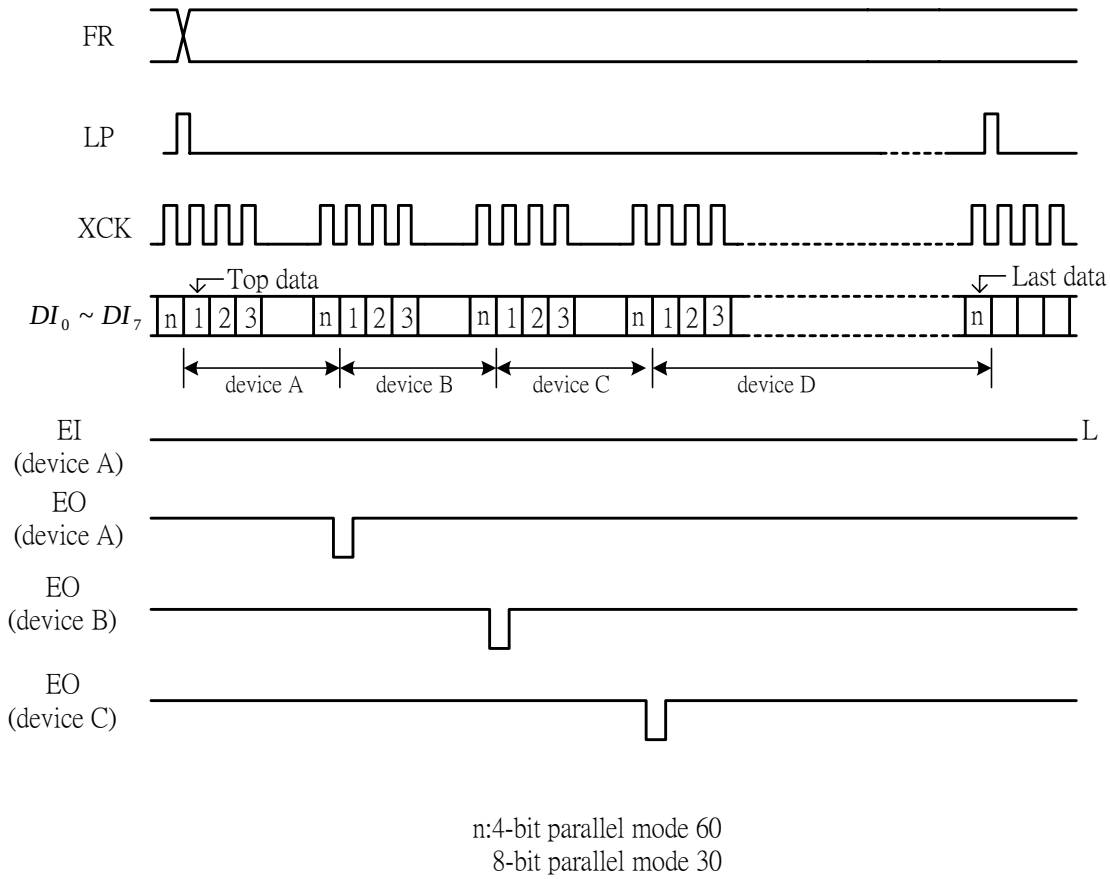


Figure 8 Dual mode DIR="H"

Timing chart of 4-device cascade connection of segment driver



n:4-bit parallel mode 60
8-bit parallel mode 30

Figure 9 Timing chart of 4-device cascade connection of segment driver

Power supply circuit for liquid crystal drive

Precaution when Connecting or Disconnecting the Power
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

. We recommend you connecting the serial resistor (50~100Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. And set up the suitable of the resistor in consideration of LCD display grade.

When connecting the power supply, show the following recommend sequence.

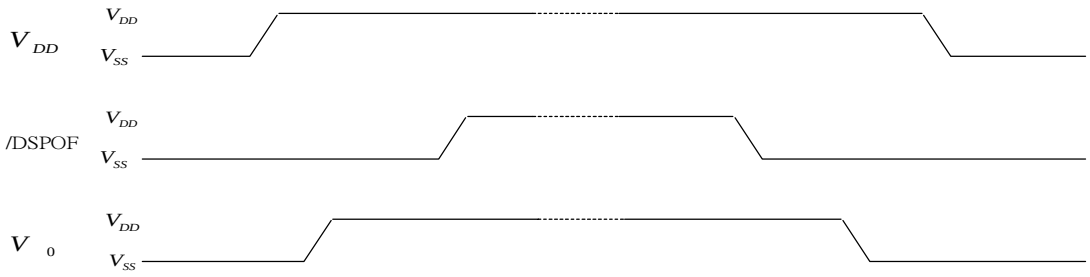


Figure 10

Drive by operational amplifier

In graphic displays, the size of the liquid crystal becomes larger and the display duty ratio becomes smaller, so the stability of liquid crystal drive level is more important than a small display system.

Since the liquid crystal for graphic display is large and has many picture elements, the load capacitance becomes large. The high impedance of power supply for liquid crystal drive produce distortion in the drive waveforms, and degrades display quality. For the reason, the liquid crystal drive level impedance should be reduced with operational amplifiers.

Range of Operating Voltage: V0

It is necessary to set the voltage for V0 within the VDD operating voltage range shown in the diagram below.

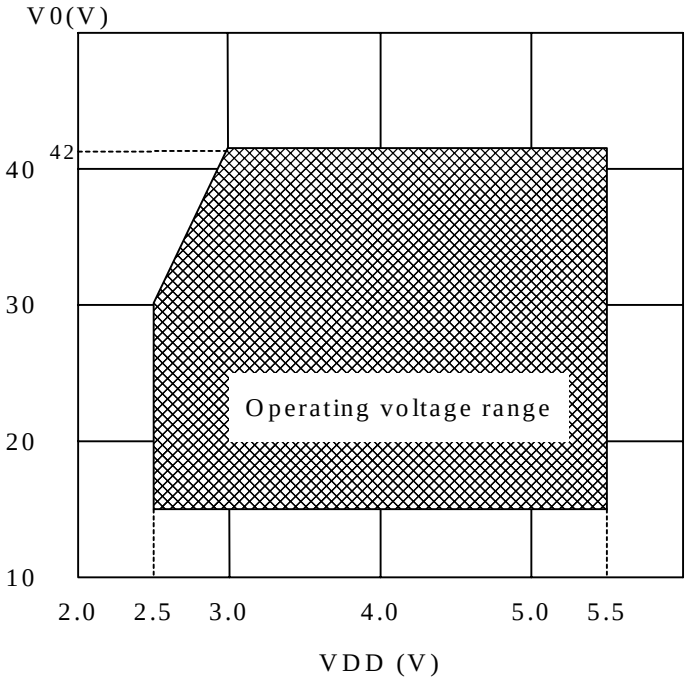


Figure 11

Preliminary

ABSOLUTE MAXIMUM RATINGS

Table 6 absolute maximum ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	T_a=25℃ Referenced to V_{SS} (0V)	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_{0-7}, XCK, LP, DIR, FR, MD, S/C, EIO_1, EIO_2, /DSPOF,$TEST_1$	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

Recommended operation conditions

Table 7 recommended operation conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced to V_{SS} (0V)	V_{DD}	+2.5		+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+15		+42	V
Operating temperature	T_{opr}			-20		+85	℃

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DC CHARACTERISTICS

Segment mode

Table 8 DC characteristics of segment mode

(V_{SS} = V_5 = 0V, V_{DD} = +2.5 to +5.5V, V_0 = +15 to +42V, T_a = -20~+85°C)

Parameter	Symbol	Conditions		Applicable pins	Min	Type	Max	Unit
Input voltage	V_{IH}			DI_0 -DI_7, XCK, LP,DIR,FR,MD, S/C,EIO_1, EIO_2, /DSPOF	0.8V_{DD}			V
	V_{IL}						0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C,EIO_1, EIO_2, /DSPOF			+10	uA
	I_{LIL}	V_I=V_{SS}					-10	uA
Output resistance	R_{ON}	|ΔV_{ON}| =0.5V	V_0=+40V	Y_1- Y_{240}		1.0	1.5	kΩ
			V_0=+30V			1.5	2.0	
			V_0=+20V			2.0	2.5	
Stand-by current	I_{STB}	*1		V_{SS}			75.0	uA
Consumed current (Deselection)	I_{DD1}	*2		V_{DD}			2.0	mA
Consumed current (Selection)	I_{DD2}	*3		V_{DD}			12.0	mA
Consumed current	I_0	*4		V_0			1.5	mA

NOTE : 1. V_{DD} = +5V, V_0 = +42V, V_I = V_{SS}

2. V_{DD} = +5V, V_0 = +42V, f_{XCK} = 20MHz, No-load, EI = V_{DD}

The input data is turned over by data taking clock (4-bit parallel input mode)

3. V_{DD} = +5V, V0 = +42V, f_{XCK} = 20MHz, No-load, EI = V_{SS}

The input data is turned over by data taking clock (4-bit parallel input mode)

4. V_{DD} = +5V, V0 = +42V, f_{XCK} = 20MHz, f_{LP} = 41.6kHz, f_{FR} = 80Hz, No-load

The input data is turned over by data taking clock (4-bit parallel input mode)

Preliminary

Common mode

Table 9 DC characteristics of common mode

(VSS = V5 = 0V, VDD = +2.5 to 5.5V, V0 = +15 to +42V, Ta = -20~85°C)

Parameter	Symbol	Conditions	Applicable pins	Min	Type	Max	Unit
Input voltage	V_{IH}		DI_0 -DI_7, XCK, LP,DIR,FR,MD, S/C,EIO_1, EIO_2, /DSPOF	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}= -0.4mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}= +0.4mA				+0.4	V
Input leakage current	I_{LIH}	VI=V_{DD}	DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C, /DSPOF			+10	uA
	I_{LIL}	V_I=V_{SS}	DI_0 -DI_7, XCK, LP, DIR, FR, MD, S/C,EIO_1, EIO_2, /DSPOF			-10	uA
Output resistance	R_{ON}	|△V_{ON}|=0.5V, V_0=+40V	Y_1- Y_{240}		1.0	1.5	kΩ
		|△V_{ON}|=0.5V, V_0=+30V			1.5	2.0	
		|△V_{ON}|=0.5V, V_0=+20V			2.0	2.5	
Input pull-down current	I_{PD}	V_I=V_{DD}	XCK,EIO_1,EIO_2, DI_7			100.0	uA
Stand-by current	I_{STB}	*1	V_{SS}			75.0	uA
Consumed current (1)	I_{DD}	*2	V_{DD}			120.0	uA
Consumed current(2)	I_0	*2	V_0			240.0	uA

NOTE: 1. V_{DD} = +5V, V_0 = +42V, V_I = V_{SS}

2. V_{DD} = +5V, V_0 = +42V, f_{LP} = 41.6kHz, f_{FR} = 80Hz, 1/480 duty, No-load

AC Electrical characteristic

Segment mode 1

Table 10 AC electrical characteristics of segment mode 1

(V_{SS} = V_5 = 0V, **V_{DD} = +4.5 to +5.5V**, V_0 = +15 to +42V, T_a = -20~85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period *1	T_{WCK}	T_R,T_F≦10ns	50			ns
Shift clock "H" pulse width	T_{WCKH}		15			ns
Shift clock "L" pulse width	T_{WCKL}		15			ns
Data setup time	T_{DS}		10			ns
Data hold time	T_{DH}		12			ns
Latch pulse "H" pulse width	T_{WLPH}		15			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		30			ns
Latch pulse rise to shift clock rise time	T_{LS}		25			ns
Latch pulse fall to shift clock fall time	T_{LH}		25			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		10			ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L=15pF			30	ns
Output delay time (2)	T_{PD1} T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

NOTES: 1. Take the cascade connection into consideration.

2. (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

Segment mode 2

Table 11 AC electrical characteristics of segment mode 2

(V_{SS} = V_5 = 0V, **V_{DD} = +3.0 to +4.5V**, V_0 = +15 to +42V, T_a = -20~8 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period *1	T_{WCK}	$T_R, T_F \leqq 10$ns	66			ns
Shift clock "H" pulse width	T_{WCKH}		23			ns
Shift clock "L" pulse width	T_{WCKL}		23			ns
Data setup time	T_{DS}		15			ns
Data hold time	T_{DH}		23			ns
Latch pulse "H" pulse width	T_{WLPH}		30			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		50			ns
Latch pulse rise to shift clock rise time	T_{LS}		30			ns
Latch pulse fall to shift clock fall time	T_{LH}		30			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		15			ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L=15pF			41	ns
Output delay time (2)	T_{PD1} T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

NOTES: 1. Take the cascade connection into consideration.

2. ($_{TWCK}$ – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

Segment mode 3

Table 12 AC electrical characteristics of segment mode 3

(V_{SS} = V_5 = 0V, **V_{DD} = +2.5 to +3.0V**, V_0 = +15 to +42V, T_a = -20~85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period *1	T_{WCK}	$T_R, T_F \leqq 10$ns	82			ns
Shift clock "H" pulse width	T_{WCKH}		28			ns
Shift clock "L" pulse width	T_{WCKL}		28			ns
Data setup time	T_{DS}		20			ns
Data hold time	T_{DH}		23			ns
Latch pulse "H" pulse width	T_{WLPH}		30			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		65			ns
Latch pulse rise to shift clock rise time	T_{LS}		30			ns
Latch pulse fall to shift clock fall time	T_{LH}		30			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		15			ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L=15pF			57	ns
Output delay time (2)	T_{PD1} T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

NOTES: 1. Take the cascade connection into consideration.

2. ($T_{WCK} - T_{WCKH} - T_{WCKL}$) / 2 is maximum in the case of high speed operation.

Common mode

Table 13 AC electrical characteristics of common mode

(V_{SS} = V_5 = 0V, V_{DD} = +2.5 to +5.5V, V_0 = +15 to +42V, T_a = -20~+85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period	T_{WLP}	T_R,$T_F \leqq$ 20ns	250			ns
Shift "H" pulse width	T_{WLPH}	V_{DD}=+5.0V±10%	15			ns
		V_{DD}=+2.5V~+4.5V	30			ns
Data setup time	T_{SU}		30			ns
Data hold time	T_H		50			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
/DSPOF removal time	T_{SD}		100			ns
/DSPOF "L" pulse time	T_{WDL}		1.2			us
Output delay time (1)	T_{DL}	C_L=15pF			200	ns
Output delay time (2)	T_{PD1},T_{PD2}	C_L=15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L=15pF			1.2	us

TIMING DIAGRAMS

Timing characteristics of segment mode

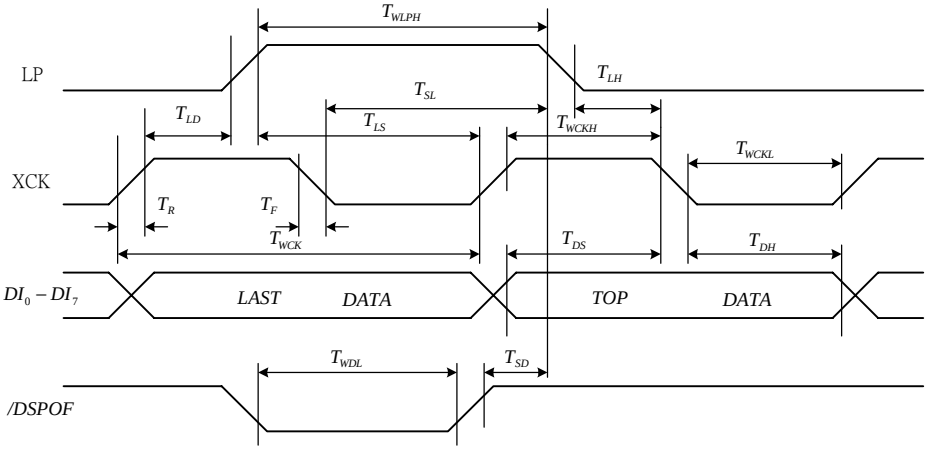


Figure 12

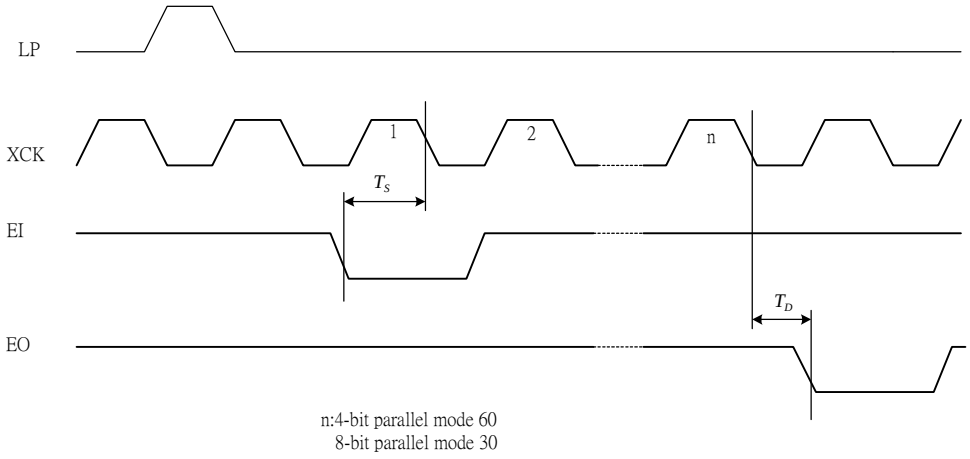


Figure 13

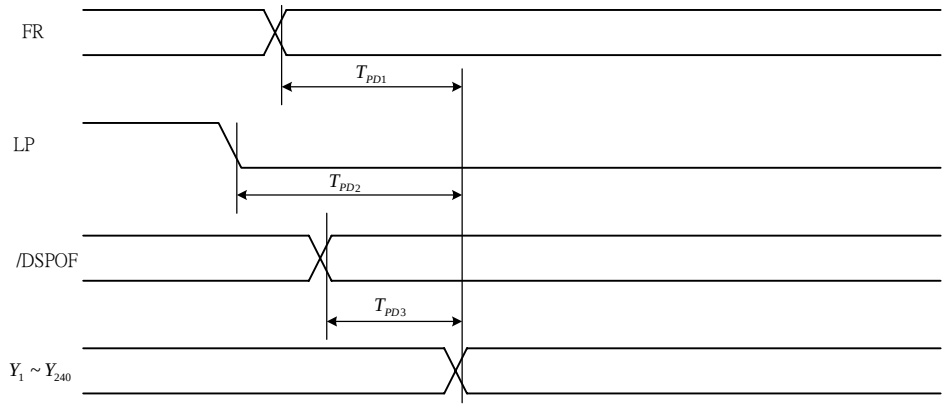


Figure 14

Timing characteristics of common mode

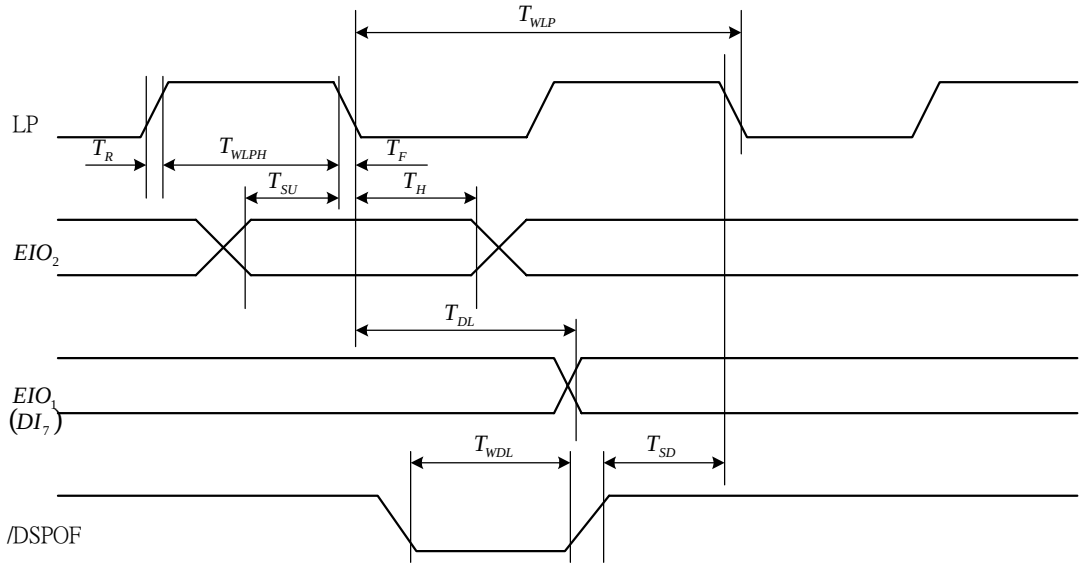


Figure 15

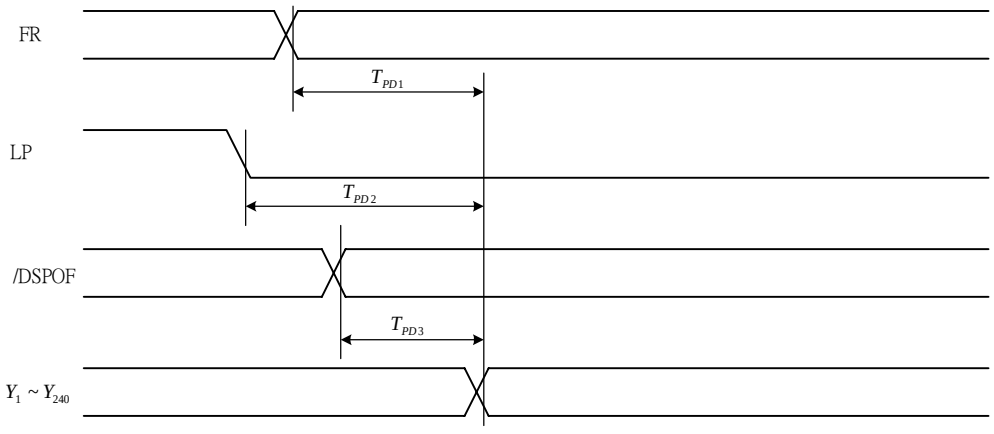


Figure 16

Preliminary

APPLICATION CIRCUIT

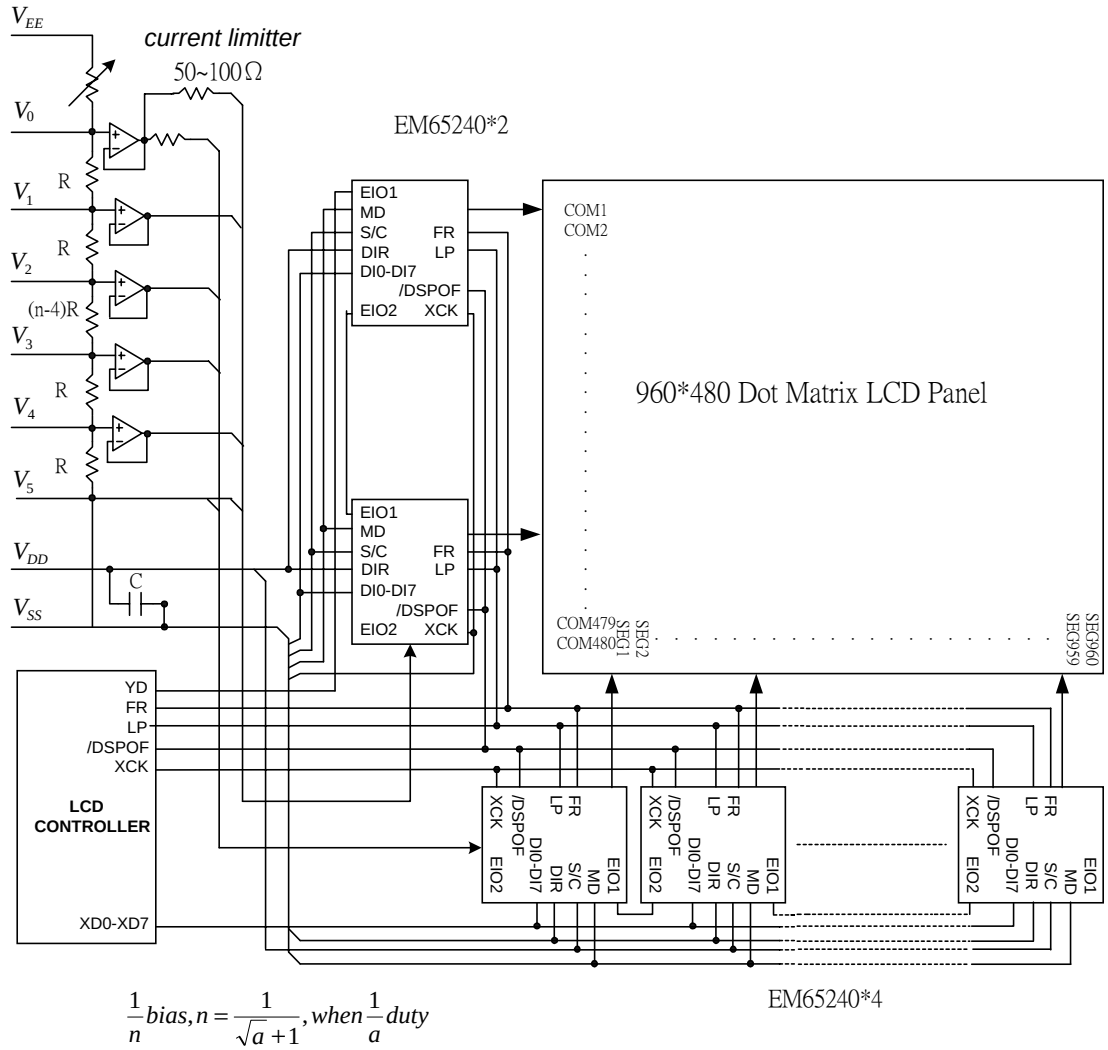


Figure 17 Application circuit of 960*480 dot matrix LCD panel

Preliminary

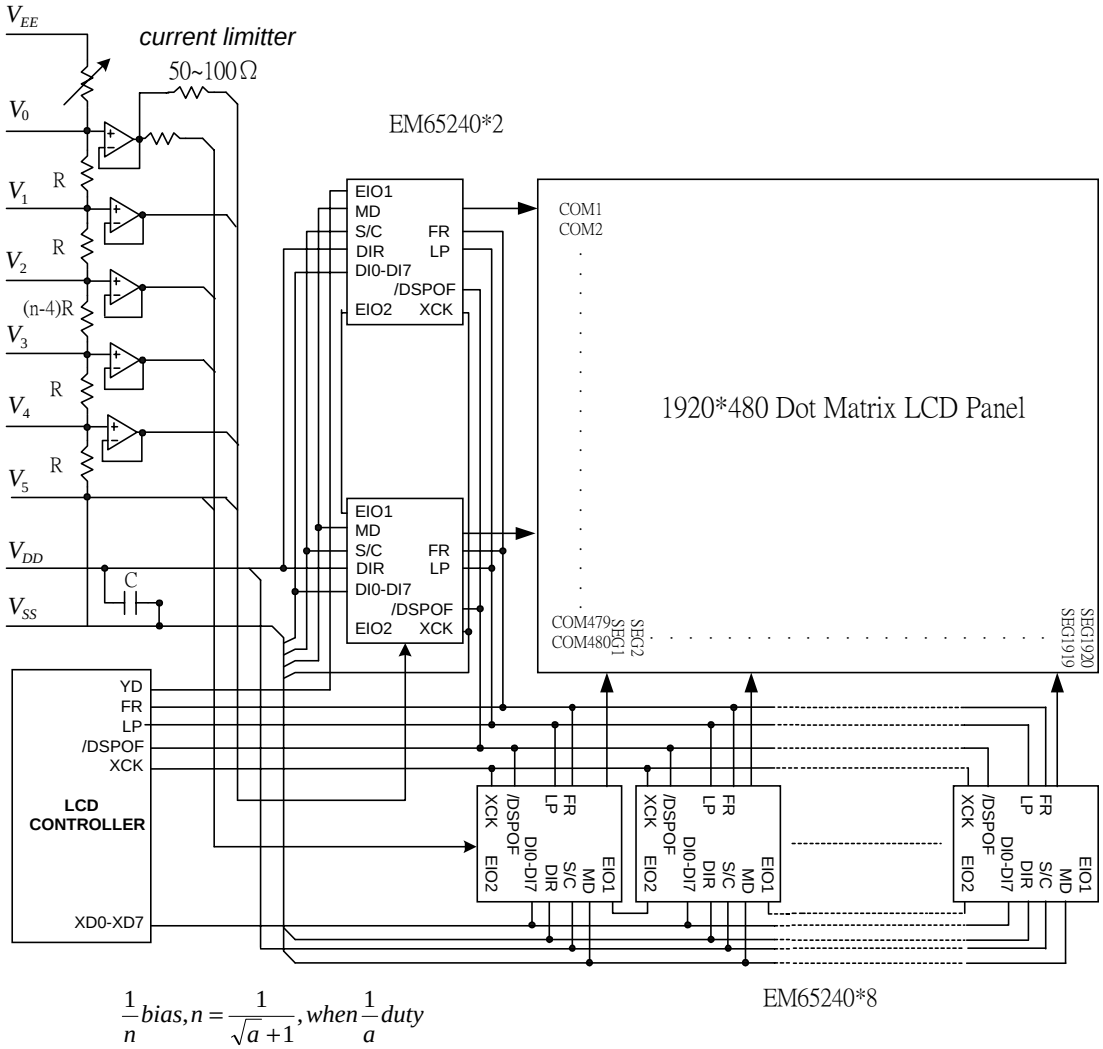
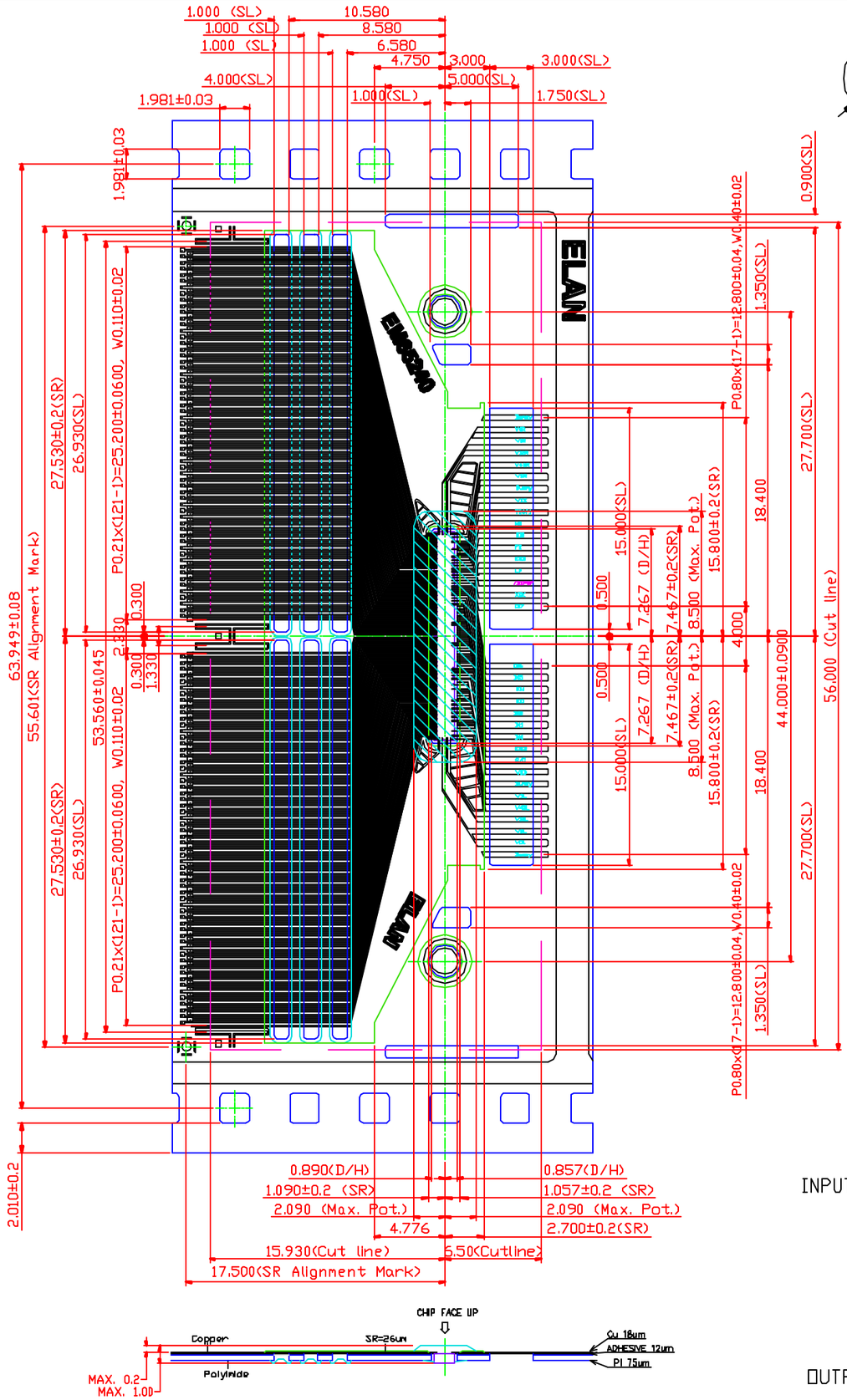
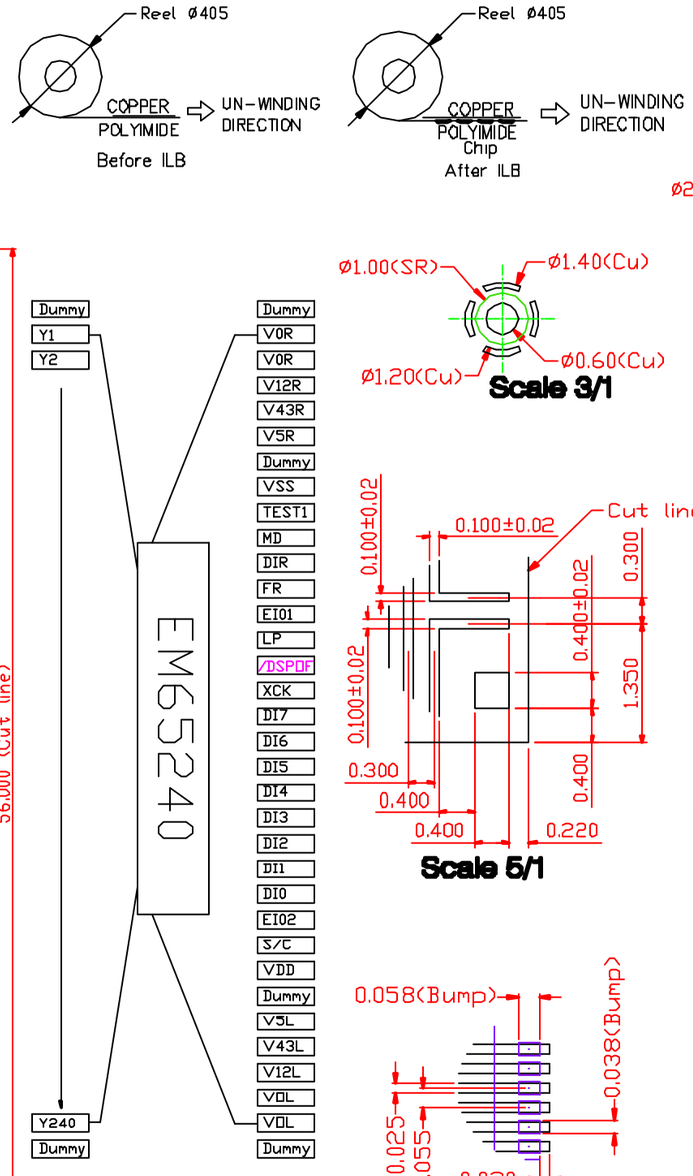
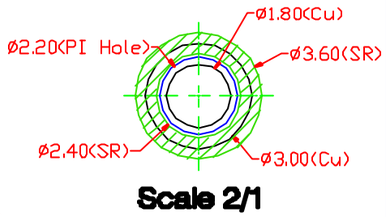
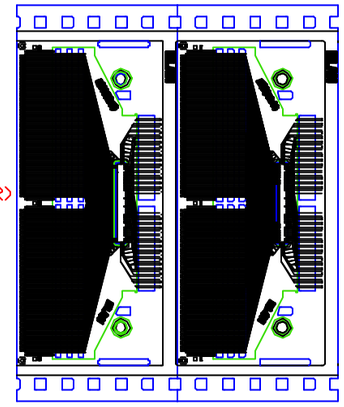


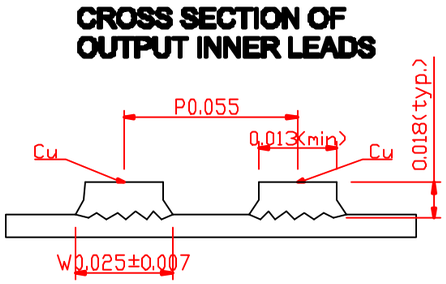
Figure 18 Application circuit of 1920*480 dot matrix LCD panel

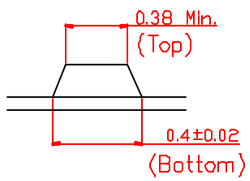




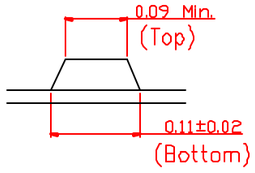




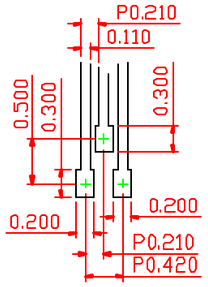




INPUT SIDE OL CROSS SECTION



OUTPUT SIDE OL CROSS SECTION



Layer Definition

Layer 0	General	□	Layer 5	Pinnr	□			Layer 11	Help_Une	□	
Layer 1	Copper	□	Layer 6	Leadnr	□			Layer 12	Center line	□	
Layer 2	Polyimid	□	Layer 7	Cutline	□			Layer 13	Punch	□	
Layer 3	Solderresist	□	Layer 8	Potting	□						
Layer 4	Chip	□	Layer 9	Dimension	□						

Material Description

1.Space Tape Material	Polyester(PET)		Dainichi Kosei
Leader Tape Material	Polyimide(PI)		UBE
PKG Reel Size	405mm		Gold
Polyimide	UPILEX-S	75±6 um	UBE
Adhesive	#7100	12±3 um	Toray
Copper	FQ-VLP	18±5 um	Mitsui
Plating	Sn	0.21±0.05 um	WUS
Flex coating	FS-100L	0.21±0.05 um	WUS
Solder Resist	AR-710D	Min 10um	WUS

Solder Resist Tolerance. ±0.200mm
2.ALL CHAMFER IS R0.200mm.
3. 5 SPROCKET HOLES (70W) FOR 1TAPESITE
4.Etchingfactor >2.5 for all pattern.

Item	Drawing Modification	Date
1		
2		
3		
4		

Unless Otherwise Specified			International Semiconductor Technology LTD.				Scale		Proj
Unit	mm						Subpack code		
Tolerance			EM65240 Outline Drawing				Material PI		
Dimension	±0.05								
Angle	±1°								
SIGN	Drawn	Checked	ILB REVIEW	POT REVIEW	FT REVIEW	Approved	Drawing No		Rev
By	Jenny Chu								1
Date	05-04-01						Sheet	1 Of 1	Size A4