T-46-19-07

pLSI™ 1048/883

programmable Large Scale Integration
High-Density Programmable Logic

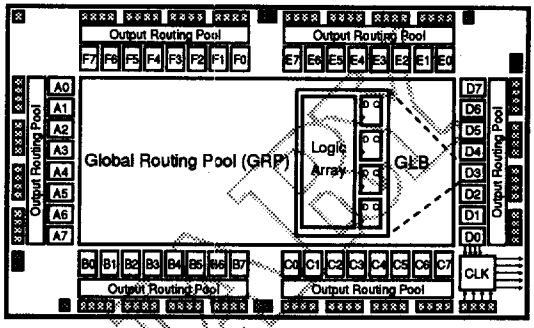
Features

- **PROGRAMMABLE HIGH-DENSITY LOGIC**
  - — MIL-STD-883 Version of the pLSI 1048
  - — High-Speed Global Interconnects
  - — 96 I/O Pins, Ten Dedicated Inputs
  - — 288 Registers
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
  - — Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 50 MHz Maximum Operating Frequency
  - — t_{pd} = 24 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Re-Programmable
  - — 100% Tested
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device can Combine Glue Logic and Structured Designs
  - — 100% Routable with High Utilization
  - — Four Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Allows Global Interconnectivity
- **pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)**

  pDS Software
  - — Easy to Use PC Windows™ Interface
  - — Boolean Logic Compiler
  - — Manual Partitioning
  - — Automatic Place and Route
  - — Static Timing Table

  pDS+™ Software
  - — Industry Standard, Third Party Design Environments
  - — Schematic Capture, State Machine, VHDL
  - — Automatic Partitioning
  - — Automatic Place and Route
  - — Comprehensive Logic and Timing Simulation
  - — PC and Workstation Platforms

Functional Block Diagram



Description

The Lattice MIL-STD-883 pLSI 1048 is a High-Density Programmable Logic Device which contains 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1048/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..F7, (see figure 1). There are a total of 48 GLBs in the pLSI 1048/883 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

5

PRELIMINARY

Copyright © 1992 Lattice Semiconductor Corp. GAL, E²CMOS and UltraMOS are registered trademarks of Lattice Semiconductor Corp. pLSI, ispLSI, pDS, pDS+ and Generic Array Logic are trademarks of Lattice Semiconductor Corp. The specifications and information herein are subject to change without notice.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; FAX (503) 681-3037; Applications Hotline: 1-800-LATTICE (528-8423)

September 1992. Rev. A

T-46-19-07

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Ambient Temp. with Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

PRELIMINARY

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	+125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention (at 55°C)	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

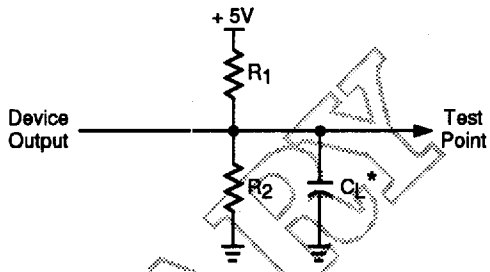
Switching Test Conditions

T-46-19-07

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$	–	–	10	µA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \le V_{IN} \le V_{IL}$	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT}	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 20 MHz	–	165	260	mA

1. One output at a time for a maximum duration of one second (25°C only).
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_C = 25°C.

PRELIMINARY

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-50		UNITS
				MIN.	MAX.	
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	24	ns
t_{pd2}	1	2	Data Propagation Delay, Worst Case Path	–	30.7	ns
f_{max}	1	3	Clock Frequency with Internal Feedback[3]	53.6	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	31.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	12	–	ns
t_{co1}	1	7	GLB Reg. Clock to Output Delay, ORP bypass	–	16	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	16	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	18.7	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	ns
t_{r1}	1	12	Ext. Reset Pin to Output Delay	–	22.7	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	13	–	ns
t_{en}	2	14	Input to Output Enable	–	26.7	ns
t_{dis}	3	15	Input to Output Disable	–	26.7	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	7	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	7	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.7	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

PRELIMINARY

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50 MIN.	-50 MAX.	UNITS
Inputs					
tiobp	20	I/O Register Bypass	–	4.0	ns
tiolat	21	I/O Latch Delay	–	5.3	ns
tiosu	22	I/O Register Setup Time before Clock	8.1	–	ns
tioh	23	I/O Register Hold Time after Clock	0.9	–	ns
tioco	24	I/O Register Clock to Out Delay	–	3.9	ns
tior	25	I/O Register Reset to Out Delay	–	4.6	ns
tdin	26	Dedicated Input Delay	–	8.0	ns
GRP					
tgrp1	27	GRP Delay, 1 GLB Load	–	3.3	ns
tgrp4	28	GRP Delay, 4 GLB Loads	–	4.0	ns
tgrp8	29	GRP Delay, 8 GLB Loads	–	5.3	ns
tgrp12	30	GRP Delay, 12 GLB Loads	–	6.7	ns
tgrp16	31	GRP Delay, 16 GLB Loads	–	8.0	ns
tgrp48	32	GRP Delay, 48 GLB Loads	–	21.3	ns
GLB					
t4ptbp	33	4 Product Term Bypass Path Delay	–	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	–	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	–	10.0	ns
txoradj	36	XOR Adjacent Path Delay[3]	–	12.7	ns
tgbp	37	GLB Register Bypass Delay	–	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	2.0	–	ns
tgh	39	GLB Register Hold Time after Clock	8.0	–	ns
tgco	40	GLB Register Clock to Output Delay	–	3.3	ns
tgr	41	GLB Register Reset to Output Delay	–	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	–	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	11.9	ns
tptck	44	GLB Product Term Clock Delay	4.6	9.9	ns
ORP					
torp	45	ORP Delay	–	4.7	ns
torpbp	46	ORP Bypass Delay	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

PRELIMINARY

5

Lattice

T-46-19-07

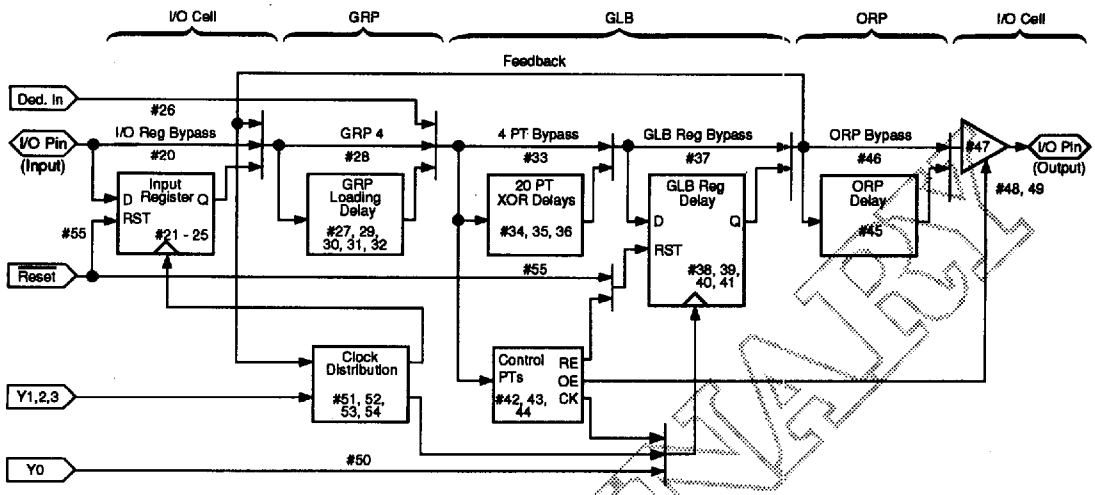
Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-50		UNITS
			MIN.	MAX.	
Outputs					
t_{ob}	47	Output Buffer Delay	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	6.7	ns
Clocks					
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.3	6.6	ns
Global Reset					
t_{gr}	55	Global Reset to GLB and I/O Registers	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

PRELIMINARY

pLSI 1048 883 Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$
= (#20 + #28 + #35) + (#38) - (#20 + #28 + #44)
7.4 ns = (4.0 + 4.0 + 10.0) + (2.0) - (4.0 + 4.0 + 4.6)

th = Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= (#20 + #28 + #44) + (#39) - (#20 + #28 + #35)
7.9 ns = (4.0 + 4.0 + 9.9) + (8.0) - (4.0 + 4.0 + 10.0)

tco = Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= (#20 + #28 + #44) + (#40) + (#45 + #47)
29.9 ns = (4.0 + 4.0 + 9.9) + (3.3) + (4.7 + 4.0)

Derivations of tsu, th and tco from the Clock GLB

tsu = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$
= (#20 + #28 + #35) + (#38) - (#50 + #40 + #52)
8.7 ns = (4.0 + 4.0 + 10.0) + (2.0) - (6.7 + 3.3 + 1.3)

th = Clock (max) + Reg h - Logic
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= (#50 + #40 + #52) + (#39) - (#20 + #28 + #35)
6.6 ns = (6.7 + 3.3 + 6.6) + (8.0) - (4.0 + 4.0 + 10.0)

tco = Clock (max) + Reg co + Output
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= (#50 + #40 + #52) + (#40) + (#45 + #47)
28.6 ns = (6.7 + 3.3 + 6.6) + (3.3) + (4.7 + 4.0)

PRELIMINARY

Pin Description

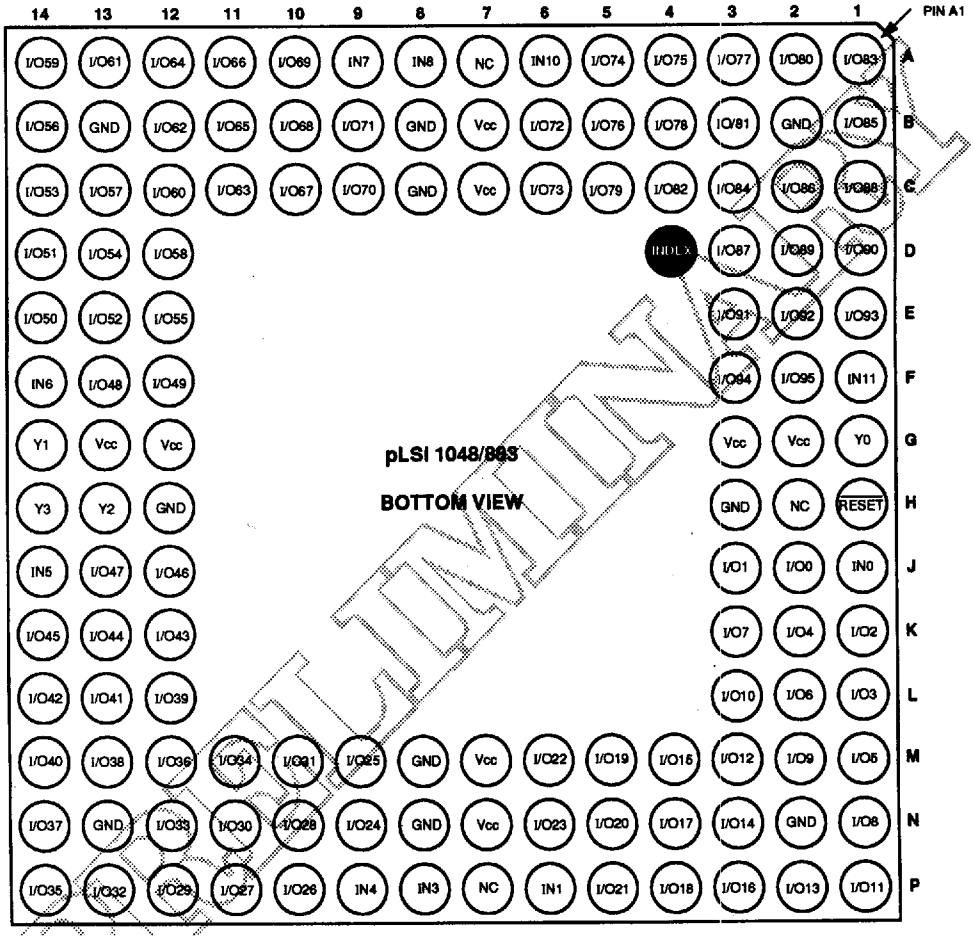
Name	PGA Pin Numbers	Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	J2, J3, K1, L1, K2, M1, L2, K3, N1, M2, L3, P1, M3, P2, N3, M4, P3, N4, P4, M5 N5, P5, M6, N6, N9, M9, P10, P11, N10, P12, N11, M10, P13, N12, M11, P14, M12, N14, M13, L12, M14, L13, L14, K12, K13, K14, J12, J13, F13, F12, E14, D14, E13, C14, D13, E12, B14, C13, D12, A14, C12, A13, B12, C11, A12, B11, A11, C10, B10, A10, C9, B9, B6, C6, A5, A4, B5, A3, B4, C5, A2, B3, C4, A1, C3, B1, C2, D3, C1, D2, D1, E3, E2, E1, F3, F2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 5 IN 6 - IN 11	J1, P6, —, P8, P9, J14, F14, A9, A8, —, A6, F1	Dedicated input pins to the device. (IN 2 and IN 9 not available)
$\overline{\text{RESET}}$	H1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	G1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	G14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	H13	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	H14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	B2, B8, B13, C8, H3, H12, M8, N2, N8, N13	Ground (GND)
V_{CC}	B7, C7, G2, G3, G12, G13, M7, N7	V_{CC}
NC	A7, P7, H2	These pins should be left floating, never connect these pins to ground.

PRELIMINARY

Pin Configuration

pLSI 1048/883 PGA Pinout Diagram

T-46-19-07



PRELIMINARY

5

Lattice

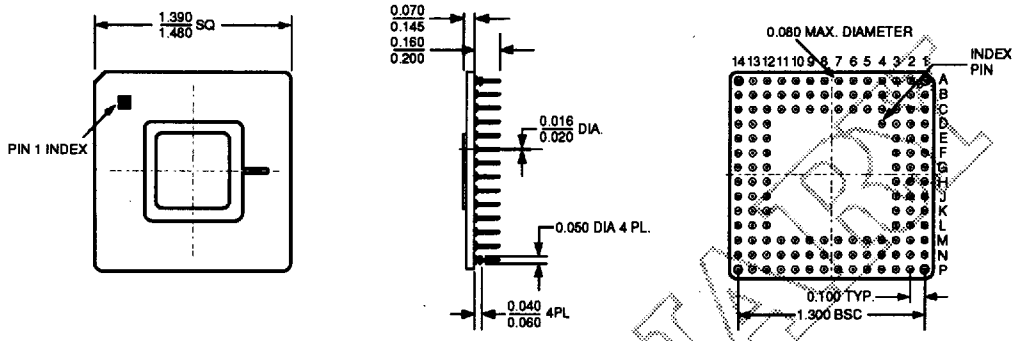
Specifications *pLSI 1048/883*

T-46-19-07

Package Diagram

132-Pin PGA

Dimensions in inches MIN./MAX.



Part Number Description

pLSI 1048 – XX X X X

Device Family

Device Number

Speed
50 = 50 MHz fmax

Power
L = Low

Package
G = 132-Pin PGA

MIL Process /883 = 883 Process

Ordering Information

fmax (MHz)	tpd (ns)	Ordering Number	Package
50	24	pLSI 1048-50LG/883	132-Pin PGA

PRELIMINARY