Consumer Microcircuits Limited

MIXED SIGNAL SOLUTIONS

Product Information

Obsolete Product
For Information Only

Features

- A 17-Tone generator
- ZVEI, CCIR, EEA Tonesets
- Fully programmable
- Low power CMOS
- Automatic repeat function
- On-chip tone timer
- Low-distortion sinewave o/p
- TX delay facility

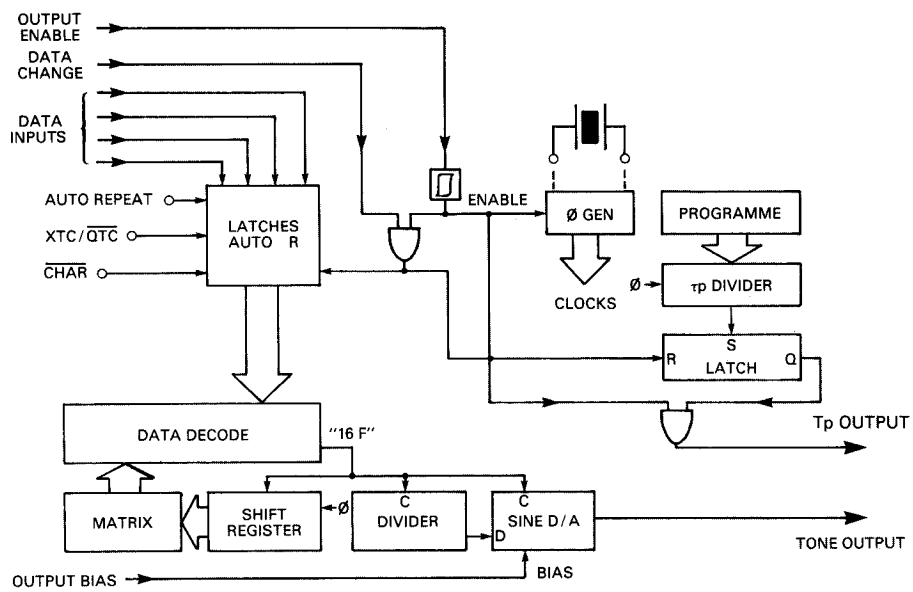


Fig. 1 Internal Block Diagram

FX503C
FX503E
FX503Z
FX503ZS

Brief Description

The FX503 is a CMOS fully programmable 17-tone generator which may be used as a selcall encoder for CCIR, ZVEI and EEA tone standards. An FX503 is also available for the EIA tone standard (see separate datasheet). The output tone is a low-distortion 16-step pseudo sinewave whose frequency is selected by four programming inputs. Tone period timing is controlled by an externally applied 'data change' input. Alternatively, the device has an onboard timer which outputs either 100, 70 or 40 ms timed outputs, depending on the tone version used.

This output may be linked to the data change input to achieve 'self timing' of the tone period. The device has an AUTO REPEAT function which will cause it to automatically insert the 'Repeat' tone when consecutive tone numbers are the same. A TX delay facility is available to allow for the transmitter 'power up' time.

All tone frequencies and internal timings are controlled by a 560 kHz reference oscillator comprising an on-chip inverter and external resonator/XTAL. Alternatively an external clock may be used.

Pin Description Function

(See Figure 2)

D.I.L. FX503*	Chip Carrier FX503*K	* C, E, Z, ZS
1	1	**Tone Output:** A 16-step pseudo-sinewave giving a low distortion output. Can be biased to approximately 40% VDD by use of the output bias or disabled (to VSS) by use of the output enable.
2	2	**Tp Output:** A tone period timer programmed to the appropriate international standards. The Tp output can be used to strobe the next data into the FX503 by connecting it to the D/C I/P. The tone period timer is started and goes to logic'0' after receipt of an output enable 0-1 edge or D/C 0-1 edge. After the appropriate timed period the Tp output is reset to logic'1'. Timing restarts at subsequent D/C 0-1 edges.
3	3	**Output Bias:** Connecting this output to the 'Output Enable' pin causes the 'Tone Output' voltage to move to the d.c. bias level before this output is enabled, (i.e. generates a tone output).
4	5	**Output Enable:** Schmitt Input: A logic 1 applied to this input will enable the encoder and send the first tone, after a delay Td. Td is set by an external RC time constant. A logic 0 applied to this input will disable the Tone Output and set the Tone Output to VSS, thus reducing current consumption.
5	8	**Data Change:** Controls the output in two ways: A logic 0-1 transition will send the appropriate tone, controlled by the data inputs. A logic 1-0 transition latches the input data until the next 0-1 data change transition.
6	9	**Auto Repeat:** A logic 1 will enable the auto repeat circuitry: two consecutive equal data (D_0-D_3) characters will output the character tone followed by the repeat tone. A logic 0, under the same condition, will cause the FX503 to generate the character tone on both occasions.
7	14	**XTC/$\overline{\text{QTC}}$:** Logic 1 sets the XTC mode which is full HEX character set and repeat tone. Logic 0 sets QTC mode which is 14 characters and repeat tone.
8	15	**VSS:** Negative Supply.
9	17 D_0	**Data Inputs:** These inputs set the value of the tone frequency generated, under the control of 'Data Change' and 'Output Enable' 0-1 edges.
10	18 D_1	
11	19 D_2	
12	20 D_3	
13	24	**$\overline{\text{Character I/P}}$:** Acts as a fifth data input. Logic 1 overrides D_0-D_3 (but still strobed by D/C) and sets tone output to 40% VDD until new data is loaded. Logic 0 sets QTC mode: 14 characters plus repeat tone E.
14	26	**Xtal/clock:** The input to an on-chip inverter for use with a 560 kHz ceramic resonator. Alternatively, an external clock may be used.
15	27	**$\overline{\text{Xtal}}$**
16	28	**VDD: Positive Supply.**
—	4, 6, 7, 10, 11, 12, 13, 16, 21, 22, 23, 25.	**Not Connected.**

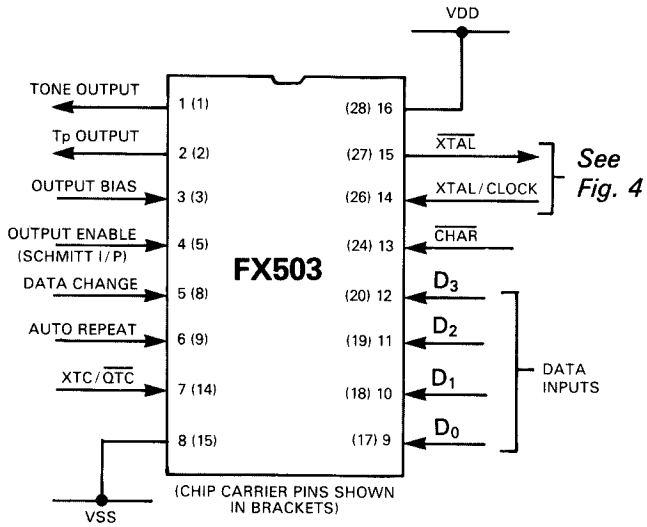


Fig. 2 External Component Connections

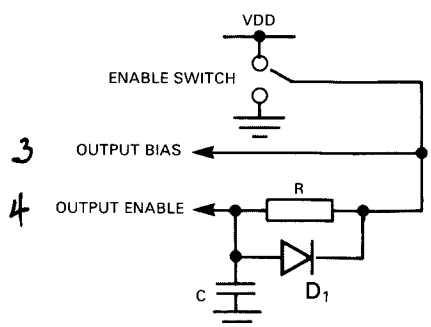


Fig. 3 Transmit Delay Circuit (See Note 3)

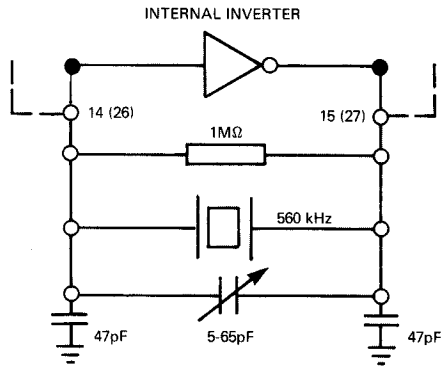


Fig. 4 560 kHz Resonator Circuit (See Notes 1 & 2)

Notes

1. Output frequency and tone period are internally divided from the input clock frequency. Output stabilities with time, temperature and supply voltage are directly proportional to input clock accuracy.

2. **Calibration Procedure for Ceramic Resonator Oscillator**
To ensure that the generated outputs are correct the oscillator frequency must be 560.0 kHz. The loading of a frequency counter on the oscillator circuitry can cause an error. The preferred method is to monitor Pin 1 while the FX503 is generating a tone (exact set-up conditions will depend on the system arrangement). Adjust the oscillator to obtain a tone output as stated below.

FX503 Calibration Tones.

ZVEI	*FX503Z*	*Use tone*	*4*	*1400 Hz*
			or 8	*2000 Hz*
			or A	*2800 Hz*
ZVEI(S)	*FX503ZS*	*Use tone*	*4*	*1400 Hz*
			or 8	*2000 Hz*
CCIR	*FX503C*	*Use tone*	*D*	*991·14 Hz*
EEA	*FX503E*	*Use tone*	*B*	*930·2 Hz*

3. **Transmit Delay Function**
A transmit delay can be arranged as shown in Figure 3. *The tone output will step to the bias condition for the delay period before commencing to generate tones.*

4. Tone frequency (Hz) obtained with the Oscillator set to 560.0 kHz.

Format Characters		Data Inputs	**Tone frequency (Hz)** *(See Note 4)*			
			FX503C	**FX503E**	**FX503Z**	**FX503ZS**
QTC	XTC	D_3 D_2 D_1 D_0	CCIR	EEA	ZVEI	ZVEI(S)
0	0	0000	1981	1981	2400	2400
1	1	0001	1124	1124	1060	1060
2	2	0010	1197	1197	1160	1160
3	3	0011	1275	1275	1270	1270
4	4	0100	1358	1358	1400	1400
5	5	0101	1446	1446	1530	1530
6	6	0110	1540	1540	1670	1670
7	7	0111	1640	1640	1830	1830
8	8	1000	1747	1747	2000	2000
9	9	1001	1860	1860	2200	2200
A (Group)	A (Group)	1010	2400	1055	2800	886
B	B	1011	930	930	810	810
C	C	1100	2247	2247	970	740
D	D	1101	991	991	886	680
E (Repeat)		1110	2110	2110	2600	970
F		1111	NOTONE	NOTONE	NOTONE	NOTONE
	E	1110	873	873	740	—
	F	1111	1055	2400	680	—
	X (Repeat)	—	2110	2110	2600	—

NOTE: FX503ZS only QTC Character Format

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

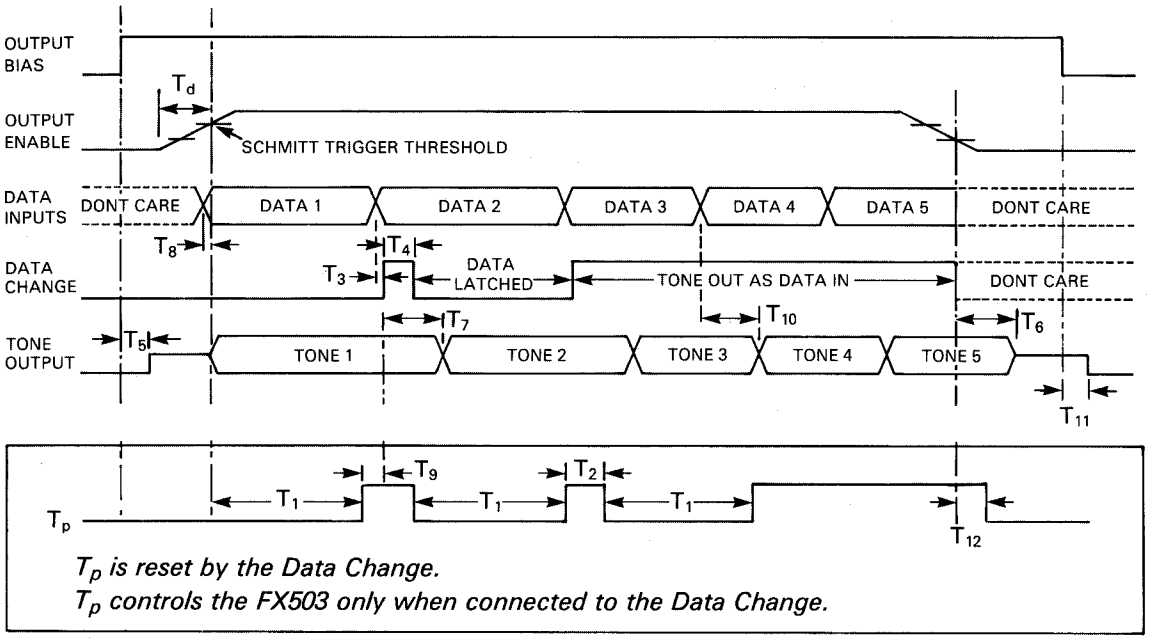
Supply voltage	−0.3V to 7.0V
Input voltage at any pin (ref VSS = OV)	−0.3V to (VDD + 0.3V)
Output sink/source current (total)	20mA
Operating temperature range: FX503 } FX503K }	−30°C to +85°C
Storage temperature: FX503 } FX503K }	−55°C to 125°C
Maximum device dissipation	100mW

Operating Limits

VDD = 5V, T_A = 25°C, Ø = 560kHz, $\Delta f\emptyset$ = 0.
All characteristics measured using the standard circuit with the following test parameters, and is valid for all tones unless otherwise stated:—

Characteristic	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5	5.5	V
Supply current (standby no tone output)	1	0.9	1.2	1.5	mA
Supply current (transmitting tone output)	1	1.9	2.2	2.5	mA
Tone output impedance			1		kΩ
Logic '1' output I source = 0.1 mA	2	4.0			V
Logic '0' output I sink = 0.1 mA	2			1.0	V
Logic '1' input Level	3	3.5			V
Logic 'O' input level	3			1.5	V
Input level to activate pin 4	4	2.8	3.1	3.3	V
Input level to deactivate pin 4	4	1.5	1.6	1.7	V
Dynamic Characteristics					
Tone output level (relative 775mV rms)		−3	0		dB
Tone frequency accuracy FX503C			*f*o ± 4		Hz
FX503E			*f*o ± 0.3		%
FX503Z			*f*o ± 0.3		%
FX503ZS			*f*o ± 0.3		%
Tone output risetime to 90% nominal O/P:			—		—
Tone output load current . . .			—		—
Total harmonic distortion . . .			7.5		%
Tone period accuracy FX503C			100 ± 0.01%		ms
FX503E			40 ± 0.01%		ms
FX503Z			70 ± 0.01%		ms
FX503ZS			70 ± 0.01%		ms

Notes *1. No load connected.*
2. Pin 2.
3. Pins 3, 6, 7 and 9-13
4. Schmitt trigger input.



NOT DRAWN TO SCALE

Fig. 5 Timing Diagram (See References)

References:

Td as required
T_1 (Tone period) See Character Tone Table
T_2 Minimum 4μs
T_3 (Data Set-up time) minimum 0μs
T_4 (Data Change) minimum 4μs

T_5 (Delay from pin 3 = '1' to O/P $\approx \frac{VDD}{2}$) 4μs
T_6 (Delay from pin 4 = '0' to O/P VSS) 8μs
T_7 (Delay from D.C. = '1' to f_O change) 12μs
T_8 (Data Set-up time) minimum 0μs
T_9 (Delay between T_p expired and Data Change rising edge) minimum 0μs
T_{10}, T_{11}, T_{12} approximately 4μs

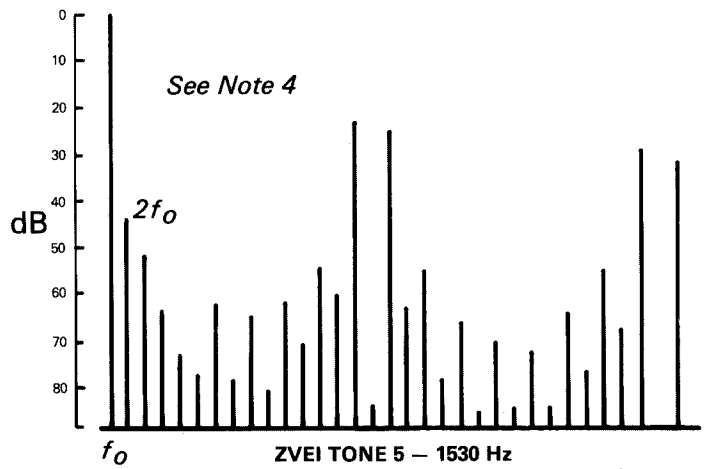


Fig. 6 Output Frequency Spectrum

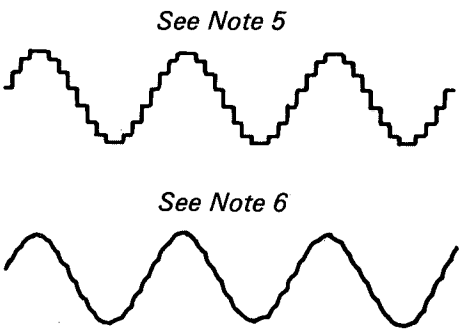


Fig. 7 Tone 5 ZVEI 1530 Hz

Notes

4. *The harmonic distribution for tone 5 of the ZVEI system — 1530 Hz as generated by the FX503Z.*
5. *The unfiltered tone output (pin 1)*
6. *The tone output produced after simple filtering by connecting a 22ηF capacitor between the output and VSS.*

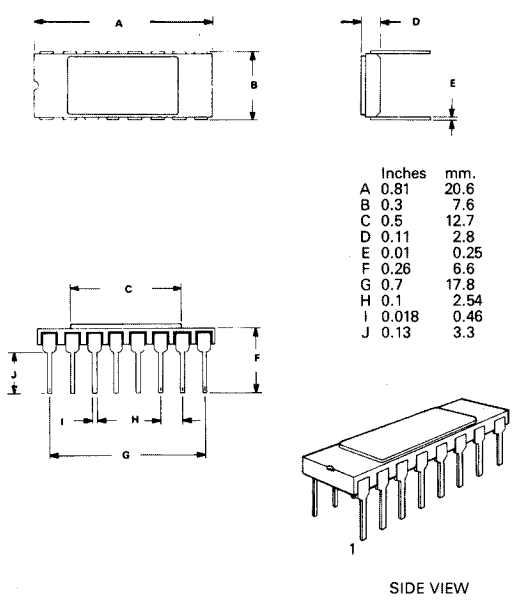
Package Outlines

The ceramic dual-in-line package of the FX503 is shown in *Figure 8* and the chip carrier version shown in *Figure 9.* For the D.I.L. package, the pins number counter-clockwise (top view) from 1 with reference to a notch as a guidance. For the chip carrier package, pins number clockwise (underneath view) from the long pad (pad 1).

Handling Precautions

The FX503 is a CMOS LSI integrated circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

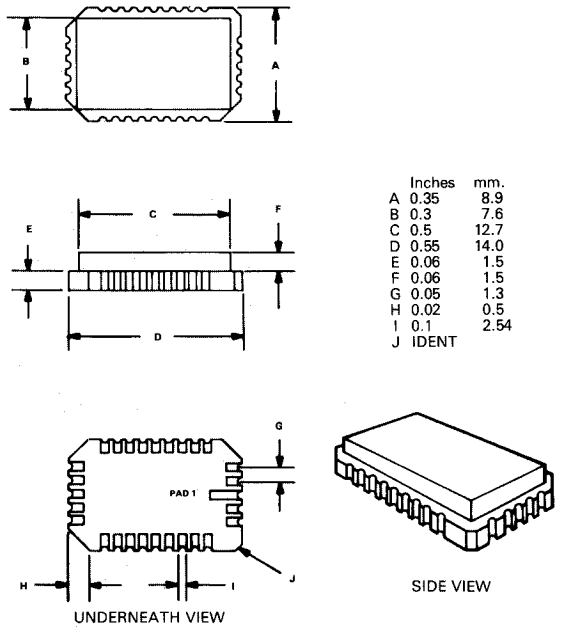
Fig. 8 ***FX503*** *D.I.L. Package*



	Inches	mm.
A	0.81	20.6
B	0.3	7.6
C	0.5	12.7
D	0.11	2.8
E	0.01	0.25
F	0.26	6.6
G	0.7	17.8
H	0.1	2.54
I	0.018	0.46
J	0.13	3.3

SIDE VIEW

Fig. 9 ***FX503K*** *Chip Carrier Package*



	Inches	mm.
A	0.35	8.9
B	0.3	7.6
C	0.5	12.7
D	0.55	14.0
E	0.06	1.5
F	0.06	1.5
G	0.05	1.3
H	0.02	0.5
I	0.1	2.54
J	IDENT	

UNDERNEATH VIEW

SIDE VIEW

Ordering Information

FX503*	**16-pin Ceramic D.I.L.**
FX503*K	**28-pad Ceramic Chip Carrier**

**** VERSIONS***

C : CCIR
E : EEA
Z : ZVEI
ZS : Suppressed ZVEI

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.

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