PRELIMINARY

DATA SHEET

ZyMOS

Zy16C452™

Dual Asynchronous Serial/Parallel Port

T-75-37-05

FEATURES

* fully IBM PC AT ™-compatible and POACH/AT ™-compatible
* compatible with industry-standard 16C452 having shared microprocessor interface
* single clock source of 1.8432 MHz, 2.4576 MHz or 3.072 MHz
* dual-channel version of the 16C450
* bi-directional parallel port

UART features for each channel include:

- o independent control of transmit, receive, line status and data set interrupts
- o individual modem control signals (CTS, RTS, DSR, DTR, RI and DCD)
- o programmable interface characteristics for:
  - five-, six-, seven- or eight-bit characters
  - even-, odd- or no-parity bit generation and detection
  - one-, one-and-one-half-, or two-stop bit generation
  - baud generation (50 to 56K baud)
- o programmable baud generator allows division of the input clock by 1 to (2^{16} - 1) and generates an internal X16 clock
- o false start bit detection
- o complete status reporting capability
- o internal diagnostic capabilities
  - loopback controls for communications link fault isolation
  - break, parity overrun, framing error simulation

Centronics™ printer interface

- o bidirectional parallel port
- o fully compatible with IBM parallel port implementation
- o supports asynchronous 8-bit parallel 'handshake' operation

* minimum discrete components
* three-state TTL output drive and input levels
* low-power CHMOS-3 technology
* available in 68-pin PLCC package
* customized versions supported
* microprocessor peripheral functions are also available as standard cells in the ZyMOS cell library for unique design integration

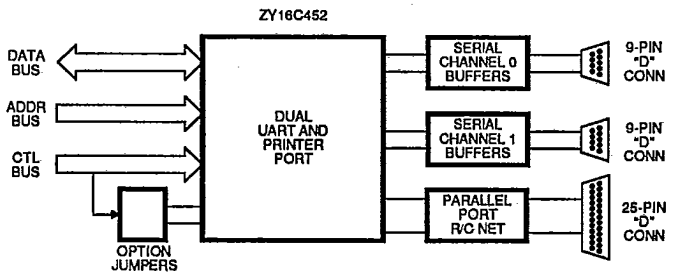
DECEMBER 1988

DESCRIPTION

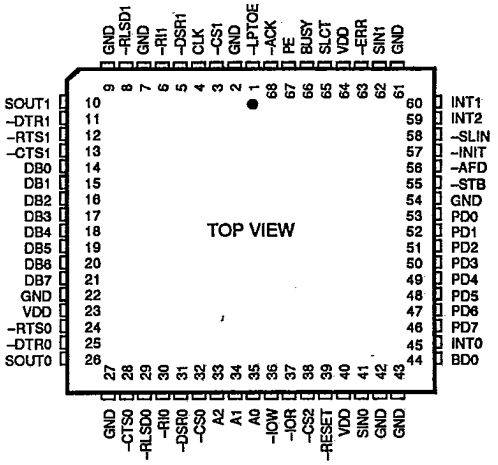
The ZyMOS Zy16C452 integrated circuit is an enhanced dual-channel version of the popular 16C450 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on characters transmitted by the CPU. The complete status of either channel can be read at any time by the CPU. The status information includes the type and condition of the transfer operations being performed, and error conditions. A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16}-1) and produce a X16 clock for driving the internal transmitter clock. Also included is complete modem control capability.

In addition to its dual communications interface capabilities, Zy16C452 provides the user with a bidirectional parallel data port that fully supports the parallel Centronics-type printer interface. The parallel port, together with the two serial ports, provide IBM PC AT-compatible computers with a single device to serve the three system ports.

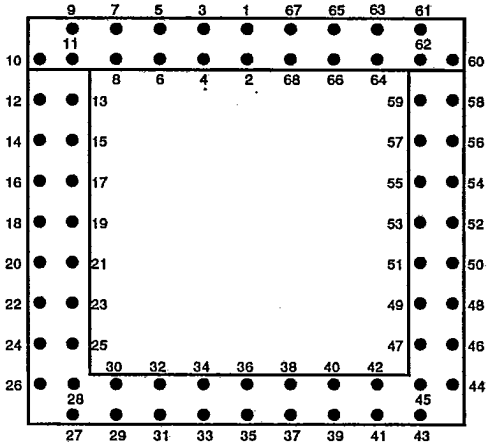
Zy16C452 complements and extends the ZyMOS POACH family of integrated circuits and chip-sets for the personal computer market. It provides a simple, cost-effective and flexible solution for implementing complex asynchronous communications products. It allows high-quality system solutions while supplying full IBM-register-level compatibility. Zy16C452 is housed in a 68-pin plastic leaded chip carrier (PLCC).



Zy16C452 Device Application



68-pin plastic flat package diagram



68-pin socket configuration diagram *(component side)*

Figure 1. Zy16C452 68-pin Plastic Flat Package Diagrams

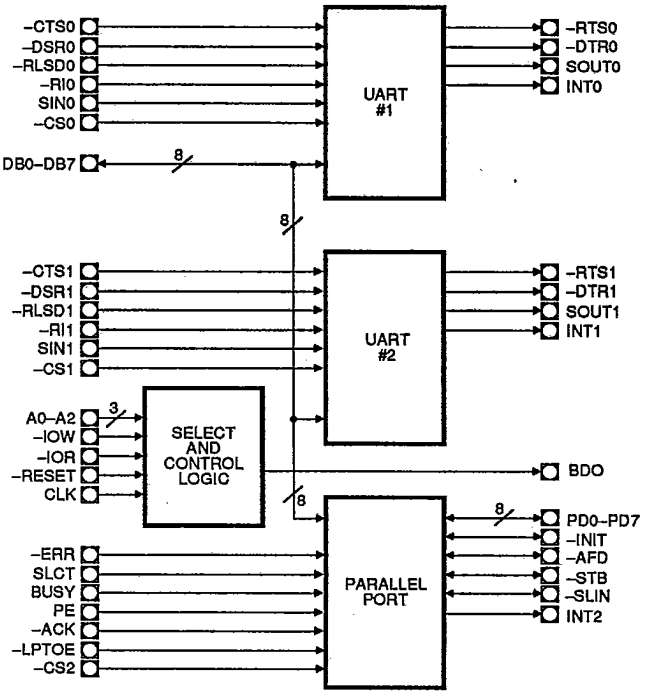


Figure 2. Zy16C452 Block Diagram

Zy16C452 Signal Summary

Signal Name	Pin Number	Signal Description
A0, A1, A2	35,34,33	**Address Lines A0-A2** - The address lines select the internal registers during CPU bus operations. See Table 2 for the decode of the serial channels, Table 12 for the decode of the parallel line printer port.
-ACK	68	**Line Printer Acknowledge** - This input goes low to indicate that a successful data transfer has taken place. A printer port interrupt is generated on a positive transition.
-AFD	56	**Line Printer Autofeed** - This open-drain output provides the line printer with an active-low signal when continuous form paper is to be autofed to the printer.
BDO	44	**Bus Buffer Output** - This active high output is asserted when either serial channel or the parallel port is read. This output can be used to control a system bus driver device (74LS245).
BUSY	66	**Line Printer Busy** - This signal is an input from the line printer that goes high when the line printer is not ready to accept data.
CLK	4	**Clock Input** - The external clock input to the baud rate divisor of each UART.
-CS0, -CS1, -CS2	32,3,38	**Chip Selects** - Each Chip Select input acts as an enable for the write and read signals for serial channels 0 (-CS0) and 1 (-CS1). -CS2 enables the signals to the line printer port.
-CTS0, -CTS1	28,13	**Clear to Send Input** - the logical state of each -CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is a bit 4 of the MSR, written MSR (4)] of each UART. A change of state on -CTS since a previous read of the MSR sets DCTS [MSR(0)]. When a -CTS pin is low, the modem is indicating that data on the associated SOUT can be transmitted.
DB0-DB7	14-21	**Data Bits DB0-DB7** - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between Zy16C452 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
DSR0, DSR1	31,5	**Data Set Ready Inputs** - The logical state of the DSR input is reflected in MSR (5) of the associated Modem Status Register. DDSR [MSR (1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR. When a DSR pin is low, its modem is indicating that it is ready to exchange data with the associated UART.
DTR0, DTR1	25,11	**Data Terminal Ready Lines** - Each DTR output can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of its associated UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR pin indicates that its UART is ready to receive data.

Zy16C452 Signal Summary *(cont.)*

Signal Name	Pin Number	Signal Description
-ERR	63	**Line Printer Error** - This signal is an input from the line printer. The line printer reports an error by holding this line low during the error condition.
GND	2,7,9,22 27,42,43, 54,61	**Ground (0 V)** - All pins must be tied to ground for proper operation.
-INIT	57	**Line Printer Initialize** - This open-drain I/O pin provides the line printer with a signal that allows the line printer initialization routine to be started.
INT0, INT1	45,60	**Serial Channel Interrupts** - Each three-state, serial channel interrupt output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service.
INT2	59	**Printer Port Interrupt** - This signal is an active high, three-state output, generated by the positive transition of -ACK. It is enabled by bit 4 of the Write Control Register.
-IOR	37	**Input/Output Read Strobe** - This is an active low input which causes the selected channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2 and chip selects -CS0, -CS1, -CS2.
-IOW	36	**Input/Output Write Strobe** - This is an active-low input which causes data from the data bus (DB0-DB7) to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2 and chip selects -CS0, -CS1, -CS2.
-LPTOE	1	**Parallel Data Output Enable** - When low this input enables the Write Data Register to the PD1-PD7 lines. A high puts the PD0-PD7 lines in the high-impedance state, allowing them to be used as inputs. -LPTOE is usually tied low for the printer operation.
PD0-PD7	54-46	**Parallel Data Bits (0-7)** - These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when -LPTOE is held in the high state.
PE	67	**Line Printer Paper Empty** - This is an input line from the line printer that goes high to indicate an out-of-paper condition.
-RI0, -RI1	30,6	**Ring Indicator Inputs** - When low, -RI indicates that a telephone ringing signal has been received by the modem or data set. The -RI signal is a modem control input whose condition is tested by reading MSR (6) (RI) of each UART. The Modem Status Register output TER1[MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3) = 1] and RI changes from a high to low, an interrupt is generated.

Zy16C452 Signal Summary *(cont.)*

Signal Name	Pin Number	Signal Description
-RESET	39	**Reset** - When low, the reset input forces Zy16C452 into an idle mode in which all data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
-RLSD0,-RLSD1	29,8	**Receive Line Signal Detect** - When low, the -RLSD output indicates that the data carrier has been detected by the modem or data set. -RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Registers. MSR (3) (DRLSD) of the Modem Status Register indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If -RLSD changes state with the modem status interrupt enabled, an interrupt occurs.
-RTS0, -RTS1	24,12	**Request to Send Outputs** - The -RTS signal is an output on each UART used to enable the modem, An -RTS pin is set low by writing a logic 1 to MCR (1) bit of its UART's Modem Control Register. Both -RTS pins are reset high by Reset. A low on the -RTS pin indicates the UART has data ready to transmit. In half-duplex operations, -RTS is used to control the direction of the line.
SIN0, SIN1	41,62	**Serial Data Inputs** - The serial data inputs move information from the communication line or modem to Zy16C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
SLCT	65	**Line Printer Selected** - This is an input line from the line printer that goes high when the line printer has been selected.
-SLIN	58	**Line Printer Select** - This open-drain line selects the printer when it is active low.
SOUT0, SOUT1	26,10	**Serial Data Outputs** - These lines are the serial data outputs from the UART's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
-STB	55	**Line Printer Strobe** - This open-drain line provides communication between POACH 71 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
V_{CC}	23,40 64	**Power Supply** - The power supply requirements is 5 V +/- 5%.

FUNCTIONAL DESCRIPTION

Zy16C452 combines three independent functional blocks into a single integrated circuit with common processor communication facilities. Each functional block has its own chip-select input to allow complete flexibility in address-map position assignments. For programming, a chip-select input must be active (low) to only the relevant block as summarized in Table 1. The -CSx inputs may be decoded only from addresses.

Table 1. Zy16C452 Functional Block Chip-select Inputs

-CS2	-CS1	-CS0	Block Enabled
1	1	0	UART #1
1	0	1	UART #2
0	1	1	parallel port

Note: All other input conditions are invalid.

Serial Channel Registers

Three types of internal registers for control, status, and data are used in each serial channel of Zy16C452. There are five control registers including the Bit Rate Select Registers DDL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control register. Two status registers are the Line Status Register and the Modem Status Register. The two data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, I/O Read, and I/O Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 2). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. For example, LCR(7) refers to Line Control Register Bit 7.

Table 2. Serial Channel Internal Register Addressing

-CSx*	DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	0	1	IER	Interrupt Enable Register
0	X	0	1	0	IIR	Interrupt Identification Register (read only)
0	X	0	1	1	LCR	Line Control Register
0	X	1	0	0	MCR	Modem Control Register
0	X	1	0	1	LSR	Line Status Register
0	X	1	1	0	MSR	Modem Status Register
0	X	1	1	1	SCR	Scratch Register
0	1	0	0	0	DLL	Divisor Latch (LSB)
0	1	0	0	1	DLM	Divisor Latch (MSB)

X = Don't Care 0 = Logic Low 1 = Logic High

***Note:** Serial Channel 0 is accessed when -CS0 is low; Serial Channel 1 is accessed when -CS1 is low. Selecting both channels simultaneously is an invalid condition, see Table 1.

Table 3. Serial Channel Registers

Register Mnemonic	Register Bit Number							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit0**
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" *if* Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	(INT) Interrupt Enable	unused	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(RLSD) Receive Line Signal Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRLSD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

The Transmitter Holding Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. Zy16C452 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

Line Control Register

The format of the data character is controlled by the Line Control Register (LCR). The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. Figure 3 shows the contents of the LCR.

The contents of the LCR are described below:

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR (1), Word Length Select Bits:
The word length of each serial character is programmed as shown in the following chart:

LCR (1)	LCR (0)	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

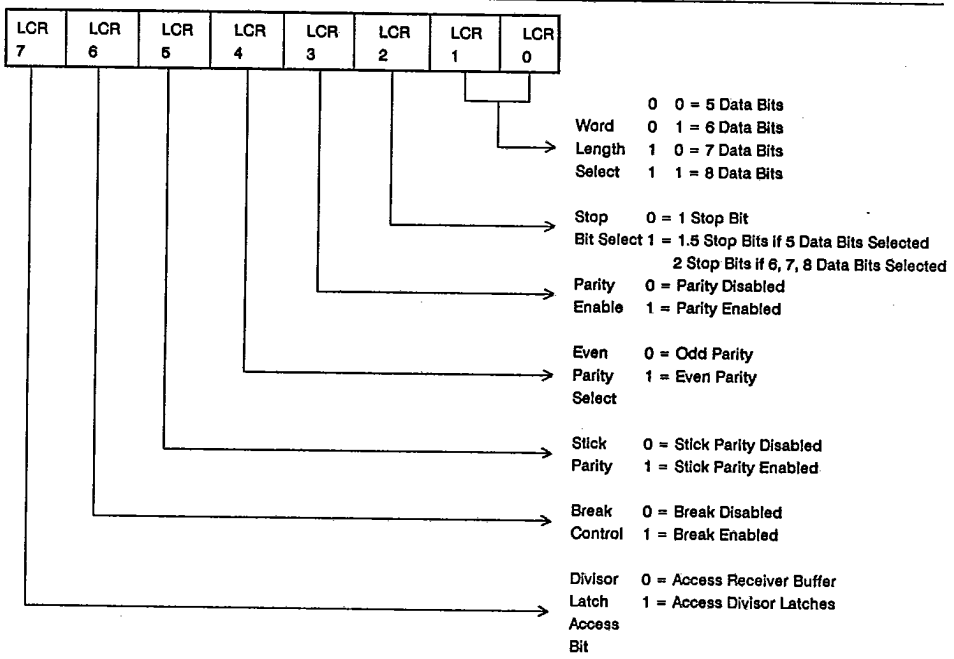


Figure 3. Line Control Register

LCR (2) Stop Bit Select: LCR (2) specifies the number of stop bits in each transmitted character. If LCR (2) is a logic 0, one stop bit is generated in the transmitted data. If LCR (2) is a logic 1 when a five-bit word length is selected, one-and-one-half stop bits are generated. If LCR (2) is a logic 1 when either a six-, seven-, or eight-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR (3) Parity Enable: When LCR (3) is high, a parity bit between the last data word bit and the stop bit is generated and checked.

LCR (4) Even Parity Select: When parity is enabled [LCR (3) = 1], LCR (4) = 0 selects odd parity, and LCR (4) = 1 selects even parity.

LCR (5) Stick Parity: When parity is enabled [LCR (3) = 1], LCR (5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR (4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR (6) Break Control: When LCR (6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR (6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"'s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1), and clear break when normal transmission has to be restored.

LCR (7) Divisor Latch Access Bit (DLAB): LCR (7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR (7) must be low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

Line Status Register

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of Zy16C452.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error character, LSR(1), indicates that the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. LSR(3), the Framing Error (FE), indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE), LSR(2), indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

Table 4. Line Status Register Bits

LSR BITS	LOGIC 1	LOGIC 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used	-	-

The Break Interrupt (BI) status bit, LSR(4), indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

Reading the LSR clears LSR (1)-LSR (4) -- (OE, PE, FE, and BI).

LSR (1) - LSR (4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER (2)=1 in the Interrupt Enable Register.

The LSR(5) Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit, LSR(6), indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER (1)], and active THRE causes an interrupt.

The Data Ready (DR) bit, LSR(0), indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

The contents of the Line Status Register shown in Table 4 are summarized below:

LSR (0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR (0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR (1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR (2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR(4)]. The PE bit is set high upon detection of parity error, and is reset low when the CPU reads the contents of the LSR.

LSR (3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR (3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low

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Table 5. Modem Control Register Bits

MCR BITS	Logic 1	Logic 0
MCR (0) Data Terminal Ready (DTR)	-DTR Output Low	-DTR Output High
MCR (1) Request To Send (RTS)	-RTS Output Low	-RTS Output High
MCR (2) unused	-	-
MCR (3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4) LOOP	Loop Enabled	Loop Disabled
MCR (5) always 0	-	-
MCR (6) always 0	-	-
MCR (7) always 0	-	-

when the CPU reads the contents of the LSR.

LSR (4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full-word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR (5) Transmitter Holding Register Empty (THRE): THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR (5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR (5) is not reset by the CPU read of the LSR.

When the THRE interrupt is enabled (IER (1) = 1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTx is cleared by a read of the IIR.

LSR (6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR (7): This bit is always 0.

Modem Control Register

The Modem Control Register (MCR) controls the interface with the modem or data set as summarized in Table 5. Figure 4 illustrates the MCR. The MCR can be written and read. The -RTS and -DTR outputs are directly controlled by the bits MCR(1) and MCR(0) in this register. A logic high data input asserts a low (true) level at the output pins. MCR Bits bit functions are described below.

In the diagnostic mode, data transmitted is immediately received, thus allowing the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) through MCR(7) are permanently set to logic 0.

MCR (0): When MCR (0), Data Terminal Ready is set high, the -DTR output is forced low. When MCR (0) is programmed low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain

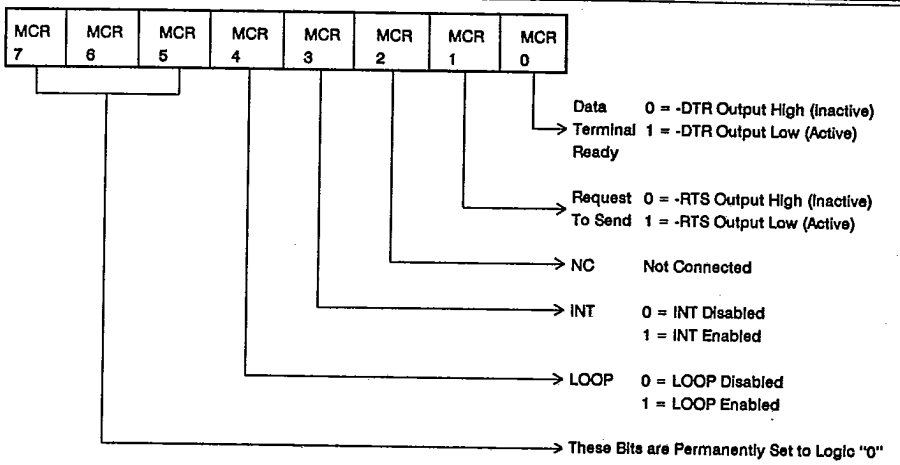


Figure 4. Modem Control Register

the proper polarity input at the modem or data set.

MCR (1): When MCR(1) Request To Send is set high, the RTS output is forced low. When MCR(1) is programmed low, the -RTS output is forced high. The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(2): MCR(2) is an unused register bit. Whatever data is written into this bit can be read back. MCR(2) is set low from an active reset- or a loop-mode operation.

MCR(3): When MCR(3) is set high, the INT output is enabled. MCR(3) is set low from an active -RESET or a loop mode operation.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR (4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (-CTS, -DSR, and -RI) are disconnected. The modem control output pins are forced to their inactive state (high).

Modem Status Register

The Modem Status Register (MSR) provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read each of the serial channel modem signal inputs by accessing the data bus interface of Zy16C452. In addition to the current status information, four bits indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are -CTS, -DSR, -RI, and -RLSD. MSR(4) - MSR(7) are status indications of these lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are summarized in Table 6. Note that the state (0 or 1) of the status bits MSR(4) to MSR(7) are inverted versions of the actual input signal level.

Table 6. Modem Status Register Bits

MSR Bit	Mnemonic	Description
MSR (0)	DCTS	Delta Clear to Send
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (3)	DRLSD	Delta Receive Line Signal Detect
MSR (4)	-CTS	Clear to Send
MSR (5)	-DSR	Data Set Ready
MSR (6)	-RI	Ring Indicator
MSR (7)	-RLSD	Receiver Line Signal Detect

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the -CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low-to-high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the -RSLD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MCR(4) = 1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSD): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4) = 1], MSR(5) is equivalent to the DTR in the MCR.

MSR(6) Ring Indicator: Indicates the status of the -RI input. If the channel is in the loop mode [MCR(4) = 1], MSR(6) is set low (inactive).

MSR (7) Receive Line Signal Detect: Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (-RLSD) input. If the channel is in the loop mode [MCR(4) = 1], MSR(4) is set low (inactive).

The modem status inputs (-RI, -RLSD, -DSR, and -CTS) reflect the current modem input signal level. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read

Table 7. RBR Bit Definition

	Character Length			
	5-bit	**6-bit**	**7-bit**	**8-bit**
RBR(0)	Data Bit 0	Data Bit 0	Data Bit 0	Data Bit 0
RBR(1)	Data Bit 1	Data Bit 1	Data Bit 1	Data Bit 1
RBR(2)	Data Bit 2	Data Bit 2	Data Bit 2	Data Bit 2
RBR(3)	Data Bit 3	Data Bit 3	Data Bit 3	Data Bit 3
RBR(4)	Data Bit 4	Data Bit 4	Data Bit 4	Data Bit 4
RBR(5)	0	Data Bit 5	Data Bit 5	Data Bit 5
RBR(6)	0	0	Data Bit 6	Data Bit 6
RBR(7)	0	0	0	Data Bit 7

Table 8. THR Bit Definition

	Character Length			
	5-bit	**6-bit**	**7-bit**	**8-bit**
THR(0)	Data Bit 0	Data Bit 0	Data Bit 0	Data Bit 0
THR(1)	Data Bit 1	Data Bit 1	Data Bit 1	Data Bit 1
THR(2)	Data Bit 2	Data Bit 2	Data Bit 2	Data Bit 2
THR(3)	Data Bit 3	Data Bit 3	Data Bit 3	Data Bit 3
THR(4)	Data Bit 4	Data Bit 4	Data Bit 4	Data Bit 4
THR(5)	X	Data Bit 5	Data Bit 5	Data Bit 5
THR(6)	X	X	Data Bit 6	Data Bit 6
THR(7)	X	X	X	Data Bit 7

X = Don't care

operation (-IOR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read (-IOR) operations. If a status condition is generated during a read (-IOR) operation, the status bit is not set until the trailing edge of the read -IOR.

If a status bit is set during a read -IOR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read -IOR instead of being set again.

Receiver Buffer Register

The receiver circuitry in each serial channel of Zy16C452 is programmable for five, six, seven, or eight data bits per character. For words of less than eight bits, the data is right justified to the least significant bit, LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than eight bits are output low to the parallel output by the serial channel as shown in Table 7.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the internal 16X clock. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is

shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register and the DR flag in the LSR register is set [LSR(0)].

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in overflow data in the Receiver Register. The OE flag in the LSR register, [LSR(1)], indicates the overrun condition.

Transmitter Holding Register

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. Characters are right justified and if the character is less than eight bits, unused bits of the microprocessor data bus are ignored by the transmitter as shown in Table 8.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflects the status of the THR. The TEMT flag [LSR(6)] indicates that both the THR and TSR are empty.

Scratchpad Register

The Scratchpad Register is a general-purpose, undedicated, eight-bit Read/Write register that has no effect on any communication channel in Zy16C452. It is intended to be used by the programmer to hold data temporarily.

SCR Register Map

SCR(0) Data Bit 0
SCR(1) Data Bit 1
SCR(2) Data Bit 2
SCR(3) Data Bit 3
SCR(4) Data Bit 4
SCR(5) Data Bit 5
SCR(6) Data Bit 6
SCR(7) Data Bit 7

Interrupts

The Interrupt Identification Register (IIR) of each serial channel of Zy16C452 has interrupt capability for interfacing to standard microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Interrupt Identification Register

Information indicating that a prioritized interrupt is pending together with the type of interrupt is stored in the Interrupt Identification Register (IIR). During a CPU read operation, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 5. The IIR is a read-only register whose contents are indicated in Table 9 and described below.

IIR(0): IIR(0) can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending

Table 9. Interrupt Identification Register

Interrupt Identification				Interrupt Set and Reset Function		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Flag**	**Interrupt Source**	**Interrupt Reset Control**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt source or a THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR -RI, -RLSD	MSR Read

X = Don't care.

and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 9.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

Interrupt Enable Register

The Interrupt Enable Register (IER) is used to independently enable the four serial channel interrupts which activate the interrupt (INT) output. All interrupts are disabled by programming IER(0) - IER(3) of the Interrupt Enable Register to 0. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register

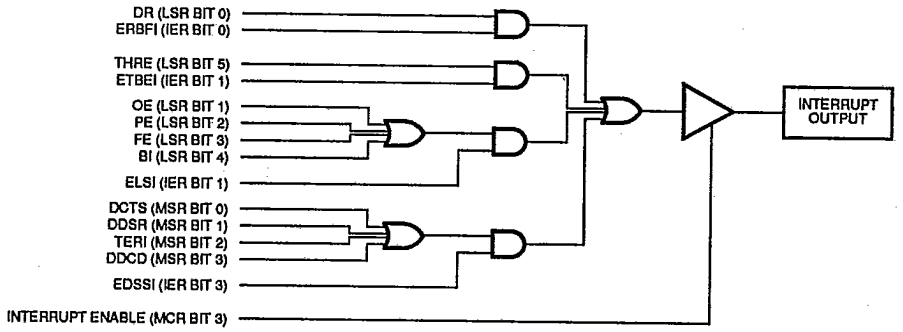


Figure 5. Zy16C452 Interrupt Control Logic

and the active -high INT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are summarized below:

IER(0): When programmed high [IER(0) = 1], IER(0) enables the Received Data Available interrupt.

IER(1): When programmed high [IER(1) = 1], IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high [IER(2) = 1], IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high [IER(3) = 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register that indicate the status of THR and TSR. To transmit a five-to eight-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The first word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR-to-TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in the LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry

which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within +/- 3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator

Each serial channel of Zy16C452 contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1}. The BRG produces clocking for the UART function, providing standard ANSI/CCIT bit rates. The oscillator driving the BRG is provided by an external clock source input to the CLK pin.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 10, 11, and 12 illustrate the divisors needed to obtain standard rates using these three crystal frequencies. The output frequency of the Baud Generator is 16X the data rate [divisor # = clock + (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

Reset

After power-up, the Zy16C452 -RESET input should be held low for 500 ns to reset internal circuits to an idle mode until initialization. A low on -RESET causes the following:

1. Initilializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (Reset high), Zy16C452 remains in the idle mode until programmed.

A hardware reset sets the THRE and TEMT status bits in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.
A summary of the effect of a reset on Zy16C452 is given in Table 13.

Programming

Each serial channel of Zy16C452 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control

words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the serial channel is not transmitting or receiving data.

Software Reset

A software reset of the serial channel is a useful method for returning to a complete known state without a system reset. A software reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Table 10. Baud Rates (1.8432-MHz Clock)

Desired Baud Rate	Divisor Used	Divisor Latch Programming (Hex)		Percent Error Difference Between Desired and Actual
		DLM	DLL	
50	2304	09	00	-
75	1536	06	00	-
110	1047	04	17	0.026
134.5	857	03	59	0.058
150	768	03	00	-
300	384	01	80	-
600	192	00	C0	-
1200	96	00	60	-
1800	64	00	40	-
2000	58	00	3A	0.69
2400	48	00	30	-
3600	32	00	20	-
4800	24	00	18	-
7200	16	00	10	-
9600	12	00	0C	-
19200	6	00	06	-
38400	3	00	03	-
56000	2	00	02	2.86

Table 11. Baud Rates (2.4576-MHz Clock)

Desired Baud Rate	Divisor Used	Divisor Latch Programming (Hex)		Percent Error Difference Between Desired and Actual
		DLM	DLL	
50	3072	0C	00	-
75	2048	08	00	-
110	1396	05	74	0.026
134.5	1142	04	76	0.0007
150	1024	04	00	-
300	512	02	00	-
600	256	01	00	-
1200	128	00	80	-
1800	85	00	55	0.392
2000	77	00	4D	0.260
2400	64	00	40	-
3600	43	00	2B	0.775
4800	32	00	20	-
7200	21	00	15	1.587
9600	16	00	10	-
19200	8	00	08	-
38400	4	00	04	-

Table 12. Baud Rates (3.072-MHz Clock)

Desired Baud Rate	Divisor Used	Divisor Latch Programming (Hex)		Percent Error Difference Between Desired and Actual
		DLM	DLL	
50	3840	0F	00	-
75	2560	0A	00	-
110	1745	06	D1	0.026
134.5	1428	05	94	0.034
150	1280	05	00	-
300	640	02	80	-
600	320	01	40	-
1200	160	00	A0	-
1800	107	00	6B	0.312
2000	96	00	60	-
2400	80	00	50	-
3600	53	00	35	0.628
4800	40	00	28	-
7200	27	00	1B	1.23
9600	20	00	14	-
19200	10	00	0A	-
38400	5	00	05	-

Table 13. Reset Summary

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Reset	All Bits Low
MODEM Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low; Except Bits 5 and 6 are High
MODEM Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
-Out2	Reset	High
-RTS	Reset	High
-DTR	Reset	High
-Out1	Reset	High

Parallel Port Registers

The parallel port of Zy16C452 provides a Centronics-style printer interface. When Chip Select 2 (-CS2) is low, the parallel port is selected. Table 14 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (-IOR) and write (-IOW) pins as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer. The status bits are Printer Busy (-BUSY), Acknowledge (-ACK), which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (-ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

The write control bits are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer (-INIT), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Table 14. Parallel Port Registers

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	-BUSY	-ACK	PE	SLCT	-ERR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE

Table 15. Parallel Port Register Select

Control Pins					Register Selected
-IOR	-IOW	-CS2	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

Note: All other combinations are invalid.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to 150°C
Voltage on any pin with respect to ground	-0.5V to V_{DD} + 0.5V
Maximum V_{DD} voltage with respect to ground	6.0V
Power Dissipation	1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Zy16C452 DC Characterisitics (V_{DD} = 5V +/- 5%, T_A = 0 to 70°C)

Symbol	Parameter	Conditions	Value MIN	TYP	MAX	Units	Notes
V_{IL}	Input Low Voltage		-0.5		0.8	V	1
V_{IH}	Input High Voltage		2.0		V_{CC}	V	1
I_{IL}	Input Current	V_{IN} = 0 to 5.2V	-10		+10	uA	2
I_{OL1}	Output Current, low	V_{OL} = 0.4 V	4.0			mA	3
I_{OL2}	Output Current, low	V_{OL} = 0.4 V	10			mA	4
I_{OL3}	Output Current, low	V_{OL} = 0.4 V	16			mA	5
I_{OCL}	Open Collector Output Current, low	V_{OL} = 0.4 V	10			mA	6
I_{OH}	Output Current, high	V_{OH}= 2.4 V			-4	mA	7
I_{OCH}	Open Collector Output Current, high	V_{OH}= 2.4 V			-0.2	mA	6
I_{OZ}	3-state Output Leakage	V_{OUT} = 0 to 5.25 V 1) Chip deselected 2) Chip and write mode selected	-20		+20	uA	
I_{DD}	Power Supply Current	Outputs unloaded CLK = 4 MHz. Baud rate = 56K			50	mA	8

Notes:

1. Note that the -RESET input is a Schmitt circuit providing hysteresis.
2. Tested with all pins other than V_{DD} and V_{SS} floating.
3. For the data bus outputs DB0 to DB7 and all the UART outputs -RTS0, -DTR0, SOUT0, INT0, -RTS1, -DTR1, SOUT1, INT1, and also BD0.
4. For the -INT2 output.
5. For the parallel port outputs PD0 to PD7.
6. For the open collector I/O signal outputs of -INIT, -AFD, -STB and -SLIN.
   These pins have an internal pull-up resistor of 2.5K-ohm to 3.5K-ohm value connected to V_{DD}, which will generate a maximum of 2.0 mA internal current (I_{OL}) when the output is active (low). Each output will sink 10 mA (at 0.4V) to meet the I_{OCL} specification in addition to this internal current.
7. For all outputs except -INIT, -AFD, -STB and -SLIN.
8. Tested with SIN0, SIN1, -DSR0, -DSR1, -RLSD0, -RLSD1, -CTS0, -CTS1, -RI0, -RI1 all at a high (2.0V) logic level.

Zy16C452 AC Characterisitics

SYMBOL	PARAMETER	Value MIN	TYP	MAX	UNITS	NOTES
Processor Interface						
1	A0-A2 setup time to -IOR active	60			ns	
2	A0-A2 hold time from -IOR inactive	20			ns	
3	A0-A2 setup time to -IOW active	60			ns	
4	A0-A2 hold time from -IOW inactive	20			ns	
	BD0 delay from -IOR			100	ns	
5	CS0-CS2 setup time to -IOR active	60			ns	
6	CS0-CS2 hold time from -IOR inactive	20			ns	
7	CS0-CS2 setup time to -IOW active	50			ns	
8	CS0-CS2 hold time from -IOW inactive	20			ns	
9	DB0-DB7 delay time from -IOR active			125	ns	
10	DB0-DB7 disable delay from -IOR inactive	0		100	ns	
11	DB0-DB7 setup time to -IOW active	40			ns	
12	DB0-DB7 hold time from -IOW inactive	40			ns	
13	-IOR pulse width	125			ns	
14	-IOR cycle time	360			ns	
15	-IOW pulse width	100			ns	
16	-IOW cycle time	360			ns	
	-RESET pulse width	5			us	
UART Operation						
	CLK high pulse width	140			ns	
	CLK low pulse width	140			ns	
	CLK input frequency			3.1	MHz	
25	-DTR0 (-DTR1) delay from -IOW inactive (Wr. MCR)			250	ns	
26	INT0 (INT1) active delay from -CTS0 (-CTS1) inactive			250	ns	
	INT0 (INT1) active delay from -DSR0 (-DSR1) inactive			250	ns	
26	INT0 (INT1) active delay from -RLSD0 (-RLSD1) inactive			250	ns	
27	INT0 (INT1) active delay from -RI0 (-RI1) inactive			250	ns	
28	INT0, INT1 inactive delay from -IOR inactive (Rd. RBR, LSR)			1	us	
29	INT0, INT1 inactive delay from -IOR inactive (Rd. IIR, MSR)			250	ns	
30	INT0, INT1 active delay from -IOW inactive (Wr. THR)	8		24	CLK cycles	
31	INT0, INT1 inactive delay from -IOR active (Wr. THR)			175	ns	
32	INT0 (INT1) active delay from SIN0 (SIN1) stop bit			1	CLK cycle	
33	INT0 (INT1) active delay from SOUT0 (SOUT1) stop bit			8	CLK cycles	
25	-RTS0 (-RTS1) delay from -IOW inactive (Wr. MCR)			250	ns	
34	SOUT0 (SOUT1) delay (transmit start) from INT0 (INT1) inactive			16	CLK cycles	

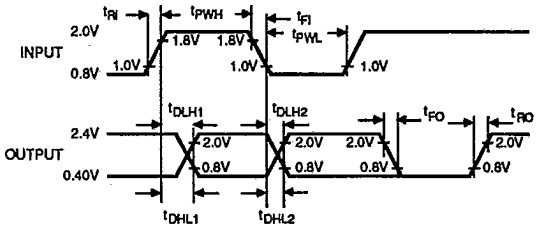
ZyC16452 AC Characterisitics *(cont.)*

SYMBOL PARAMETER	Value MIN	TYP	MAX	UNITS	NOTES
Parallel Port Operation					
-AFD active delay from -IOW inactive			100	ns	
-AFD inactive delay from -IOW inactive			400	ns	4
-AFD inactive delay from -RESET active			400	ns	4
DB0 delay from -STB			100	ns	3
DB1 delay from -AFD			100	ns	3
DB2 delay from -INIT			100	ns	3
DB3 delay from -ERR			100	ns	3
DB3 delay from -SLIN			100	ns	3
DB4 delay from SLCT			100	ns	3
DB5 delay from PE			100	ns	3
DB6 delay from -ACK			100	ns	3
DB7 delay from BUSY			100	ns	3
DB0-DB7 delay from PD0-PD7			100	ns	3
-INIT active delay from -IOW inactive			100	ns	
-INIT inactive delay from -IOW inactive			400	ns	4
-INIT active delay from -RESET active			400	ns	4
-INT2 delay from -ACK			100	ns	
PD0-PD7 delay from -IOW inactive			100	ns	
PD0-PD7 enable/disable delay from -LPTOE			100	ns	1
-SLIN inactive delay from -IOW inactive			400	ns	4
-SLIN active delay from -IOW inactive			100	ns	
-SLIN inactive delay from -RESET active			400	ns	4
-STB active delay from -IOW inactive			100	ns	
-STB inactive delay from -IOW inactive			400	ns	4
-STB inactive delay from -RESET active			400	ns	4

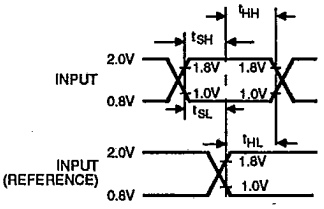
Notes:

1. The output float or high impedance condition occurs when the output current is less than I_{OZ} in magnitude.
2. Input rise and fall times are assumed to be less than 20 ns unless otherwise specified.
3. Tested with -IOR active.
4. The output rise time is set by the internal pullup resistance value. External pullup resistors may be optionally added to the system in order to decrease the rise time.

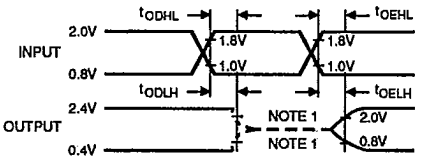
Zy16C452 Timing Waveforms



Delay Time and Pulse Width Measurements



Setup/Hold Time Measurements



Output Enable/Disable Measurements

Diagram 1. Zy16C452 AC Measurement Points

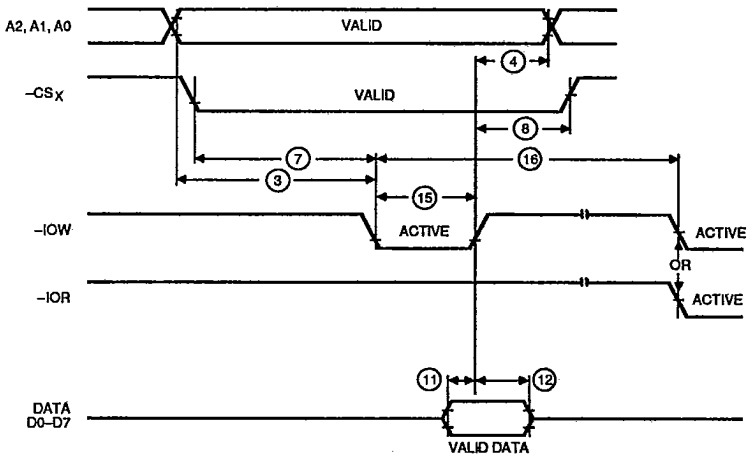


Diagram 2. I/O Write Cycle Timing

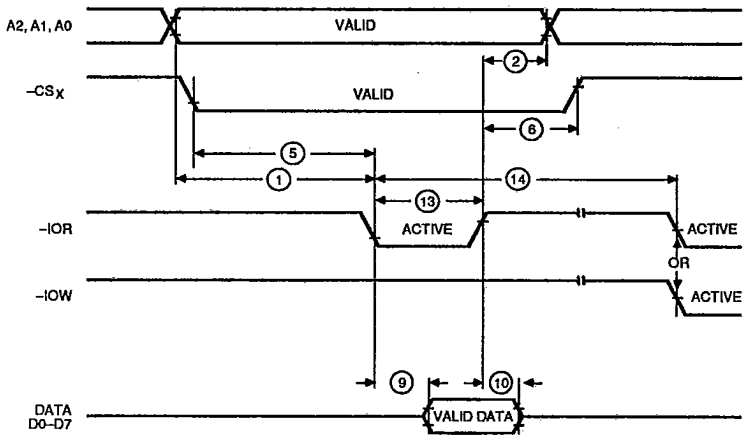


Diagram 3. I/O Read Cycle Timing

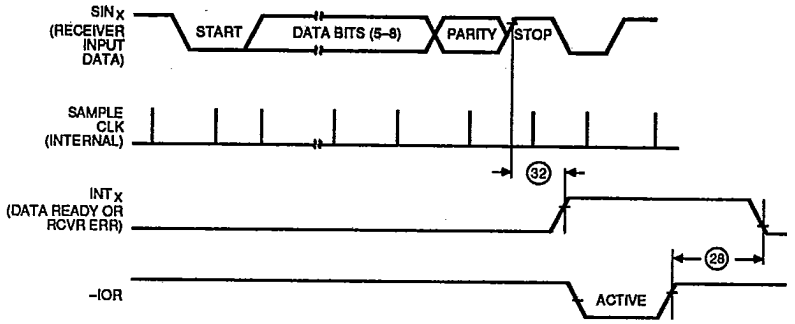


Diagram 4. UART Receiver Operation

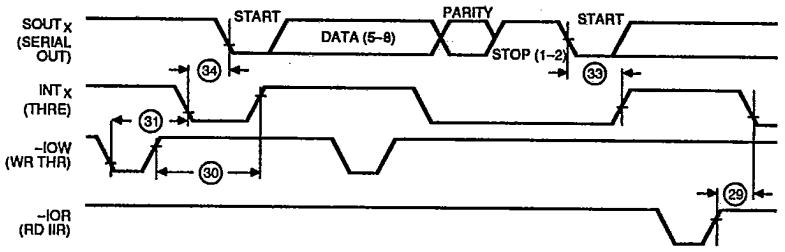


Diagram 5. UART Transmitter Operation

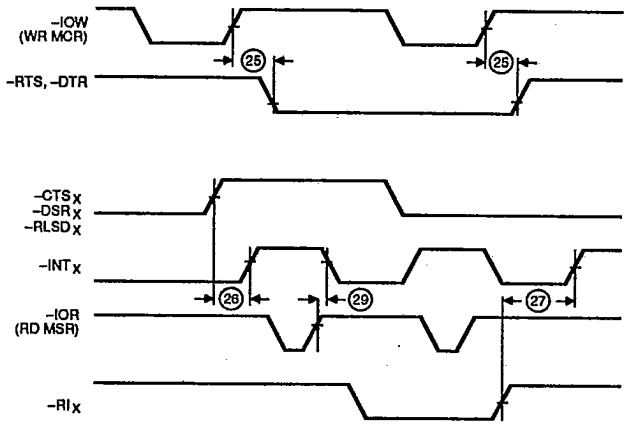


Diagram 6. Modem Operation

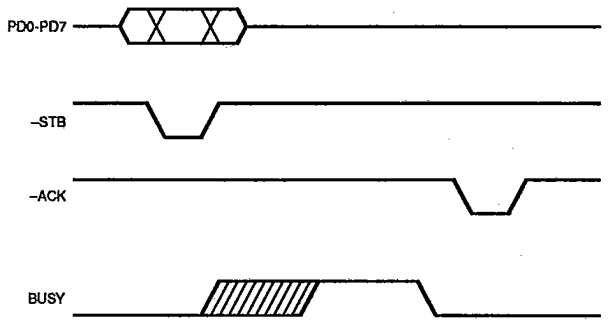
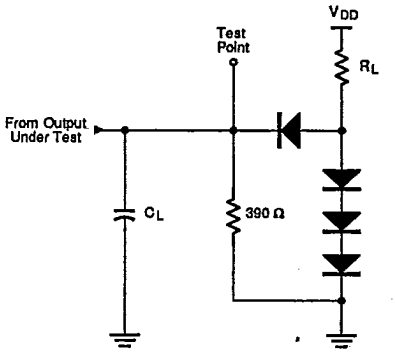


Diagram 7. Parallel Port Operation

Output Test Load Network

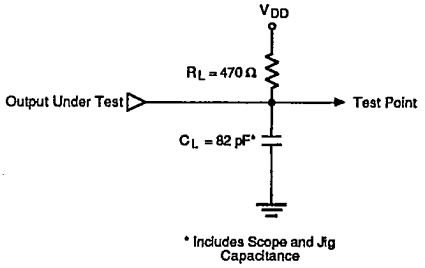
Standard Outputs



Notes:

C_L = 100 pF for all outputs
R_L = 620 ohms for I_{OL1} specification outputs
R_L = 300 ohms for the -INT2 output
R_L = 220 ohms for the PD0-PD7 outputs

Open Collector Outputs

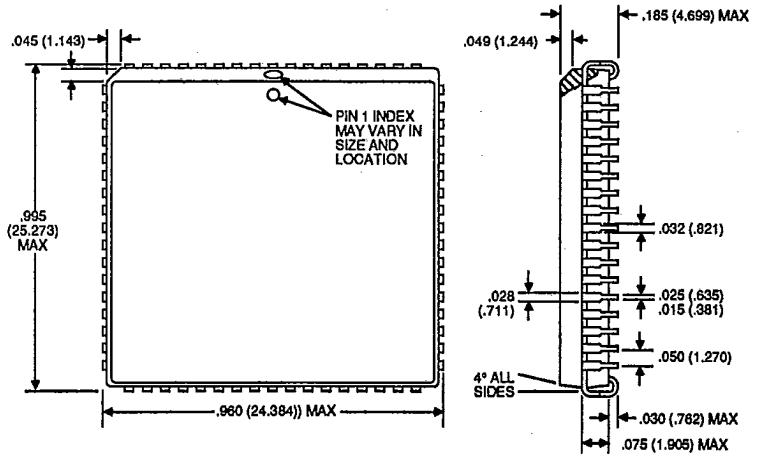


Note:

For the -INIT, -AFD, -STB and -SLIN outputs

T-75-37-05

68-pin PLCC Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED
1 TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESESES.

68-pin PLCC Package Marking Details