

UT54ACS373/UT54ACTS373

Radiation-Hardened Octal Transparent Latches with Three-State Outputs

FEATURES

- 8 latches in a single package
- Three-state bus-driving true outputs
- Full parallel access for loading
- 1.2 μ radiation-hardened CMOS
 - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
 - 20-pin DIP
 - 20-lead flatpack

DESCRIPTION

The UT54ACS373 and the UT54ACTS373 are 8-bit latches with three-state outputs designed for driving highly capacitive or relatively low-impedance loads. The device is suitable for buffer registers, I/O ports, and bidirectional bus drivers.

The eight latches are transparent D latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

An output-control input (\overline{OC}) places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The high-impedance third state and increased drive provide the capability to drive the bus line in a bus-organized system without need for interface or pull-up components.

The output control \overline{OC} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

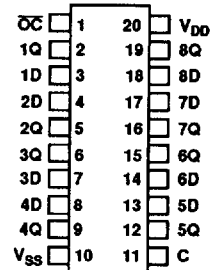
INPUTS			OUTPUT
\overline{OC}	C	nD	nQ
L	H	H	H
L	H	L	L
L	L	X	nQ ₀
H	X	X	Z ¹

Note:

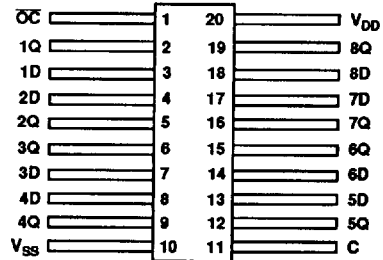
1. Data may be latched internally.

PINOUTS

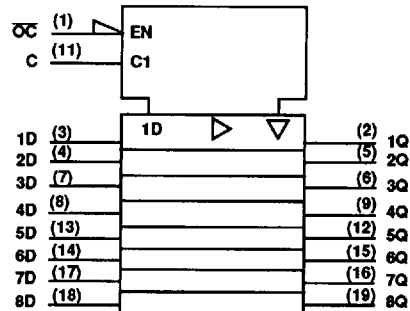
20-Pin DIP
Top View



20-Lead Flatpack
Top View



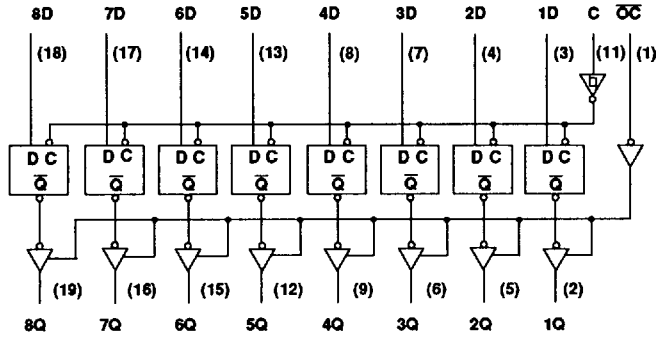
LOGIC SYMBOL



Note:

1. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold ²	80	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

- Logic will not latchup during radiation exposure within the limits defined in the table.
- Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS ⁷(V_{DD} = 5.0V ±10%; V_{SS} = 0V ⁶, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low-level input voltage ¹ ACTS ACS			0.8 3V _{DD}	V
V _{IH}	High-level input voltage ¹ ACTS ACS		.5V _{DD} .7V _{DD}		V
I _{IN}	Input leakage current ACTS/ACS	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
V _{OL}	Low-level output voltage ³ ACTS ACS	I _{OL} = 8.0mA I _{OL} = 100μA		0.40 0.25	V
V _{OH}	High-level output voltage ³ ACTS ACS	I _{OH} = -8.0mA I _{OH} = -100μA	.7V _{DD} V _{DD} - 0.25		V
I _{OZ}	Three-state output leakage current	V _O = V _{DD} and V _{SS}	-20	20	μA
I _{OS}	Short-circuit output current ^{2,4} ACTS/ACS	V _O = V _{DD} and V _{SS}	-200	200	mA
P _{total}	Power dissipation ^{8,9}	C _L = 50pF		1.9	mW/ MHz
I _{DDQ}	Quiescent Supply Current	V _{DD} = 5.5V		10	μA
C _{IN}	Input capacitance ⁵	f = 1MHz @ 0V		15	pF
C _{OUT}	Output capacitance ⁵	f = 1MHz @ 0V		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density ≤ 5.0E5 amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose ≤ 1E6 rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

AC ELECTRICAL CHARACTERISTICS ²(V_{DD} = 5.0V ±10%; V_{SS} = 0V ¹, -55°C < T_C < +125°C)

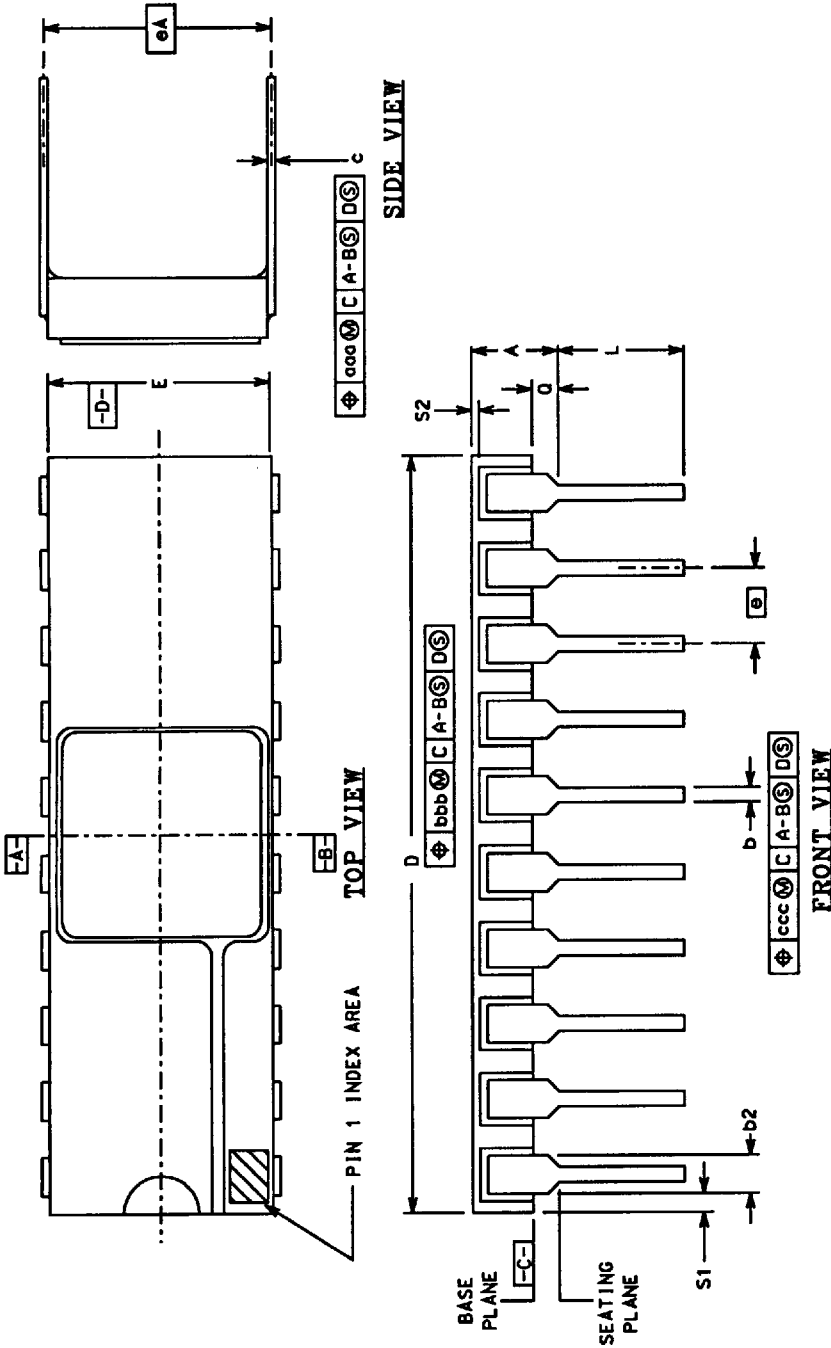
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PLH}	Data to Qn	1	14	ns
t _{PHL}	Data to Qn	1	16	ns
t _{PLH}	C or CLK to Qn	1	16	ns
t _{PHL}	C or CLK to Qn	1	18	ns
t _{PZL}	\overline{OC} low to Qn	1	14	ns
t _{PZH}	\overline{OC} low to Qn	1	14	ns
t _{PLZ}	\overline{OC} high to Qn three-state	1	14	ns
t _{PHZ}	\overline{OC} high to Qn three-state	1	14	ns
f _{MAX}	Maximum clock frequency		71	MHz
t _{SU}	Data setup time before C ↓	5		ns
t _H	Data hold time after C ↓	2		ns
t _w	Minimum pulse width C high	7		ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).

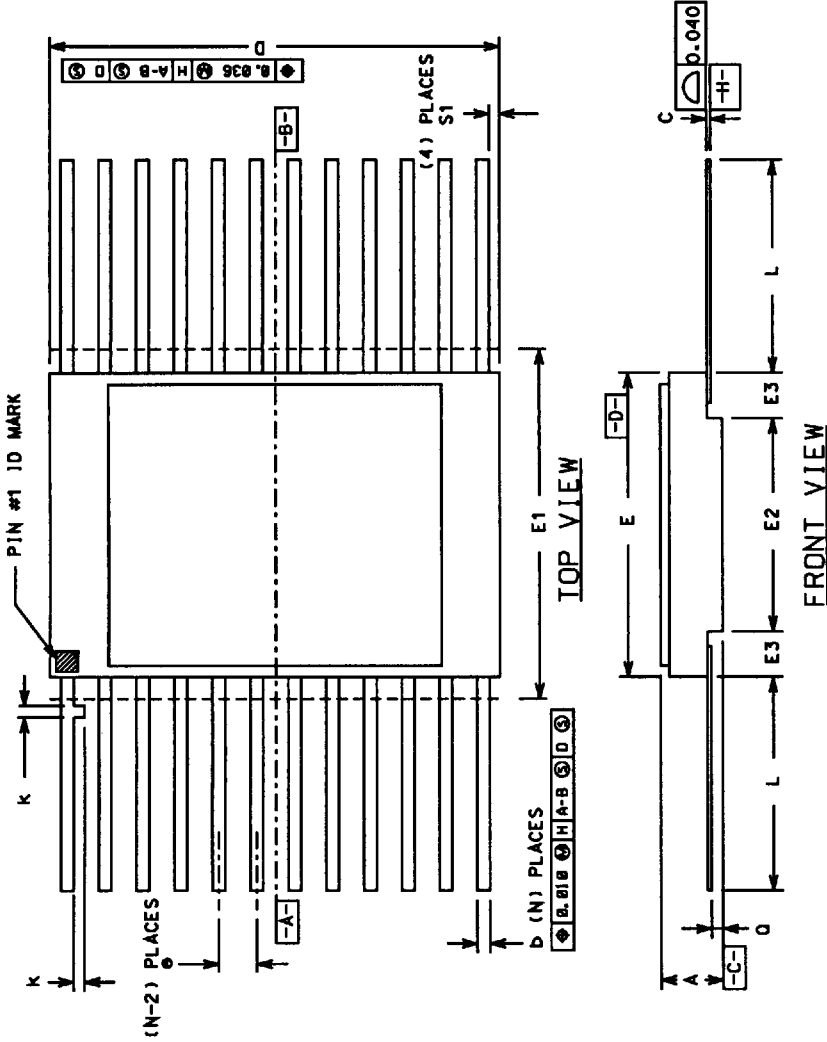
2.0 RAD-HARD MSI PACKAGES

Side-Brazed Packages



PKG CONFIG	MIL-STD- 1835 Dwg CONF C	DIMENSION SYMBOLS														
		A	b	b2	c	D	E	e	eA	L	Q	S1	S2	ddd	bbb	ccc
-01	14 D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-02	16 D-2	0.200	0.014	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-03	20 D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.015	0.030	0.010

Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS											
			A	b	c	D	E	E1	E2	E3	e	k	L	O
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 0.290	0.260 0.235	0.290 0.130	0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 0.245	0.285 0.245	0.315	0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 0.245	0.300 0.245	0.330	0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	0.000