Description

The μPD7730/77C30 is a large scale integration (LSI) single-chip digital signal processor, which compresses and decompresses digitized speech signals. It is a speech encoder/decoder that converts pulse code modulated audio to and from adaptive differential pulse code modulation (ADPCM). The μPD7730/77C30 encodes pulse coded modulation (PCM) data into ADPCM data, and decodes ADPCM data into PCM data. The μPD7730/77C30 is ideal for office automation applications, such as voice store and forward systems, and for various telecommunication applications. It reduces voice transmission bandwidth and voice storage requirements by half (from 64 kb/s to 32 kb/s). Its robust ADPCM algorithm makes it well qualified for transmission applications and the fact that it compresses speech by half makes it suitable for store and forward applications.

The μPD7730 and μPD77C30 are functionally identical, but the power requirement for the CMOS μPD77C30 is lower than that of the NMOS μPD7730. Both devices are housed in plastic DIP; the temperature range of the low power NMOS device is −10 to +70°C and the CMOS device is −40 to +85°C.

The maximum clock (CLK) frequency for the μPD7730/77C30 is 8.33 MHz, which corresponds to a CLK cycle time of 120 ns.

The μPD7730/77C30 accepts PCM data through its serial interface. The serial interface can be connected directly to a single-chip coder/decoder (CODEC) for digital μ-law PCM input/output or to a general purpose A/D or D/A converter for linear PCM code. This programmable serial interface supports both 8-bit logarithmic (μ-law) and 16-bit linear formats. The μPD7730/77C30 interfaces to the host CPU through a standard microprocessor bus interface.

If a clock frequency of 8.33 MHz is used to encode PCM data, then the μPD7730/77C30 requires 116 μs to process each sample, thus limiting the sampling frequency to 8.59 kHz. This implies that if the sample frequency is 8.0 kHz and the CLK is 8.33 MHz, then the internal algorithm will take approximately 93% of the time between samples. Serial data being shifted in or out has the full time between samples to accomplish the transfer of the data. This is because there is an internal buffer that is separate from the shift register and the serial input is internally read at the rising edge of the sample clock, while the next value is starting to be shifted in.

When the μPD7730/77C30 operates in the sample 4-bit encode mode, it never outputs the value 00H. However, when it is in the sample 4-bit decode mode, it can accept 00H as an input value and interpret it the same as an input value of 88H.

The μPD7730/77C30 performs as a intelligent peripheral device and is controlled and programmed from the host processor. The μPD7730/77C30 offers toll quality (equivalent quality to 56 kb/s μ-law PCM) speech meeting the CCITT recommendations G.712.

Features

- Half-duplex ADPCM encoder or decoder
- Compression data rate
  - — 32 kb/s/8 kHz sampling/4-bit data
  - — 24 kb/s/8 kHz sampling/3-bit data
- Byte data (2x ADPCM data) handling
- Robust adaptation scheme for quantizer and predictors
- Selectable functions
  - — Encoder /decoder operating mode
  - — ADPCM data length 3 or 4 bit
  - — A/D and D/A conversion μ-law or linear
- Presentable voice detection threshold
- Standard microprocessor interface to the host CPU
- Easy interface to PCM combo
- Toll quality speech at 32 kb/s (meets CCITT recommendations G.712)
- Single +5 V power supply
- Low power CMOS technology (μPD77C30)
  NMOS technology (μPD7730)
- Clock frequency 8.192 MHz maximum
- 28-pin plastic DIP
- 44-pin PLCC

Ordering Information

Part Number	Type	Package
μPD7730C	NMOS	28-pin plastic DIP (600 mil)
μPD77C30C	CMOS	28-pin plastic DIP (600 mil)
μPD77C30L	CMOS	44-pin PLCC

Block Diagram