NEC

MOS INTEGRATED CIRCUIT

μPD4264160, 4265160

64 M-BIT DYNAMIC RAM
4 M-WORD BY 16-BIT, FAST PAGE MODE

Description

The μPD4264160, 4265160 are 4,194,304 words by 16 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 50-pin plastic TSOP(II).

Features

- 4,194,304 words by 16 bits organization
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD4264160-A50	396 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μPD4265160-A50	504 mW				
μPD4264160-A60	360 mW		60 ns	110 ns	40 ns
μPD4265160-A60	432 mW				
μPD4264160-A70	324 mW		70 ns	130 ns	45 ns
μPD4265160-A70	396 mW				
μPD4264160-A80	288 mW		80 ns	150 ns	50 ns
μPD4265160-A80	360 mW				

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

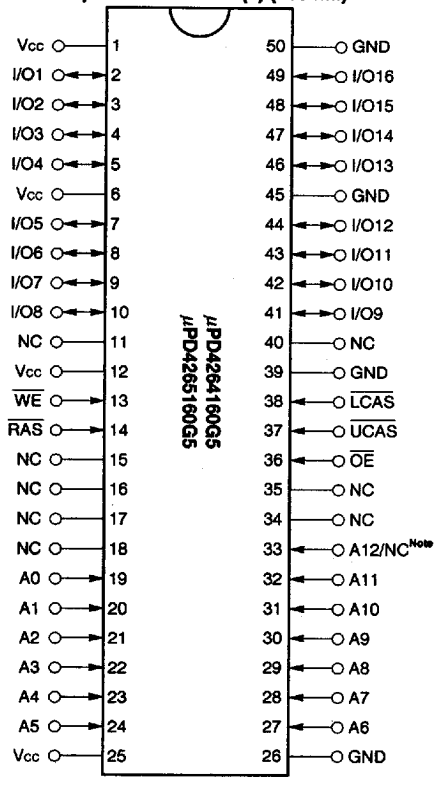
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264160	A0 - A12	A0 - A8	$\overline{RAS}$ only refresh, Normal read/write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265160	A0 - A11	A0 - A9	$\overline{RAS}$ only refresh, Normal read/write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD4264160G5-A50	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264160G5-A60	60 ns		
μPD4264160G5-A70	70 ns		
μPD4264160G5-A80	80 ns		
μPD4265160G5-A50	50 ns		
μPD4265160G5-A60	60 ns		
μPD4265160G5-A70	70 ns		
μPD4265160G5-A80	80 ns		

Pin Configuration (Marking Side)

50-pin Plastic TSOP (II) (400 mil)



Note A12 ... μPD4264160
NC ... μPD4265160

A0 to A12	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Upper Byte Column Address Strobe
$\overline{LCAS}$	:	Lower Byte Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264160, 4265160 have input pins $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{UCAS}$, $\overline{LCAS}$ (Upper, Lower column address strobe)	Input	$\overline{UCAS}$, $\overline{LCAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD4264160	A0-A12	13	9
μPD4265160	A0-A11	12	10

Electrical Specifications (Preliminary)

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μPD4264160]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		110	mA	1, 2, 3
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		100		
		I_O = 0 mA	t_{RAC} = 70 ns		90		
			t_{RAC} = 80 ns		80		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 50 ns		110	mA	1, 2, 3, 4
		t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		100		
			t_{RAC} = 70 ns		90		
			t_{RAC} = 80 ns		80		
Operating current	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		90	mA	1, 2, 5
(Fast page mode)		t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		80		
			t_{RAC} = 70 ns		70		
			t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1, 2
refresh current		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265160]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1, 2, 3
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 50 ns		140	mA	1, 2, 3, 4
		t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		120		
			t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		90	mA	1, 2, 5
		t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		80		
			t_{RAC} = 70 ns		70		
			t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1, 2
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ V_{IL} (MAX.) and $\overline{CAS}$ ≥ V_{IH} (MIN.).

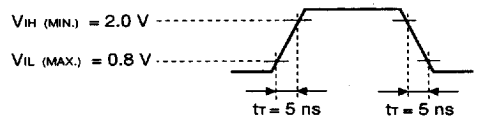
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

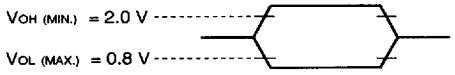
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

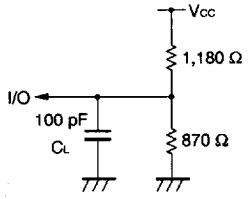
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	tRC	90	–	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time	tRP	30	–	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time	tCPN	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13	–	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time	tCSH	50	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	37	20	45	20	52	25	60	ns	1
$\overline{RAS}$ to column address delay time	tRAD	13	25	15	30	15	35	17	40	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	–	5	–	5	–	5	–	ns	2
Row address setup time	tASR	0	–	0	–	0	–	0	–	ns	
Row address hold time	tRAH	8	–	10	–	10	–	12	–	ns	
Column address setup time	tASC	0	–	0	–	0	–	0	–	ns	
Column address hold time	tCAH	13	–	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	tOES	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	tCLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	tOLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	tOED	10	–	13	–	15	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$	tMRH	0	–	0	–	0	–	0	–	ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	
Refresh time	tREF	–	64	–	64	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	128	–	153	–	175	–	195	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	–	83	–	95	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	33	–	38	–	43	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	45	–	53	–	60	–	65	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

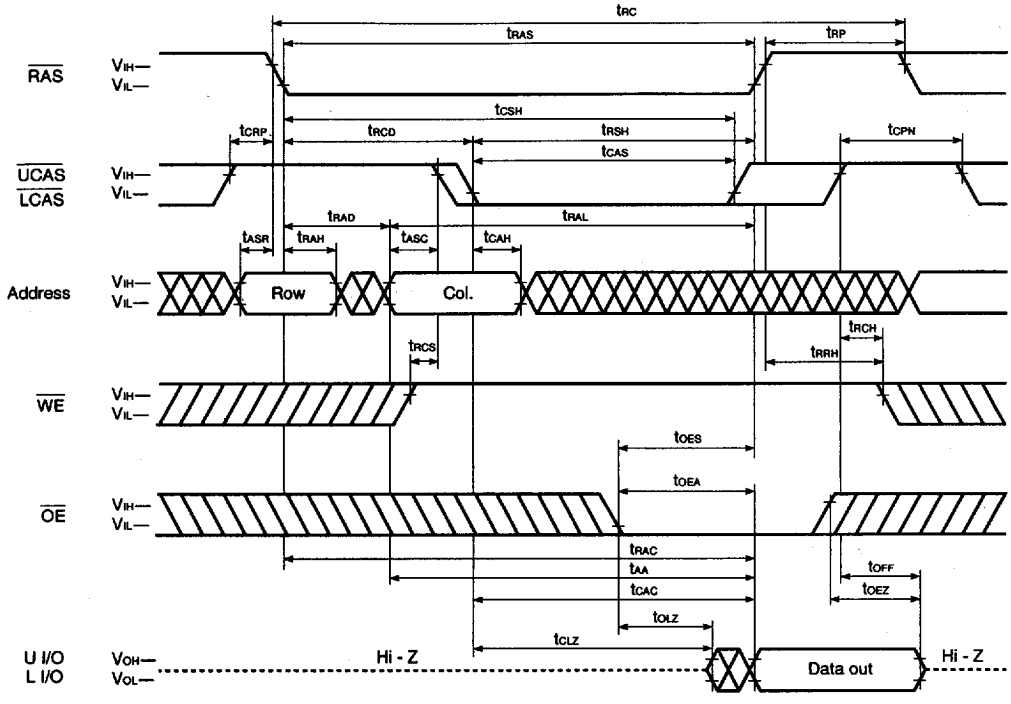
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

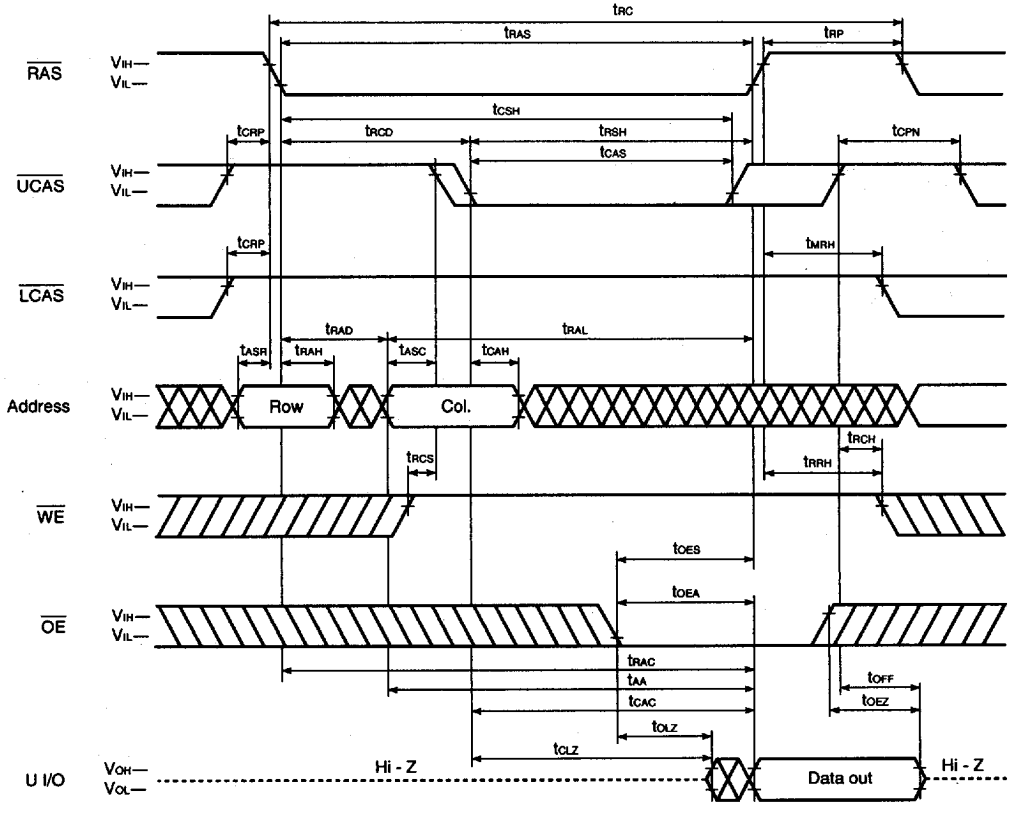
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	15	–	ns	

Read Cycle

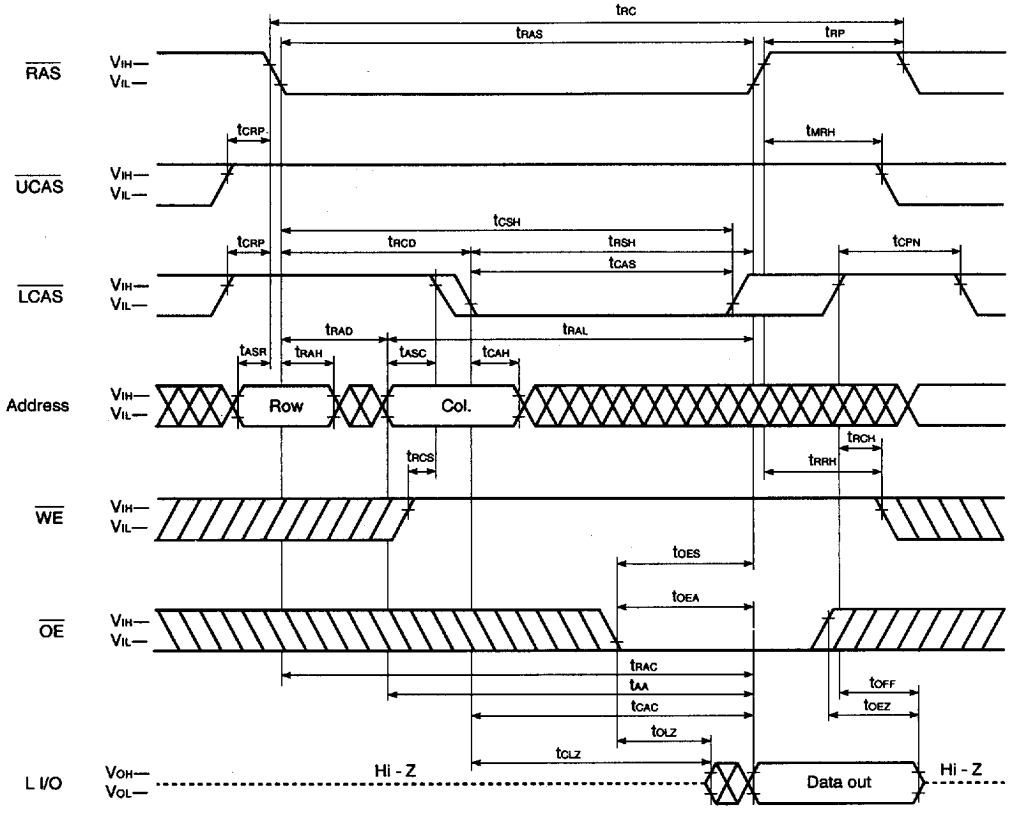


Upper Byte Read Cycle



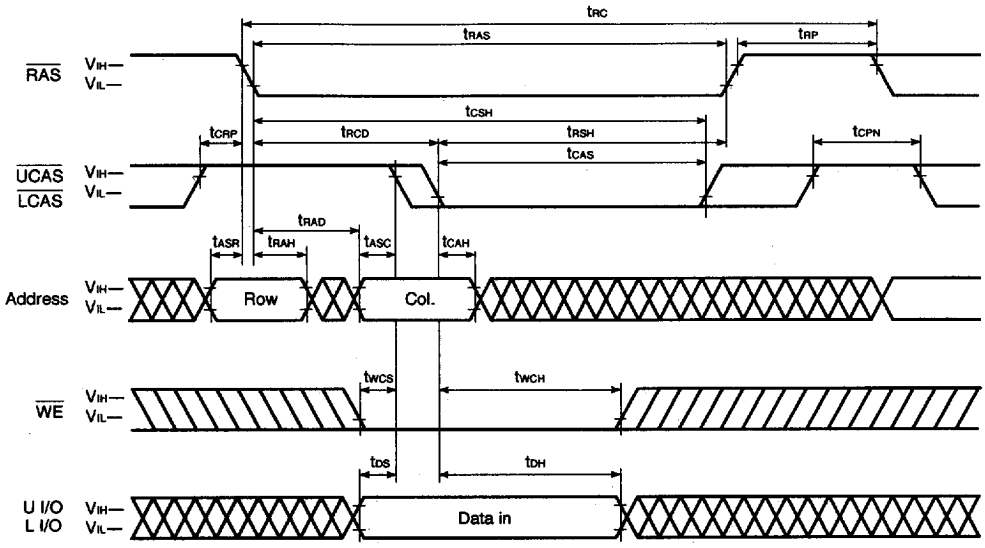
Remark L I/O: Hi-Z

Lower Byte Read Cycle



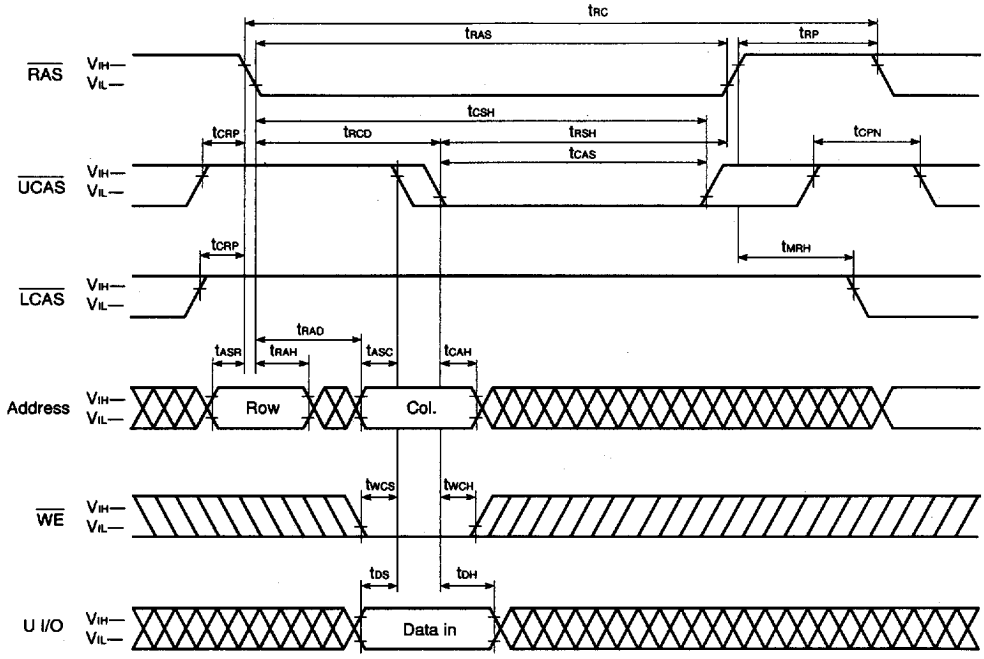
Remark U I/O: Hi-Z

Early Write Cycle



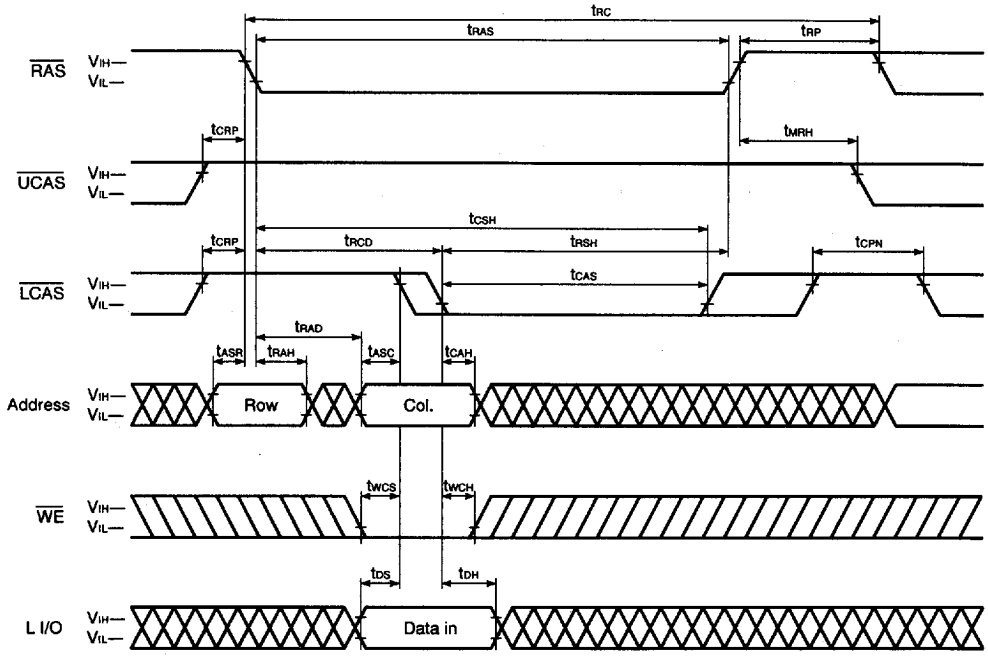
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



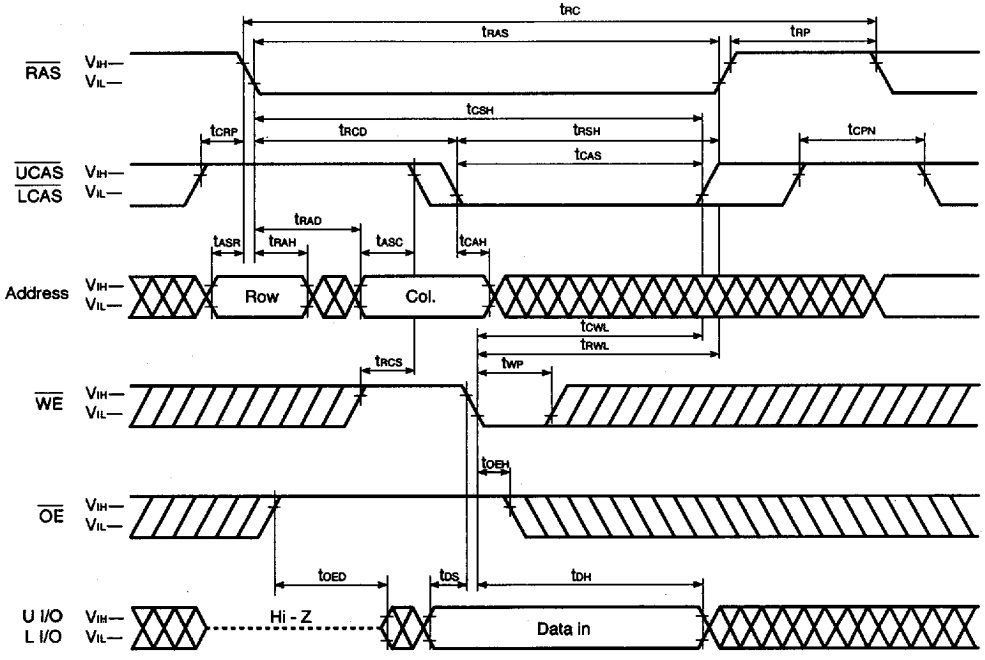
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

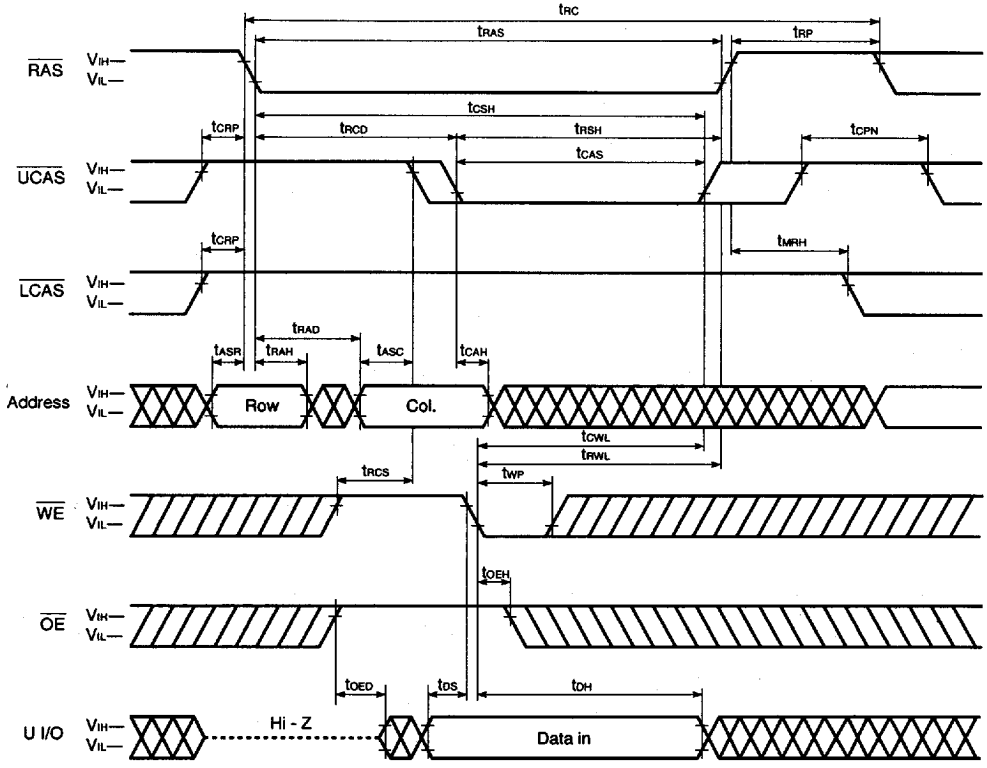


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

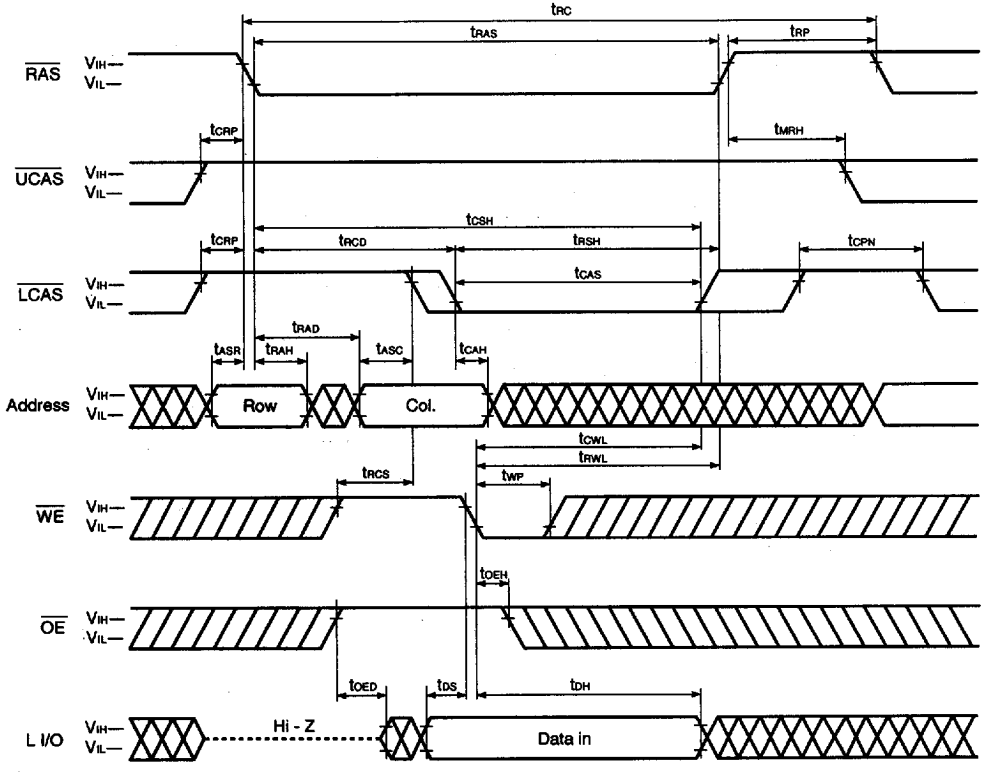


Upper Byte Late Write Cycle



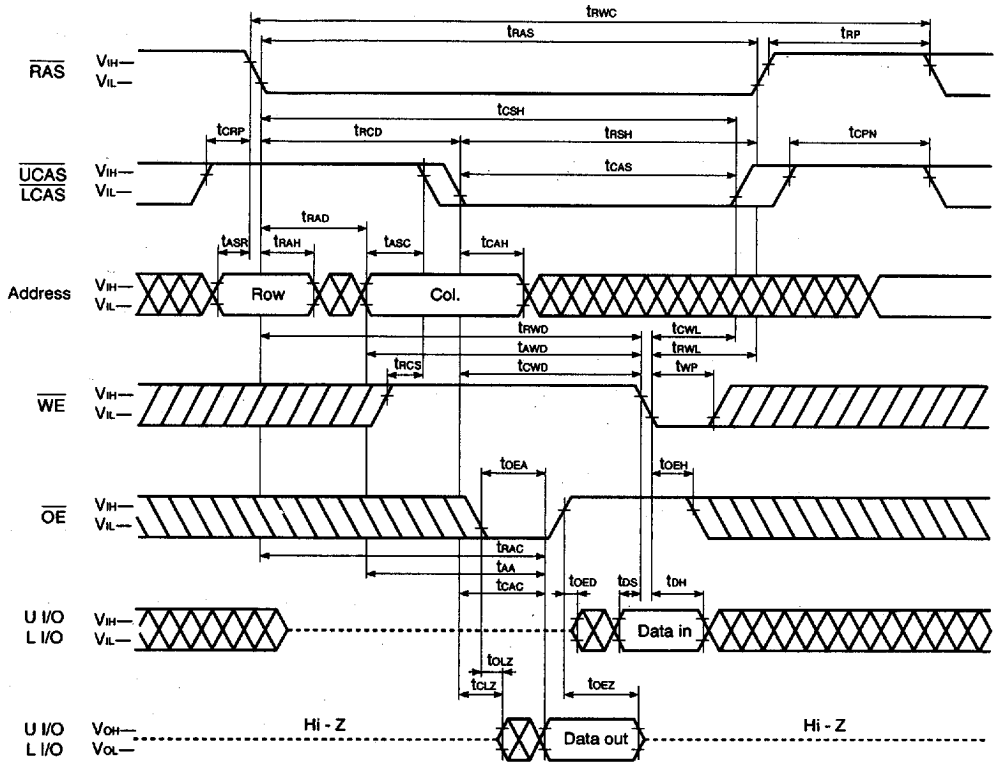
Remark L I/O: Don't care

Lower Byte Late Write Cycle

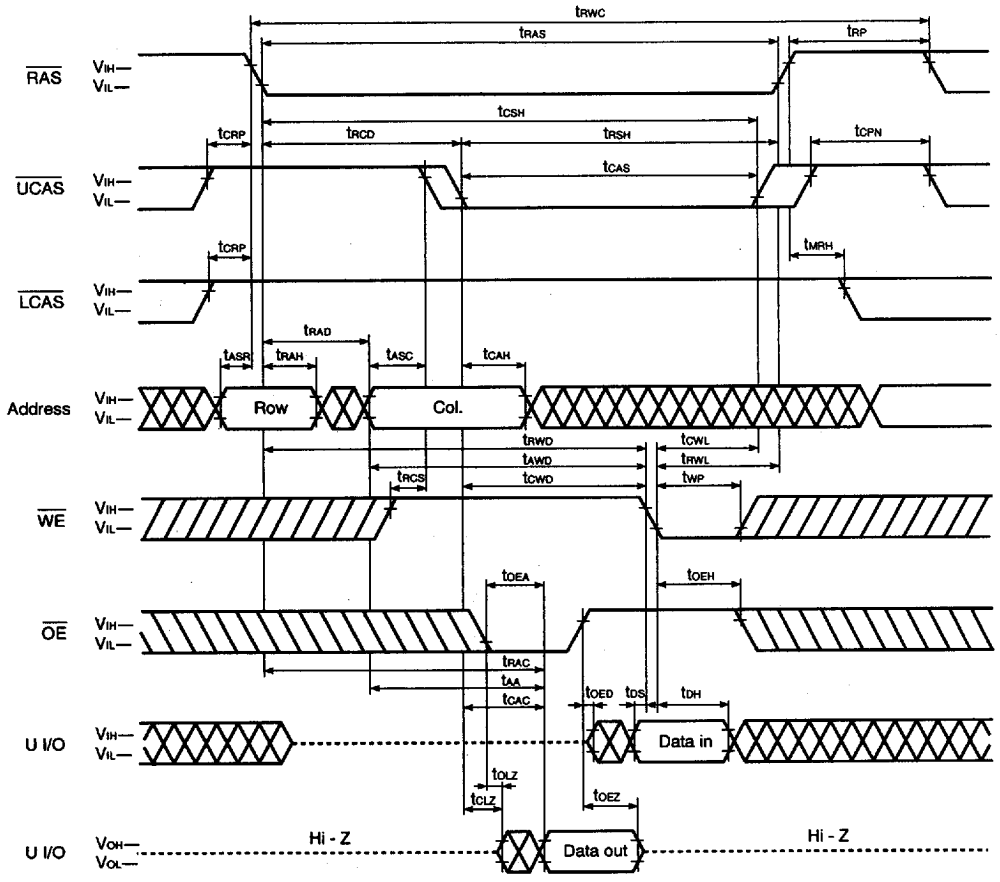


Remark U I/O: Don't care

Read Modify Write Cycle

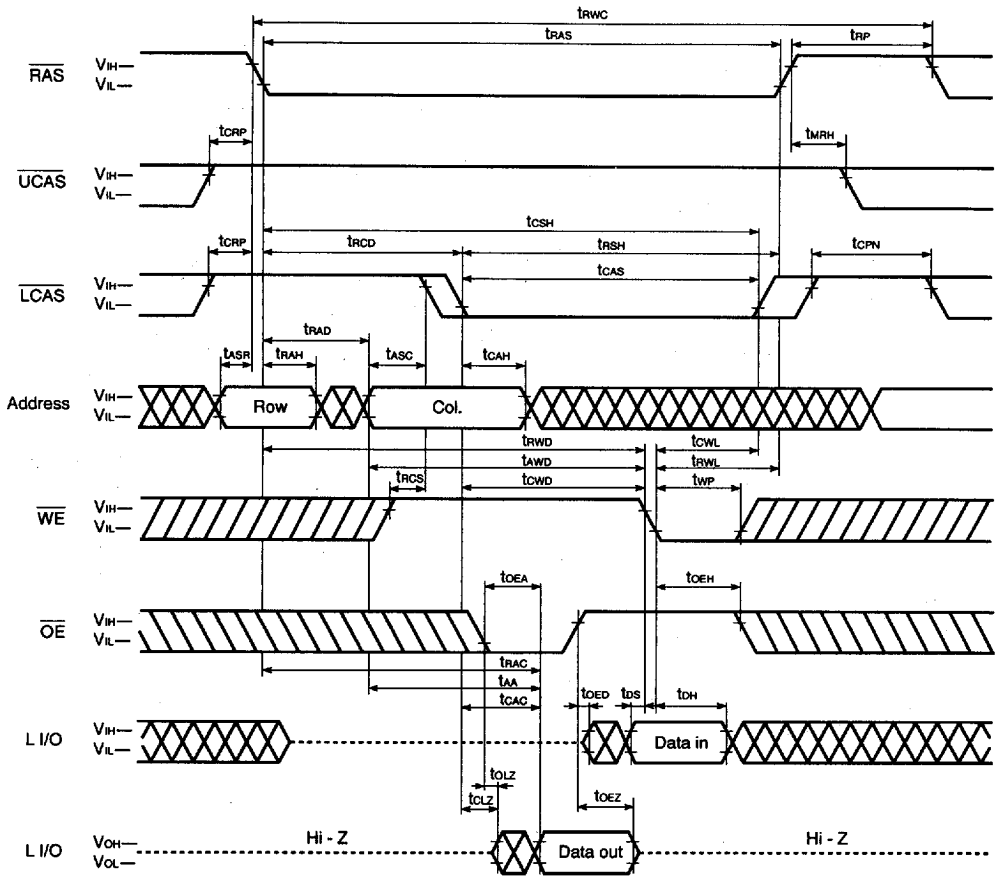


Upper Byte Read Modify Write Cycle



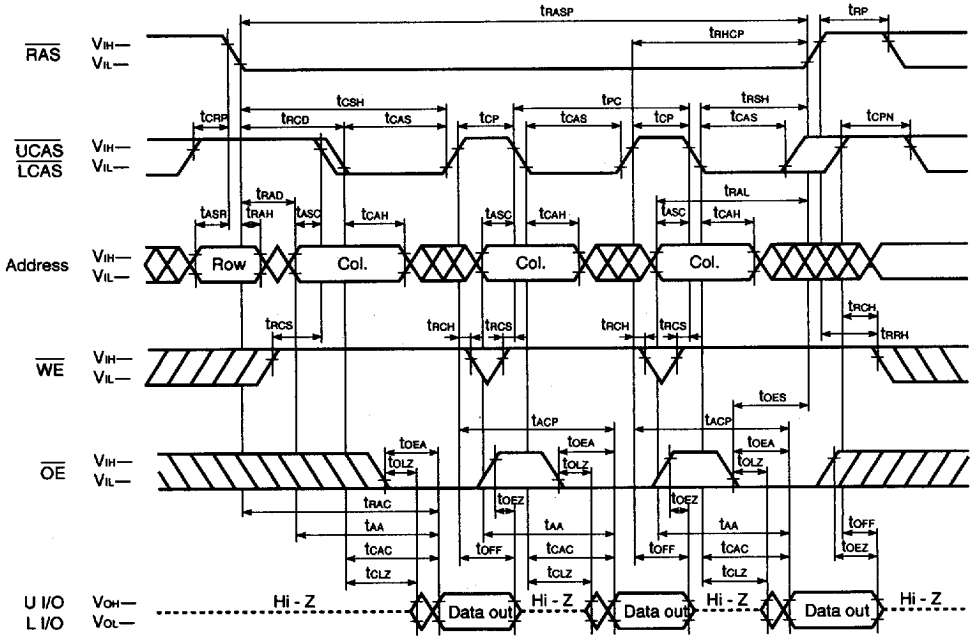
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



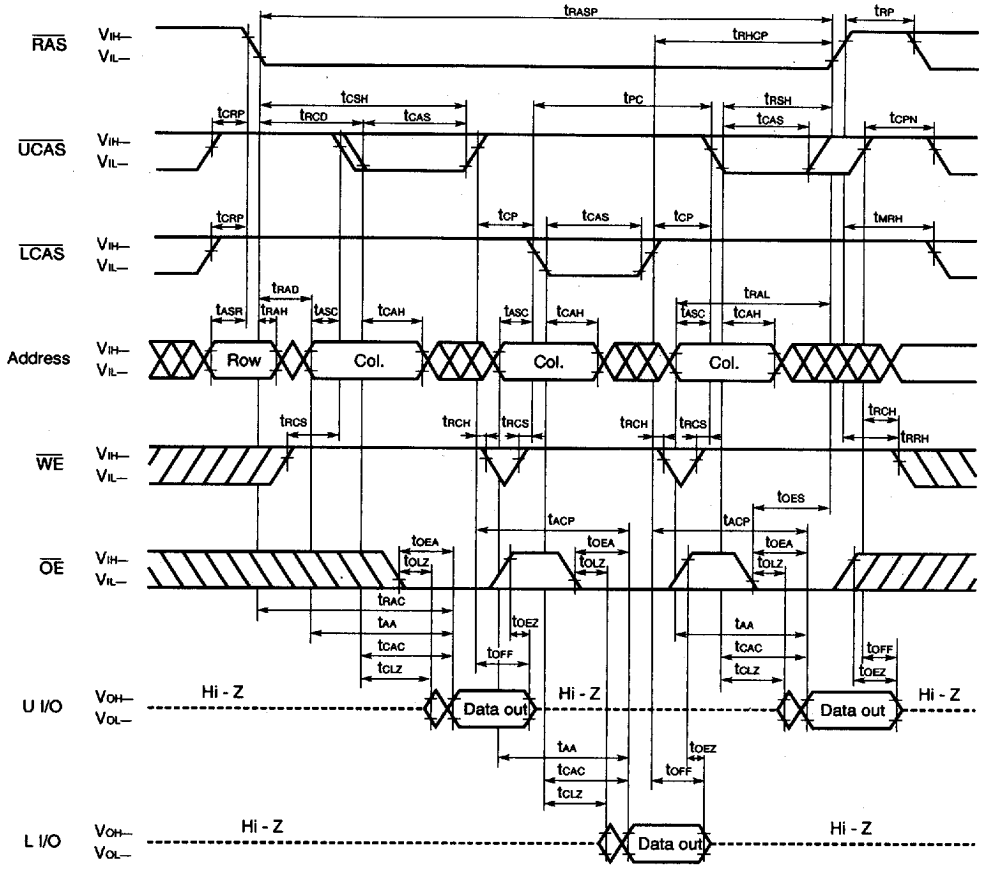
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

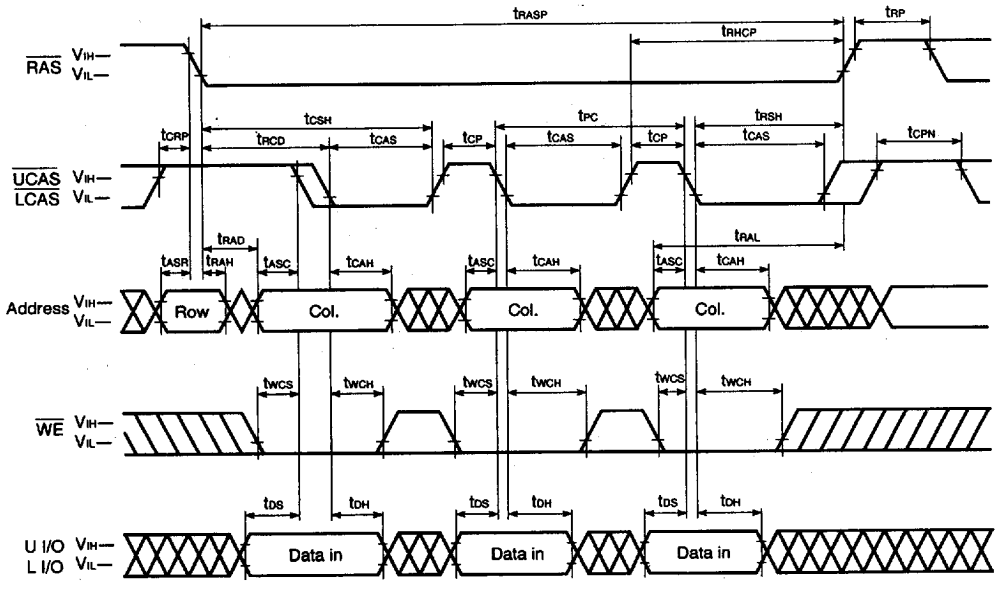
Fast Page Mode Byte Read Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

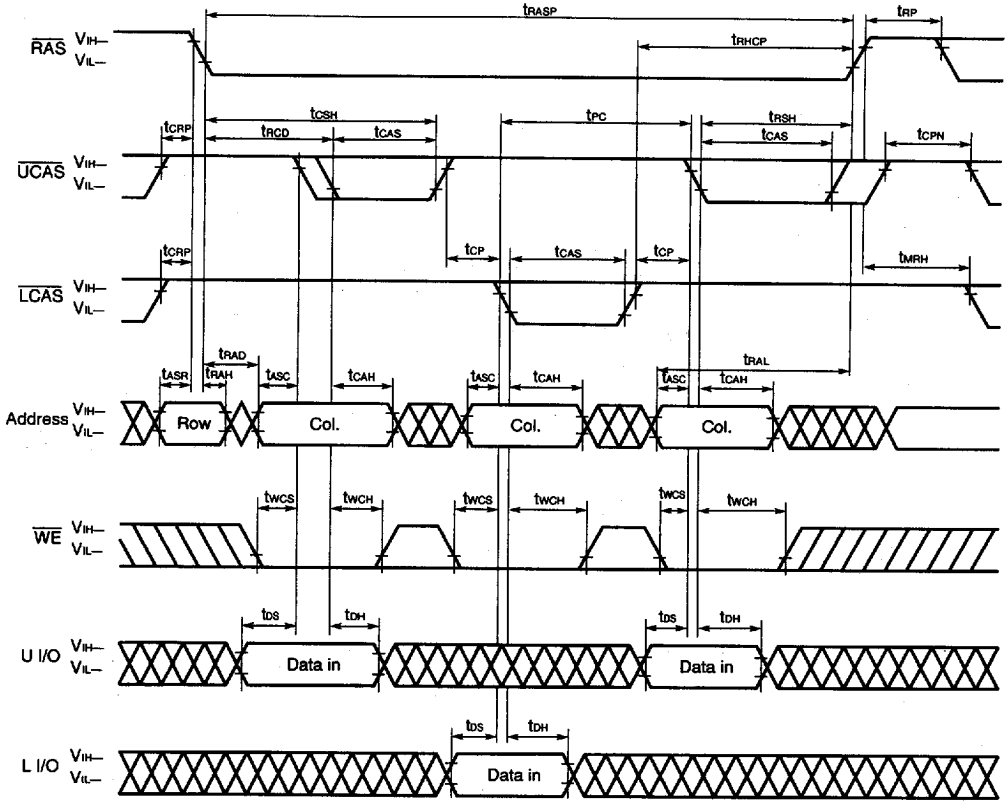
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

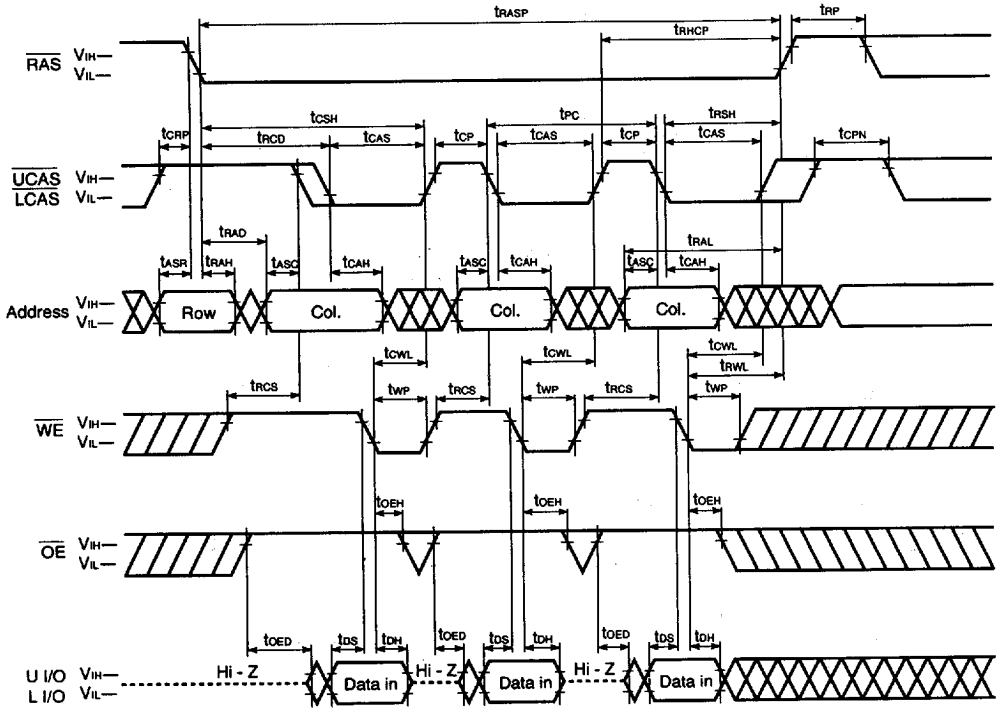
Fast Page Mode Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

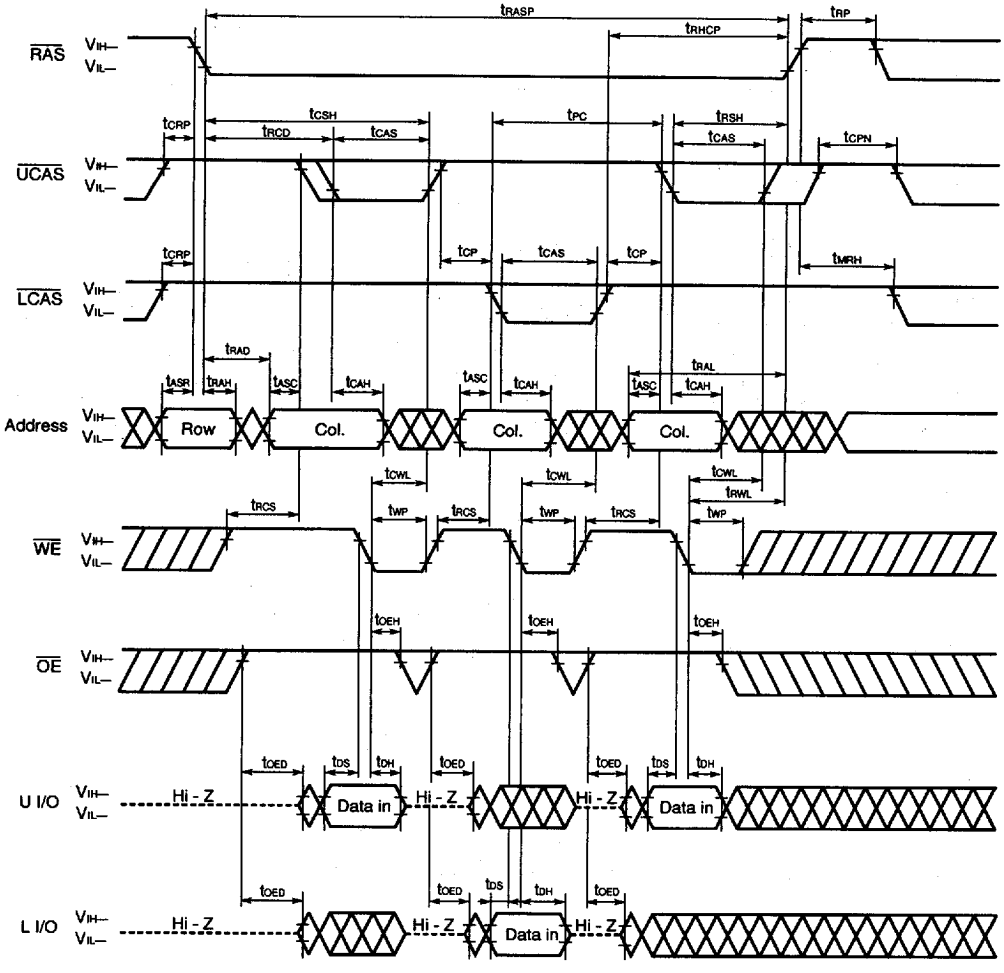
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

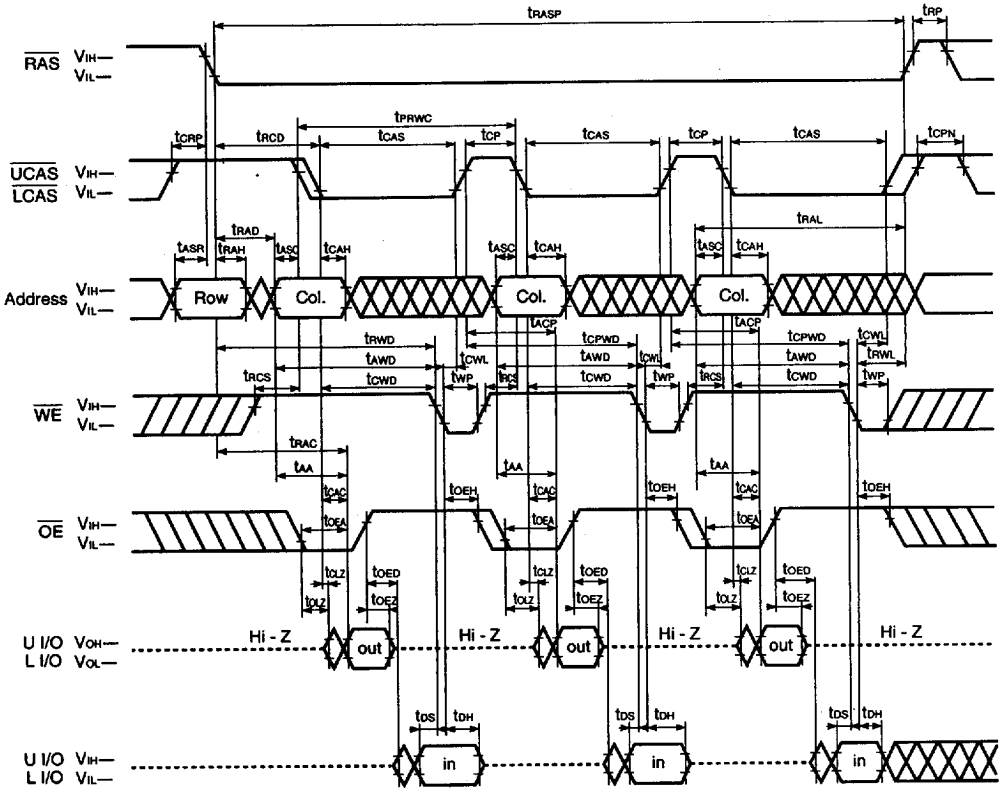
Fast Page Mode Byte Late Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

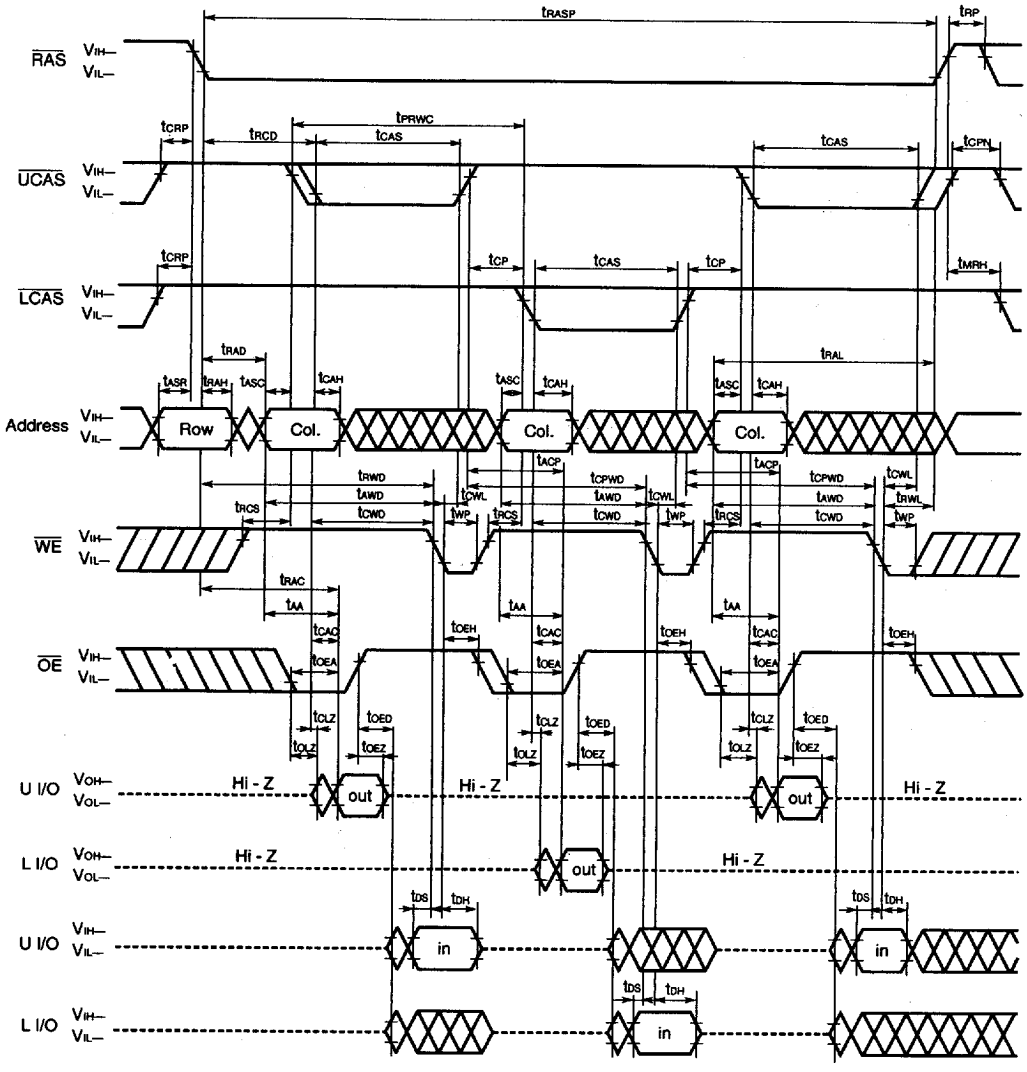
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

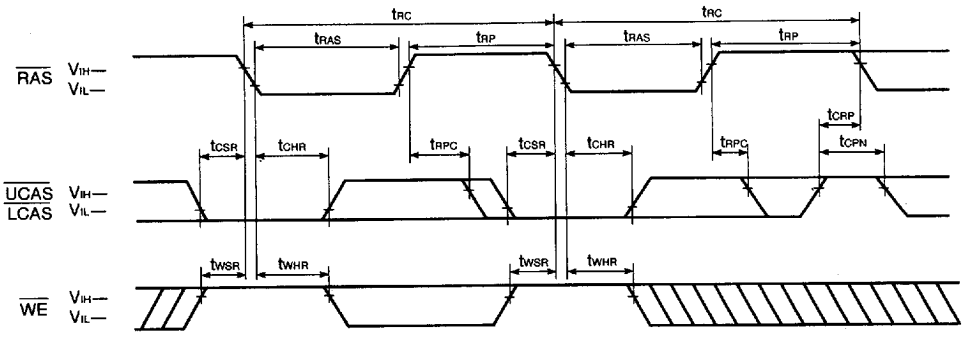
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

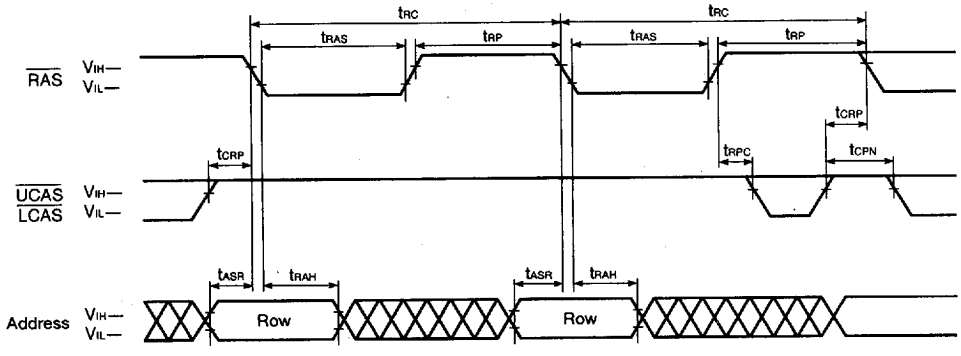
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



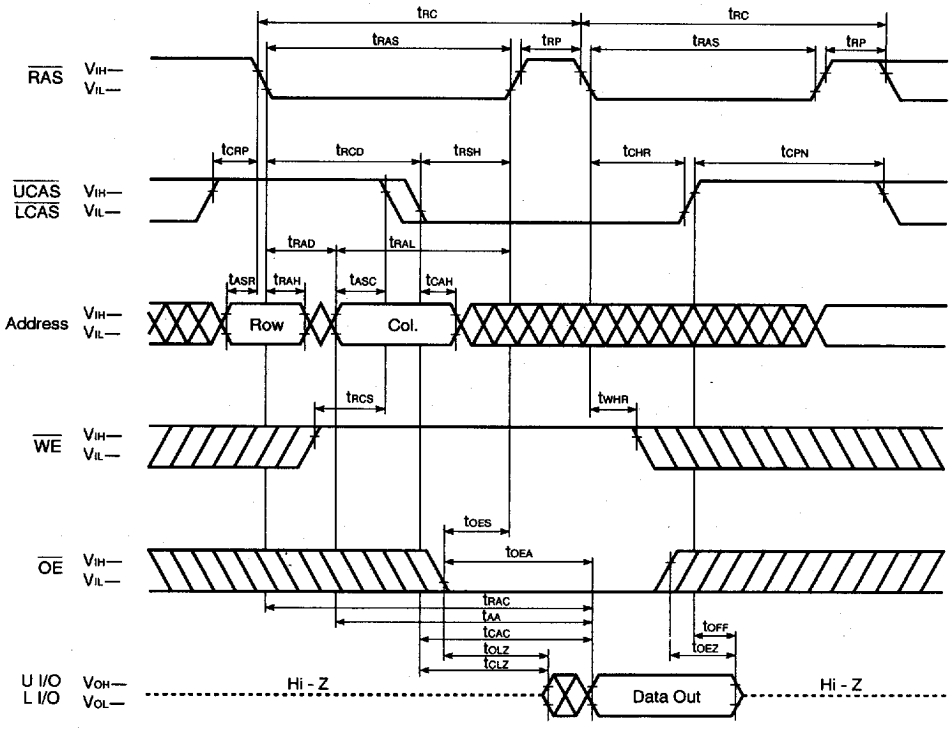
Remark Address, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

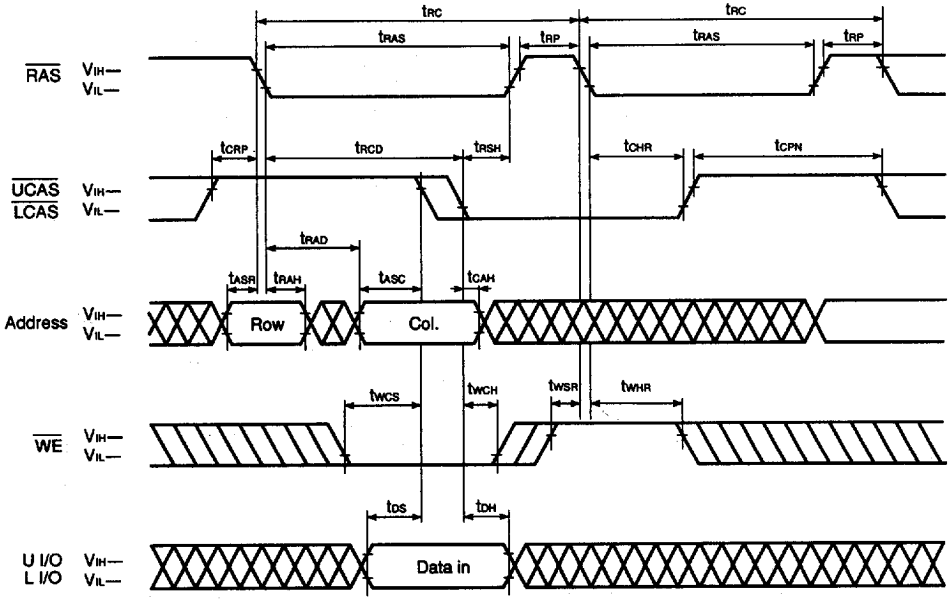


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



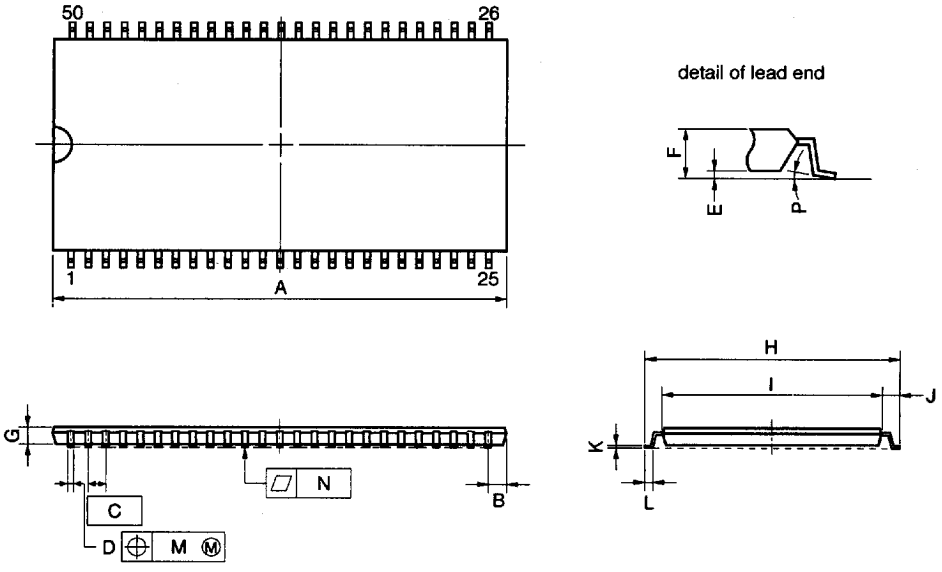
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawing

50PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF3