Burr-Brown Products from Texas Instruments

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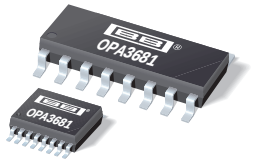
OPA3681



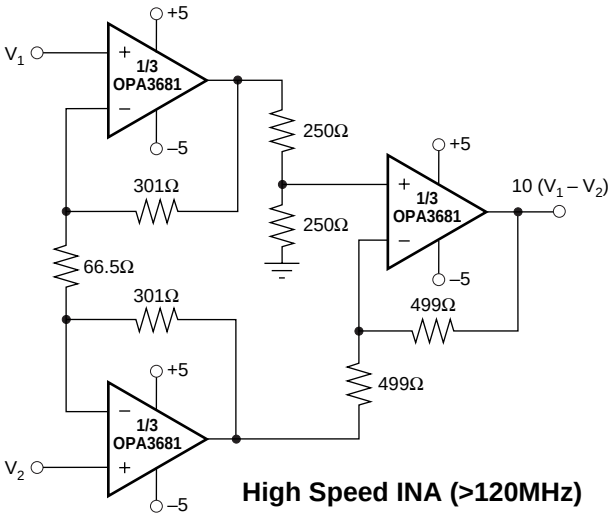
SpeedPLUS™ Triple Wideband, Current-Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- WIDEBAND +5V OPERATION: 225MHz (G = +2)
- UNITY GAIN STABLE: 280MHz (G = 1)
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 2100V/μs
- LOW SUPPLY CURRENT: 6mA/ch
- LOW DISABLED CURRENT: 300μA/ch
- IMPROVED HIGH FREQUENCY PINOUT

APPLICATIONS

- RGB AMPLIFIERS
- WIDEBAND INA
- BROADBAND VIDEO BUFFERS
- HIGH SPEED IMAGING CHANNELS
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS
- CABLE DRIVERS



High Speed INA (>120MHz)

DESCRIPTION

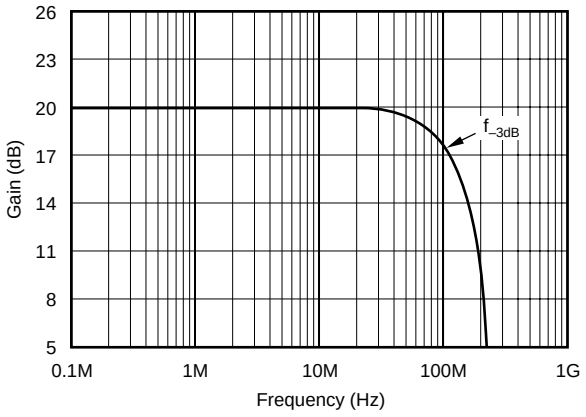
The OPA3681 sets a new level of performance for broadband triple current-feedback op amps. Operating on a very low 6mA/ch supply current, the OPA3681 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers a high output current with minimal voltage headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA3681 can deliver a 1V to 4V output swing with over 100mA drive current and 150MHz bandwidth. This combination of features makes the OPA3681 an ideal RGB line driver or single-supply ADC input driver.

The OPA3681's low 6mA/ch supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, guarantees lower guaranteed maximum supply current than competing products. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it high, gives normal operation. If pulled low, the OPA3681 supply current drops to less than 300μA/ch while the output goes into a high impedance state. This feature may be used for power savings or for video MUX applications.

OPA3681 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage Feedback	OPA680	OPA2680	OPA3680
Current Feedback	OPA681	OPA2681	OPA3681
Fixed Gain	OPA682	OPA2682	OPA3682

DIFFERENTIAL TO SINGLE-ENDED FREQUENCY RESPONSE



TEXAS INSTRUMENTS

SPECIFICATIONS: $V_S = \pm 5V$

$R_F = 499\Omega$, $R_L = 100\Omega$, and G = +2, (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA3681E, U TYP +25°C	OPA3681E, U GUARANTEED +25°C[2]	OPA3681E, U GUARANTEED 0°C to 70°C[3]	OPA3681E, U GUARANTEED –40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE (Figure 1)								
Small Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, $R_F = 549\Omega$	280				MHz	typ	C
	G = +2, $R_F = 499\Omega$	220	220	210	190	MHz	min	B
	G = +5, $R_F = 365\Omega$	185				MHz	typ	C
	G = +10, $R_F = 182\Omega$	125				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O = 0.5Vp-p	90	50	45	45	MHz	min	B
Peaking at a Gain of +1	$R_F = 453$, V_O = 0.5Vp-p	0.4	2	4		dB	max	B
Large Signal Bandwidth	G = +2, V_O = 5Vp-p	150				MHz	typ	C
Slew Rate	G = +2, 4V Step	2100	1600	1600	1200	V/µs	min	B
Rise/Fall Time	G = +2, V_O = 0.5V Step	1.7				ns	typ	C
	G = +2, 5V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	$R_L = 100\Omega$	–75				dBc	typ	C
	$R_L \geq 500\Omega$	–81				dBc	typ	C
3rd Harmonic	$R_L = 100\Omega$	–80				dBc	typ	C
	$R_L \geq 500\Omega$	–95				dBc	typ	C
Input Voltage Noise	f > 1MHz	2.2	3.0	3.4	3.6	nV/√Hz	max	B
Non-Inverting Input Current Noise	f > 1MHz	12	14	15	15	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15	18	18	19	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.001				%	typ	C
	$R_L = 37.5\Omega$	0.005				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.01				deg	typ	C
	$R_L = 37.5\Omega$	0.05				deg	typ	C
Crosstalk	Input Referred, f = 5MHz, All Hostile	–55				dBc	typ	C
DC PERFORMANCE[4]								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 100\Omega$	100	**56**	56	56	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.3	**±5**	±6.5	±7.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			+35	+40	µV/°C	max	B
Non-Inverting Input Bias Current	V_{CM} = 0V	+30	**+55**	±65	±85	µA	max	A
Average Non-Inverting Input Bias Current Drift	V_{CM} = 0V			–400	–450	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	**±40**	±50	±55	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			–125	–150	nA°/C	max	B
INPUT								
Common-Mode Input Range[5]		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Common-Mode Rejection (CMR)	V_{CM} = 0V	52	**47**	46	45	dB	min	A
Non-Inverting Input Impedance		100 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open Loop	42				Ω	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	$R_L = 100\Omega$	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing	V_O = 0	+190	**+160**	+140	+80	mA	min	A
Current Output, Sinking	V_O = 0	–150	**–135**	–130	–80	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C
DISABLE (Disabled Low)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–960				µA	typ	C
Disable Time		100				ns	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±50				mV	typ	C
Turn Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	V_{DIS} = 0, Each Channel	100	**160**	160	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Max Quiescent Current (3 Channels)	V_S = ±5V	18	**19.2**	19.5	19.8	mA	max	A
Min Quiescent Current (3 Channels)	V_S = ±5V	18	**16.8**	16.5	15.0	mA	min	A
Power Supply Rejection Ratio (–PSRR)	Input Referred	58	52	50	49	dB	min	A
TEMPERATURE RANGE								
Specification: E, U		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
E SSOP-16		100				°C/W	typ	C
U SO-16		100				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C guaranteed specifications. (3) Junction temperature = ambient at low temperature limit: Junction temperature = ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

SPECIFICATIONS: V_S = +5V

R_F = 499Ω, R_L = 100Ω to V_S/2, G = +2, (Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA3681E, U						TEST LEVEL(1)
		TYP	GUARANTEED					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	
AC PERFORMANCE (Figure 2)								
Small Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, R_F = 549Ω	250				MHz	typ	C
	G = +2, R_F = 499Ω	225	180	140	110	MHz	min	B
	G = +5, R_F = 365Ω	180				MHz	typ	C
	G = +10, R_F = 182Ω	165				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	100	50	35	23	MHz	min	B
Peaking at a Gain of +1	R_F = 649Ω, V_O < 0.5Vp-p	0.4	2	4		dB	max	B
Large Signal Bandwidth	G = +2, V_O = 2Vp-p	200				MHz	typ	C
Slew Rate	G = +2, 2V Step	830	700	680	570	V/µs	min	B
Rise/Fall Time	G = +2, V_O = 0.5V Step	1.5				ns	typ	C
	G = +2, V_O = 2V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	14				ns	typ	C
0.1%	G = +2, V_O = 2V Step	9				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	R_L = 100Ω to V_S/2	–75				dBc	typ	C
	R_L ≥ 500Ω to V_S/2	–79				dBc	typ	C
3rd Harmonic	R_L = 100Ω to V_S/2	–68				dBc	typ	C
	R_L ≥ 500Ω to V_S/2	–70				dBc	typ	C
Input Voltage Noise	f > 1MHz	2.2	3	3.4	3.6	nV/√Hz	max	B
Non-Inverting Input Current Noise	f > 1MHz	12	14	14	15	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15	18	18	19	pA/√Hz	max	B
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 100Ω to V_S/2	100	**60**	53	51	kΩ	min	A
Input Offset Voltage	V_{CM} = 2.5V	±1	**±5**	±6.0	±7	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			+15	+20	µV/°C	max	B
Non-Inverting Input Bias Current	V_{CM} = 2.5V	+40	**+65**	+75	+95	µA	max	A
Average Non-Inverting Input Bias Current Drift	V_{CM} = 2.5V			–300	–350	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 2.5V	±5	**±20**	±25	±35	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 2.5V			–125	–175	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.5	**1.6**	1.7	1.8	V	max	A
Most Positive Input Voltage(5)		3.5	**3.4**	3.3	3.2	V	min	A
Common-Mode Rejection (CMR)	V_{CM} = V_S/2	51	**45**	44	44	dB	min	A
Non-Inverting Input Impedance		100 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open Loop	44				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4	**3.8**	3.7	3.5	V	min	A
	R_L = 100Ω, 2.5V	3.9	**3.7**	3.6	3.4	V	min	A
Least Positive Output Voltage	No Load	1	**1.2**	1.3	1.5	V	max	A
	R_L = 100Ω, 2.5V	1.1	**1.3**	1.4	1.6	V	max	A
Current Output, Sourcing	V_O = V_S/2	150	**110**	110	60	mA	min	A
Current Output, Sinking	V_O = V_S/2	–110	**–75**	–70	–50	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C
DISABLE (Disable Low)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–810				µA	typ	C
Disable Time		100				ns	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S /2	±50				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S /2	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	100				µA	typ	C
POWER SUPPLY								
Specified Single Supply Operating Voltage		5				V	typ	C
Maximum Single Supply Operating Voltage			**12**	12	12	V	max	A
Max Quiescent Current (3 Channels)	V_S = +5V	14.4	**16.2**	16.5	16.5	mA	max	A
Min Quiescent Current (3 Channels)	V_S = +5V	14.4	**12.3**	11.1	10.8	mA	min	A
Power Supply Rejection Ratio (+PSRR)	Input Referred	48				dB	typ	C
TEMPERATURE RANGE								
Specification: E, U		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
E SSOP-16		100				°C/W	typ	C
U SO-16		100				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C guaranteed specifications. (3) Junction temperature = ambient at low temperature limit: Junction temperature = ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ±CMIR limits.

ABSOLUTE MAXIMUM RATINGS

Power Supply	±6.5VDC
Internal Power Dissipation[1]	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: E, U	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

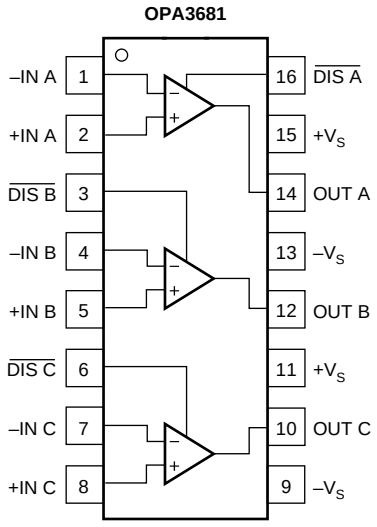
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View **SSOP-16, SO-16**



PACKAGE/ORDERING INFORMATION

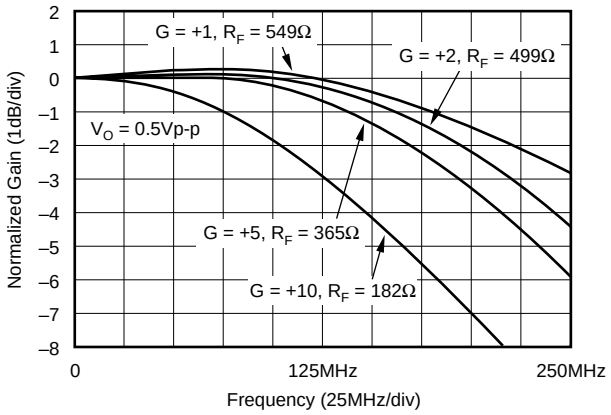
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA
OPA3681E	SSOP-16 Surface Mount	322	–40°C to +85°C	OPA3681E	OPA3681E/250	Tape and Reel
"	"	"	"	"	OPA3681E/2K5	Tape and Reel
OPA3681U	SO-16 Surface Mount	265	–40°C to +85°C	OPA3681U	OPA3681U	Rails
"	"	"	"	"	OPA3681U/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA3681E/2K5" will get a single 2500-piece Tape and Reel.

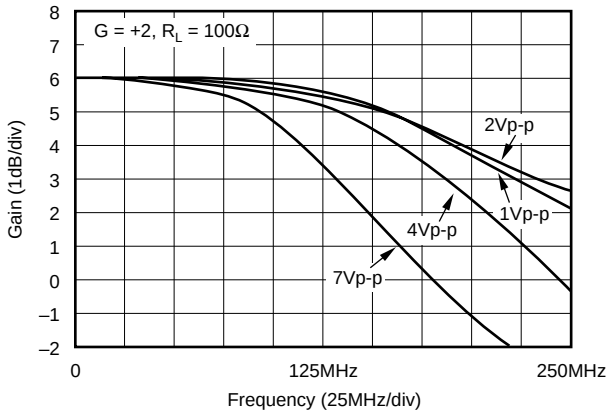
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

G = +2, R_F = 499Ω, and R_L = 100Ω, unless otherwise noted (see Figure 1).

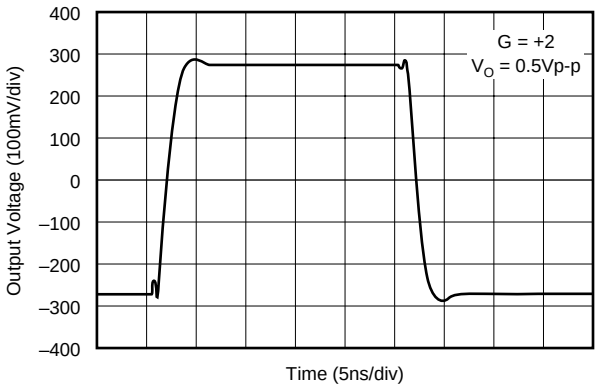
SMALL-SIGNAL FREQUENCY RESPONSE



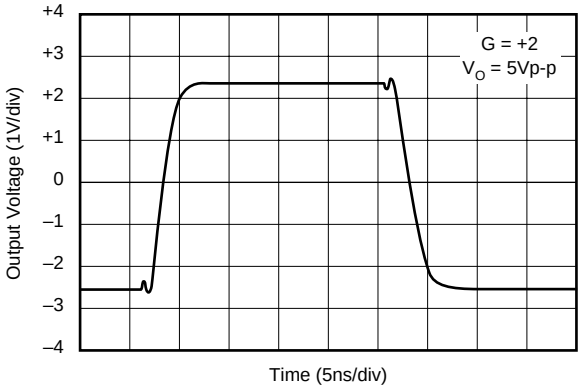
LARGE-SIGNAL FREQUENCY RESPONSE



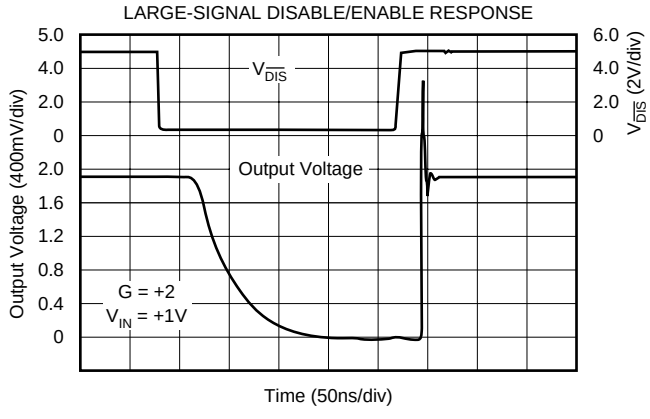
SMALL-SIGNAL PULSE RESPONSE



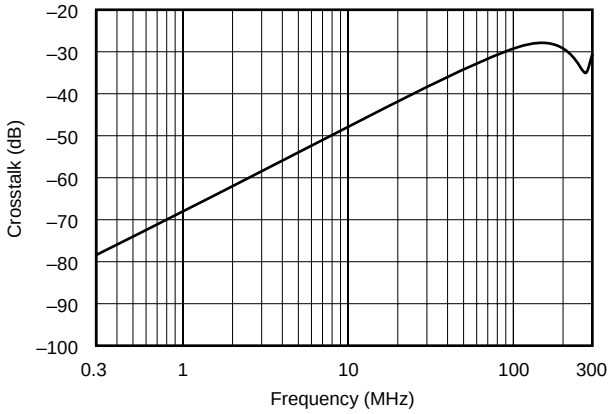
LARGE-SIGNAL PULSE RESPONSE



LARGE-SIGNAL DISABLE/ENABLE RESPONSE



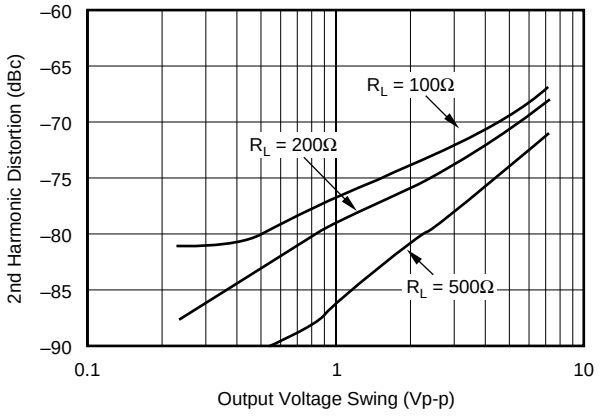
ALL HOSTILE CROSSTALK



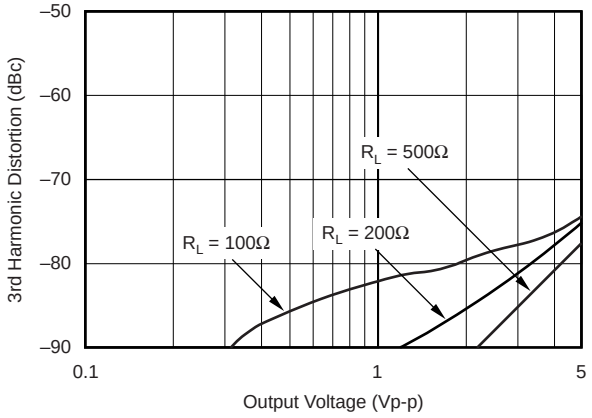
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2, R_F = 499Ω, and R_L = 100Ω, unless otherwise noted (see Figure 1).

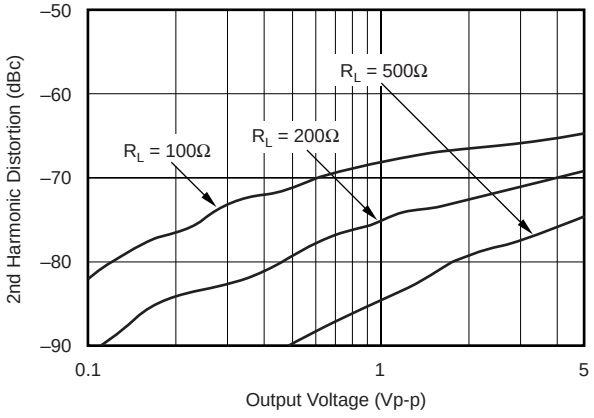
5MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



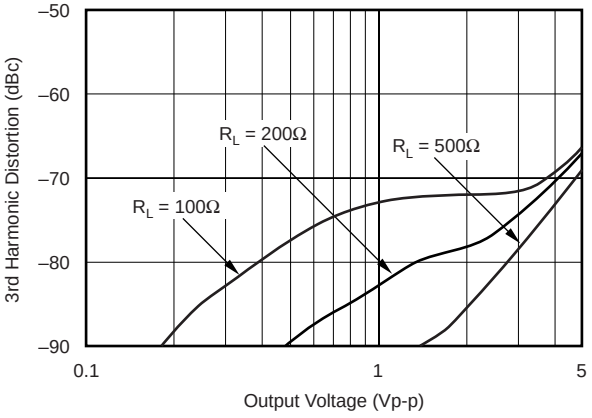
5MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



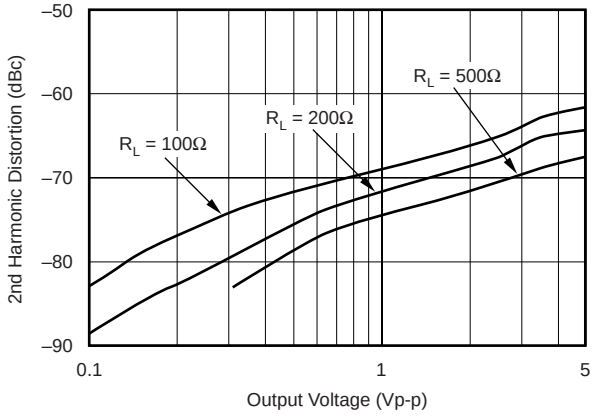
10MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



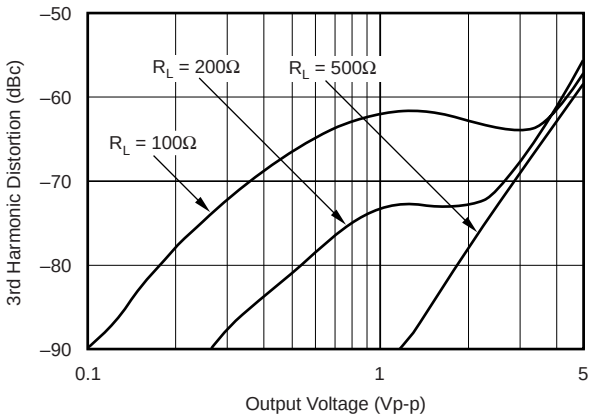
10MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



20MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



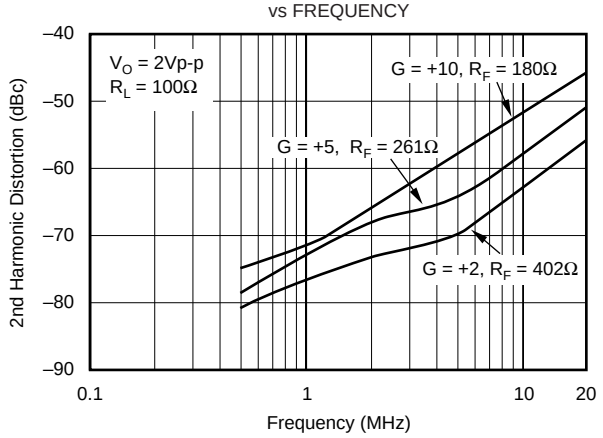
20MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



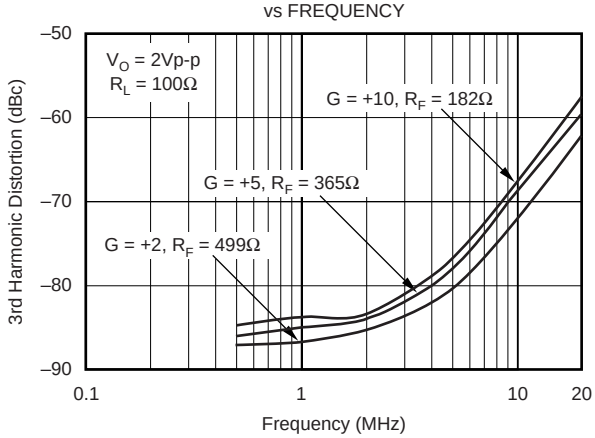
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2, R_F = 499Ω, and R_L = 100Ω, unless otherwise noted (see Figure 1).

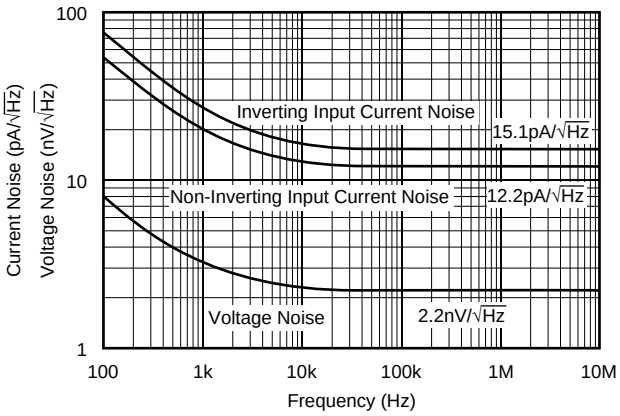
2nd HARMONIC DISTORTION vs FREQUENCY



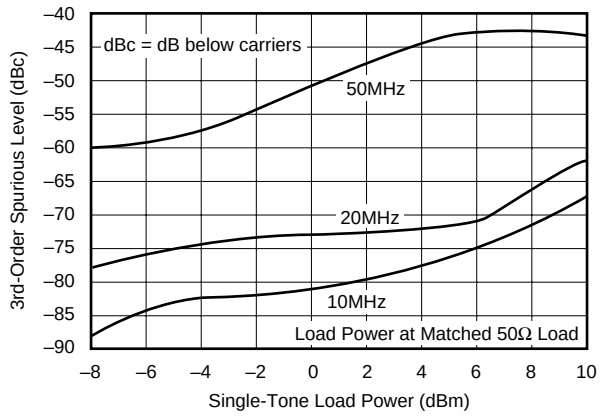
3rd HARMONIC DISTORTION vs FREQUENCY



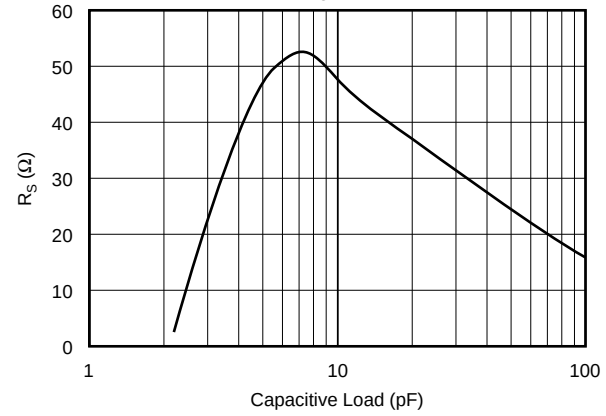
INPUT VOLTAGE AND CURRENT NOISE DENSITY



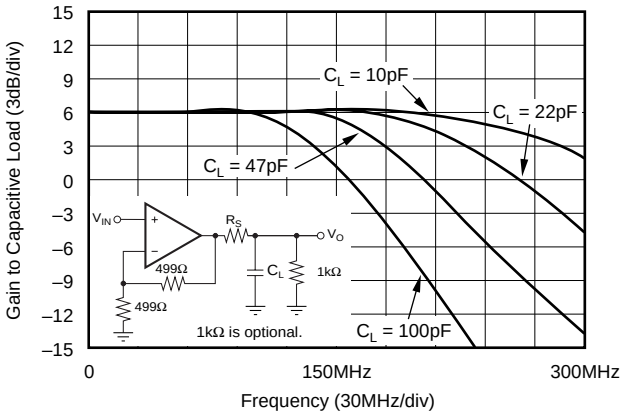
TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS



RECOMMENDED R_S vs CAPACITIVE LOAD



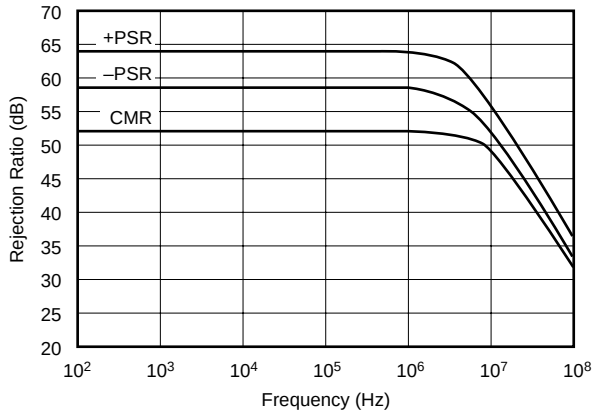
FREQUENCY RESPONSE vs CAPACITIVE LOAD



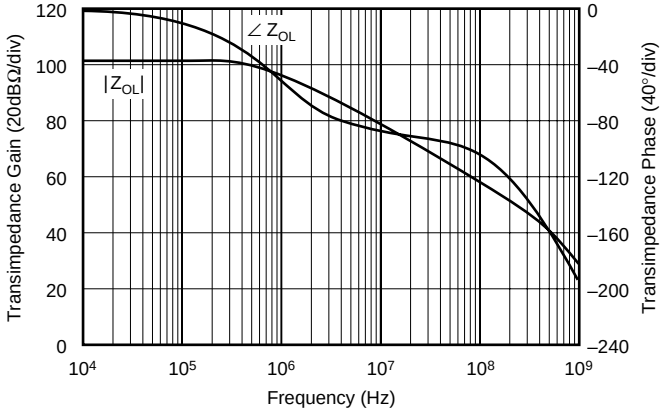
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2, R_F = 499Ω, and R_L = 100Ω, unless otherwise noted (see Figure 1).

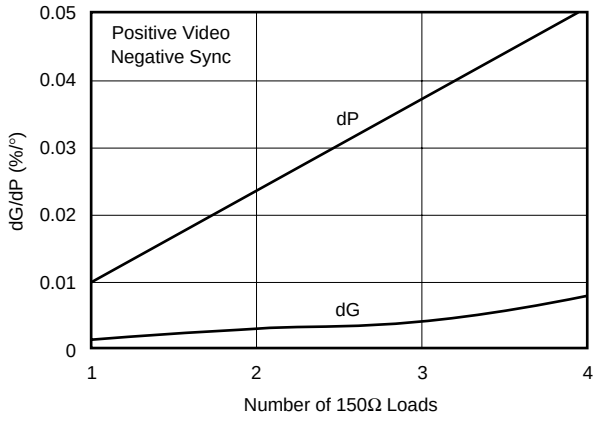
CMR AND PSR vs FREQUENCY



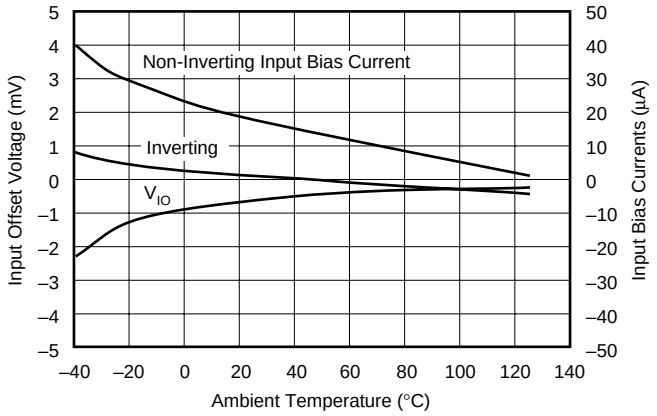
OPEN-LOOP TRANSIMPEDANCE GAIN/PHASE



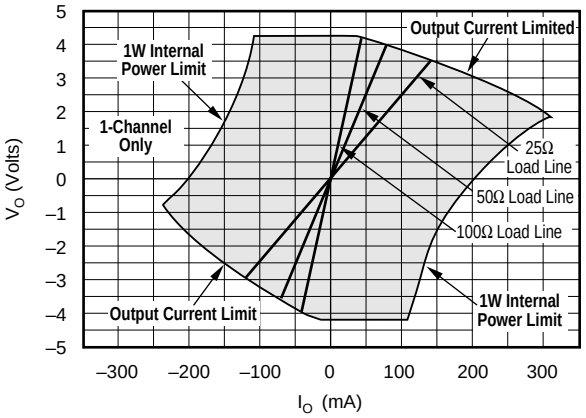
COMPOSITE VIDEO dG/dP



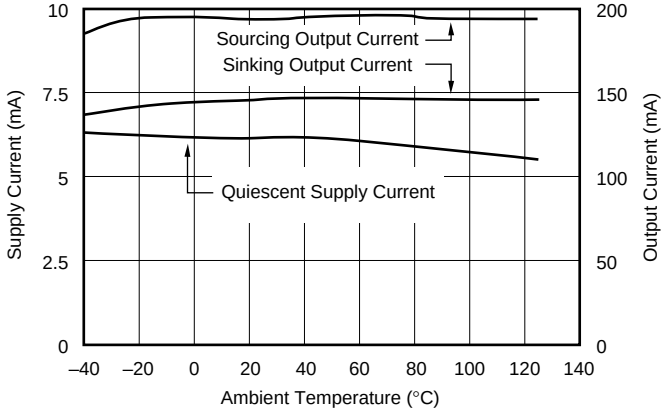
TYPICAL DC DRIFT OVER TEMPERATURE



OUTPUT VOLTAGE AND CURRENT LIMITATIONS



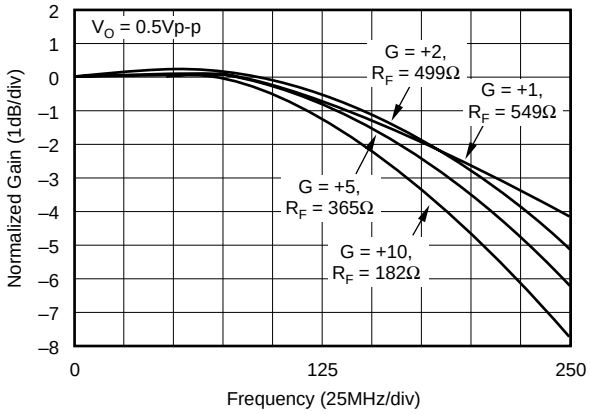
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



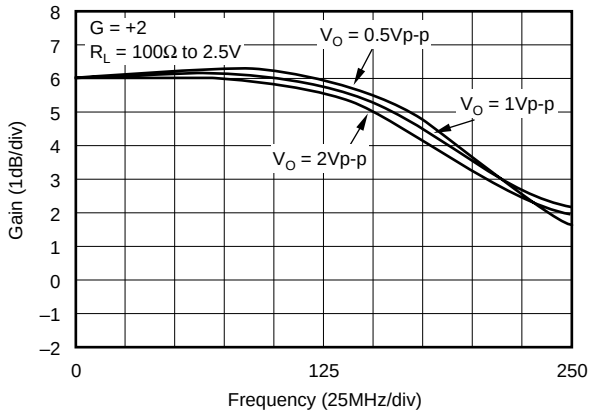
TYPICAL PERFORMANCE CURVES: V_S = +5V

G = +2, R_F = 499Ω, and R_L = 100Ω, unless otherwise noted (see Figure 1).

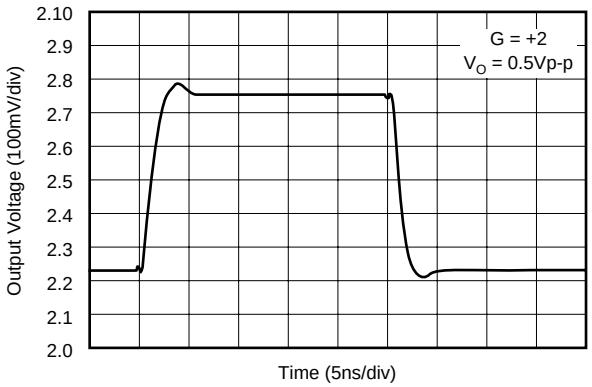
SMALL-SIGNAL FREQUENCY RESPONSE



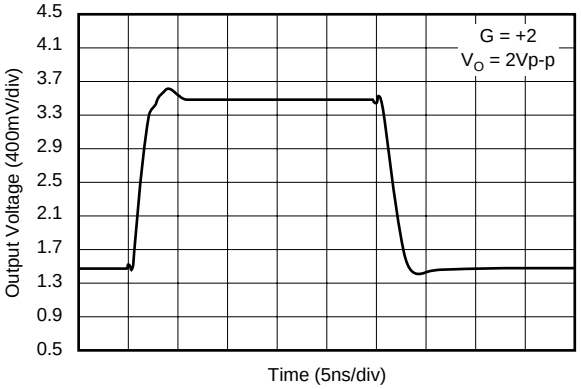
LARGE-SIGNAL FREQUENCY RESPONSE



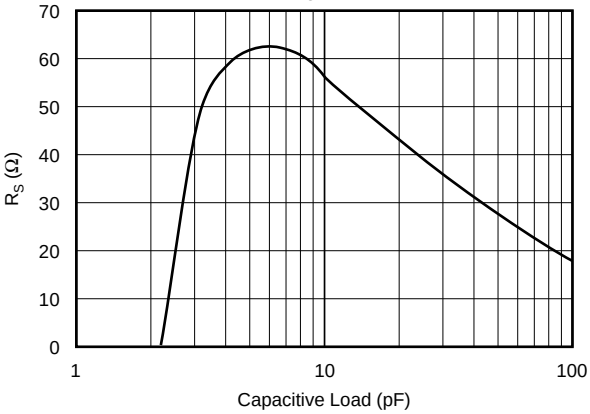
SMALL-SIGNAL PULSE RESPONSE



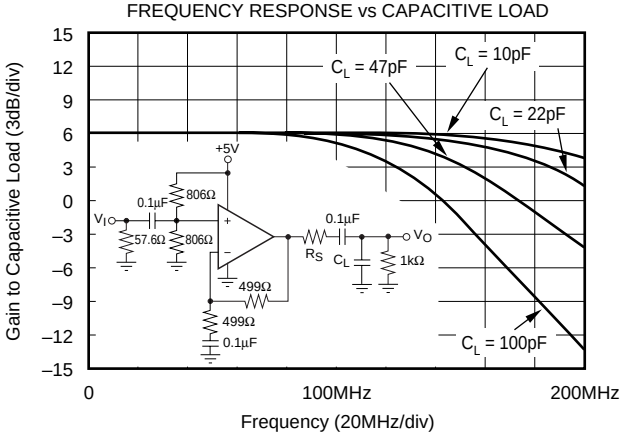
LARGE-SIGNAL PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



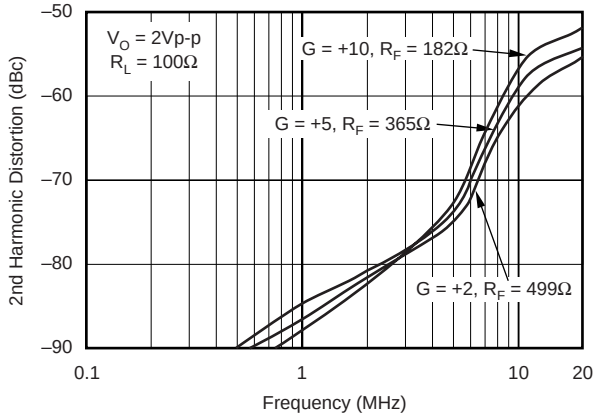
FREQUENCY RESPONSE vs CAPACITIVE LOAD



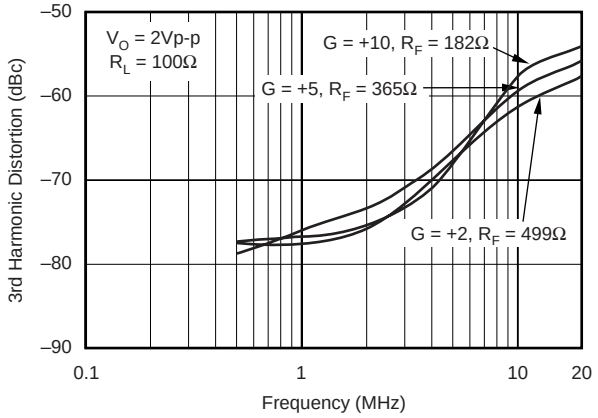
TYPICAL PERFORMANCE CURVES: V_S = +5V (Cont.)

G = +2, R_F = 499Ω, and R_L = 100Ω, unless otherwise noted (see Figure 1).

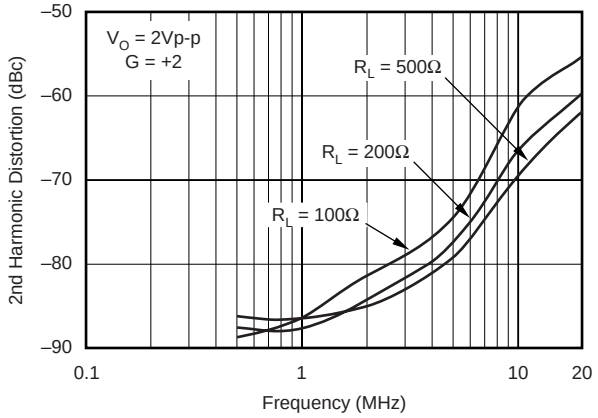
2nd HARMONIC DISTORTION vs FREQUENCY



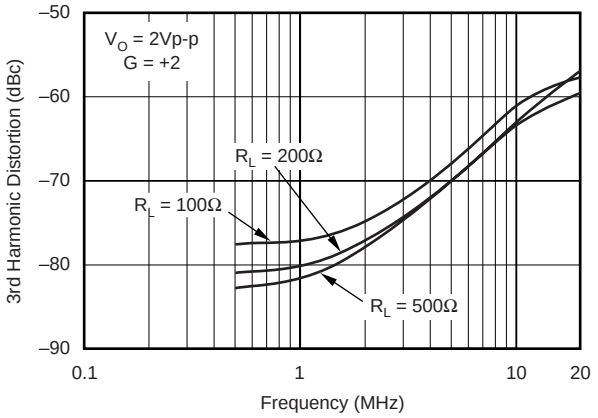
3rd HARMONIC DISTORTION vs FREQUENCY



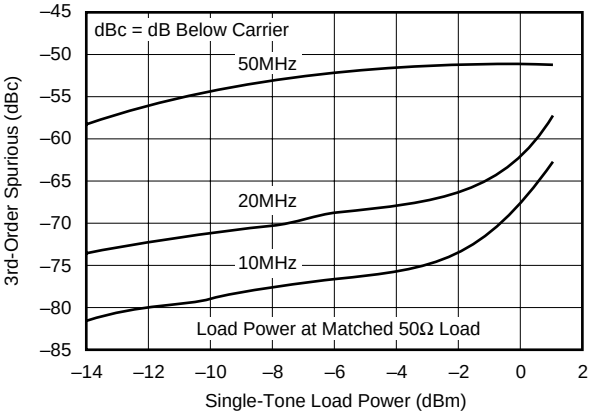
2nd HARMONIC DISTORTION vs FREQUENCY



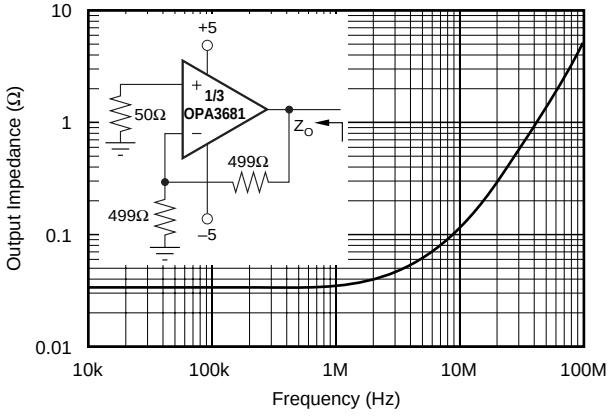
3rd HARMONIC DISTORTION vs FREQUENCY



TWO-TONE, 3rd-ORDER SPURIOUS LEVEL



CLOSED-LOOP OUTPUT IMPEDANCE



APPLICATIONS INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA3681 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear, high power output stage. Requiring only 6mA/ch quiescent current, the OPA3681 will swing to within 1V of either supply rail and deliver in excess of 135mA guaranteed at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA3681 will deliver greater than 200MHz bandwidth driving a 2Vp-p output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers have typically suffered from very poor crossover distortion as the output current goes through zero. The OPA3681 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain.

Figure 1 shows the DC-coupled, gain of +2, dual power supply circuit configuration used as the basis of the ±5V Specifications and Typical Performance Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 998Ω. The disable control line ($\overline{DIS}$) is typically left open to guarantee normal amplifier operation. One optional component is included in Figure 1. In addition to the usual power supply de-coupling capacitors to ground, a 0.1µF capacitor is included between the two power supply pins. In practical PC board layouts, this optionally added capacitor will typically improve the 2nd harmonic distortion performance by 3dB to 6dB.

Figure 2 shows the AC-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Specifications and Typical Performance Curves. Though not a "rail-to-rail" design, the OPA3681 requires minimal input and output voltage headroom compared to other very wideband current-feedback op amps. It will deliver a 3Vp-p output swing on a single +5V supply with greater than 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a 2Vp-p input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the input DC bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 75mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA3681 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, 3rd harmonic distortion plots.

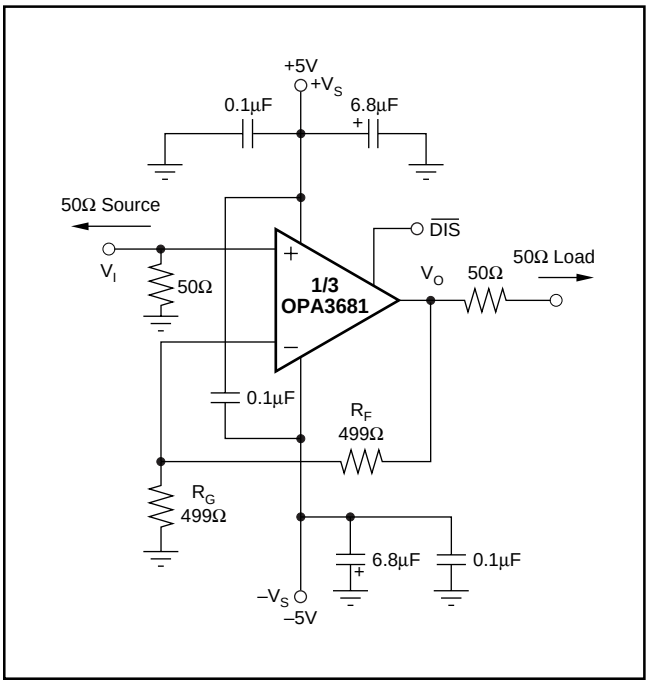


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

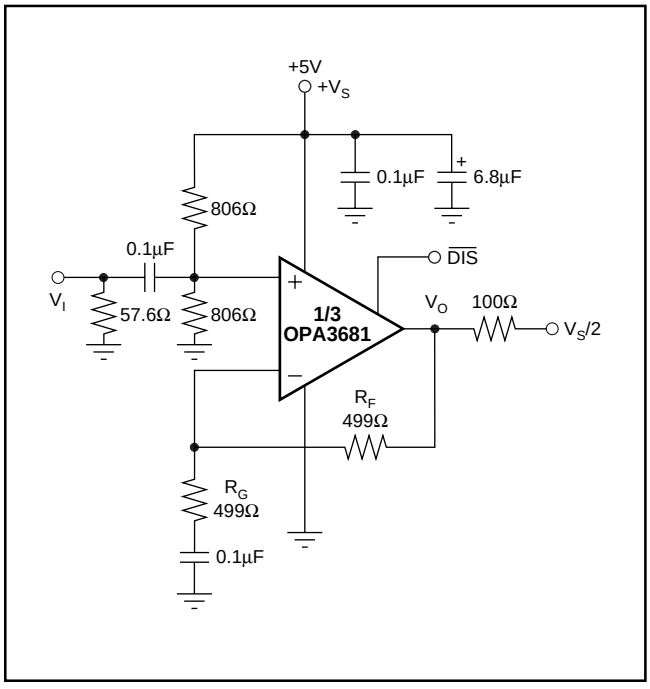


FIGURE 2. AC-Coupled, G = +2, Single Supply, Specification and Test Circuit.

TRIPLE ADC BUFFER CHANNEL

The OPAx681 family is ideally suited to single supply, wideband ADC driving. A current feedback op amp is ideal where high gains with high bandwidths are required. The wide 3Vp-p output swing with over 150MHz full power bandwidth on a single +5V supply is well suited to the 2Vp-p input range commonly required from modern CMOS pipelined ADCs. Three channels of very high speed digitizer channels are shown in Figure 3 using the OPA3681 driving three ADS831s (8-bit, 80Msps CMOS converters). Each input is AC-coupled into a 50Ω gain resistor that also will act as a 50Ω impedance match at high frequencies. The amplifier's inputs and outputs are centered on the ADC common-mode input voltage by tying each converter's V_{CM} to the non-inverting inputs of the amplifier. This V_{CM} acts as the swing midpoint for the input to the converter. Since the ADS831 can operate with differential inputs, driving into the $\overline{IN}$ input will give a net non-inverting signal channel even with the amplifiers operating at an inverting gain of –6. The other input to the ADS831 is tied to this V_{CM} as well to give an input signal midpoint equal to V_{CM}. The 300Ω feedback resistor will be the output load in this configuration. Harmonic distortion for the OPA3681 will not degrade the converter's SFDR performance in this application.

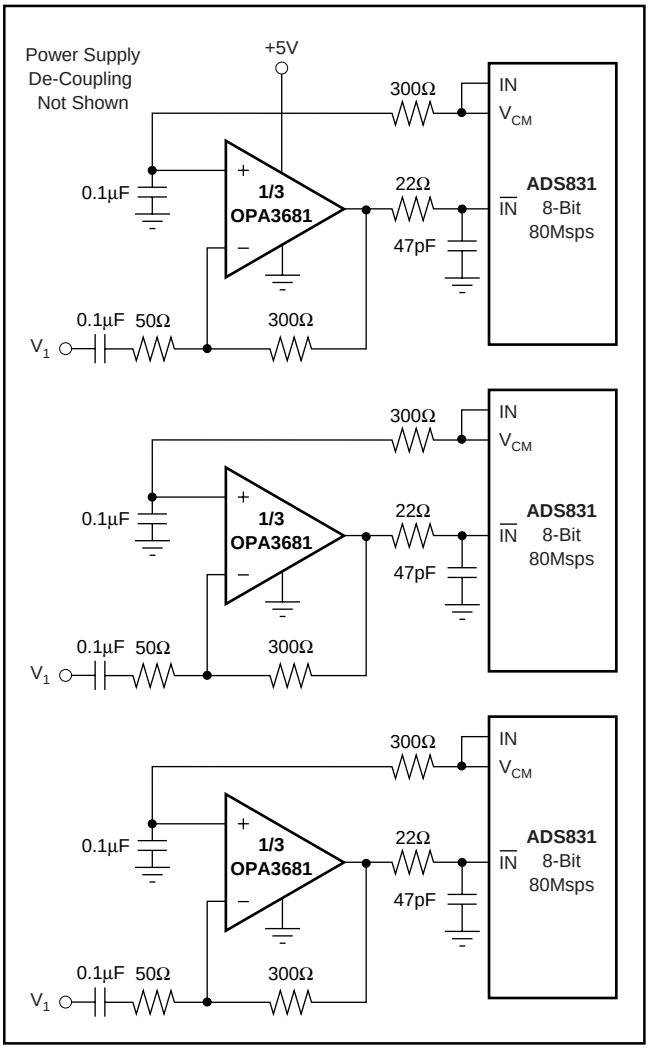


FIGURE 3. ADC Driver.

WIDEBAND RGB MULTIPLEXER

The OPA3681 is ideally suited to implementing a simple, very wideband, 2x1 RGB multiplexer. This simple "wired-OR video multiplexer" can be easily implemented using the circuit shown in Figure 4.

This circuit uses two OPA3681s where each package accepts the three RGB component video signals from one of two possible sources. Each non-inverting input is terminated

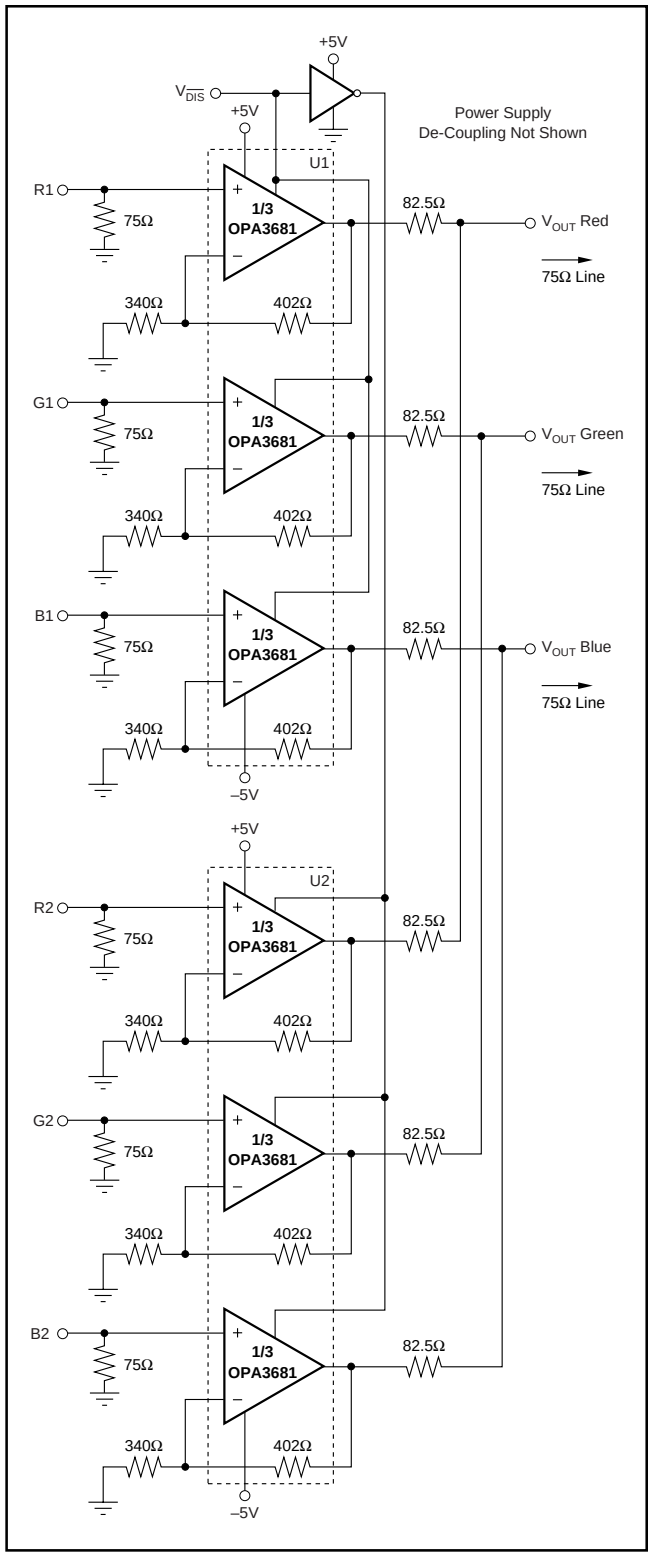


FIGURE 4. Wideband 2x1 RGB Multiplexer.

in 75Ω to match the typical video source impedance. The disable control is used to switch between channels by feeding a logic control line directly to all three $V_{\overline{DIS}}$ inputs on one package, and its complement to the three $V_{\overline{DIS}}$ inputs on the other. Since the disable feature is intentionally make-before-break (to ensure that the output does not float in transition), each of the two possible outputs for the three RGB lines are combined through a limiting resistor. This 82.5Ω resistor limits the current between the two outputs during switching. Each output will have a disabled channel. The feedback and output network connected on the output slightly attenuates the signal going out onto the 75Ω cable. The gain and output matching resistors (82.5Ω) have been slightly increased to get a signal gain of +1 to the matched load and provide a 75Ω output impedance to the cable. The section on Disable Operation shows the turn-on and turn-off switching glitches, using a grounded input for the single channel, is typically less than ±50mV. Where two outputs are switched (shown in Figure 4), the output line is always under the control of one amplifier or the other due to the "make-before-break" disable timing. In this case, the switching glitches for 0V inputs drops to < 20mV.

VIDEO DAC RECONSTRUCTION FILTER

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as fixed gain block inside a passive RC circuit network. Their relatively constant bandwidth versus gain, provides low interaction between the actual filter poles and the required gain for the amplifier. Figure 5 shows an example of a video DAC reconstruction filter.

The delay-equalized filter in Figure 5 compensates for the DAC's sin(x)/x response, and minimizes aliasing artifacts. It is designed for single +5V operation, with a 13.5Msps DAC sampling rate, and a 5.5MHz cutoff frequency.

The first op amp buffers the video DAC output and the first filter section from each other. This first filter section provides group delay equalization. The second and third filter sections provide a 6th-order lowpass filter response that also compensates for the DAC's sin(x)/x response.

The filter response can be seen in Figure 6.

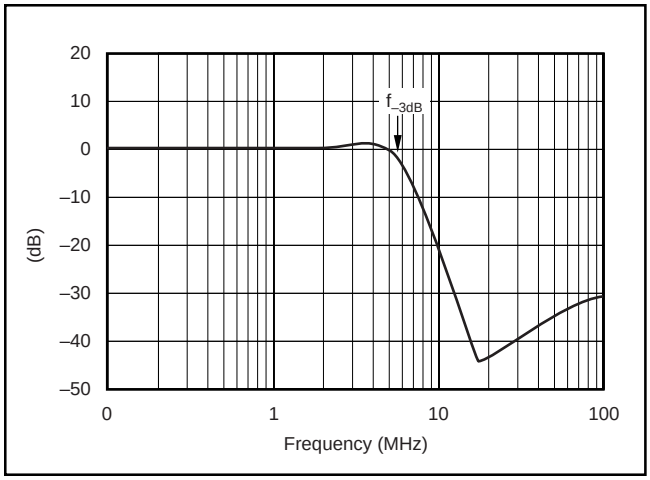


FIGURE 6. DAC Reconstruction Filter Response.

HIGH POWER xDSL LINE DRIVER

Emerging broadband access technologies are making significant demands on the output stage drivers. Some of the higher frequency versions, particularly in VDSL, require passive bandpass filters to spectrally isolate the upstream from downstream frequency bands. Figure 7 shows one possible implementation of this using single-ended filters and giving differential push/pull drive into a transformer. The DAC output from the analog front end (AFE) typically requires isolation from the complex filter impedance. The first stage provides a tunable gain (using R_G) with a fixed

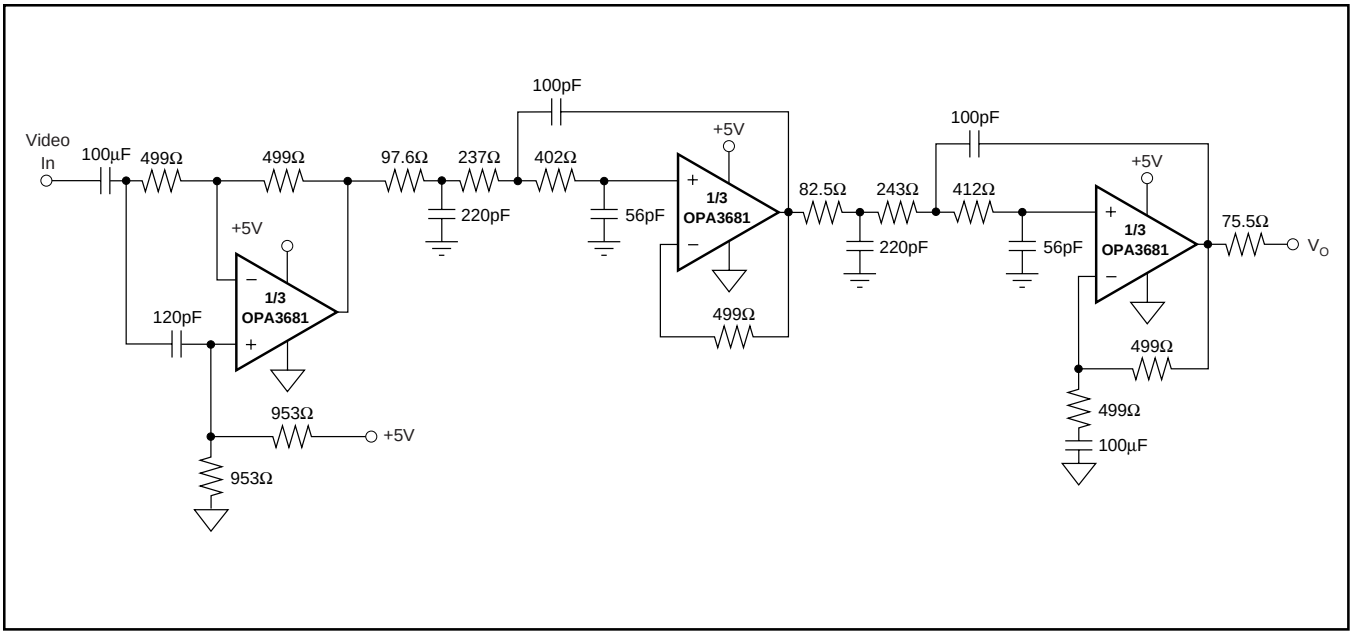


FIGURE 5. Filter Schematic.

termination for the DAC, R_T. It is very useful from a distortion standpoint to scale the characteristic impedance up for the filter. This reduces the loading at the first stage amplifier output, typically improving 3rd-order terms directly, as well as some improvement in 2nd-order terms. Figure 7 assumes a 100Ω characteristic impedance for the filter. The filter is driven from a 100Ω source resistor into a 100Ω load that is formed by the input gain resistor of the inverting amplifier channel. The other non-inverting input is isolated by a series 50Ω resistor—principally to isolate that input from the out-of-band source impedance of the filter. In this example, the output stage is set up for a differential gain of 8. The total gain from the output of the bandpass filter to the line will be 4 • n, where n is the turns ratio used in the transformer. Very broad bandwidths at high power levels are possible using the OPA3681 in the circuit of Figure 7. Recognize also, that the output is in fact bandlimited by the filter. Very high dynamic range is possible inside the filter bandwidth due to the significant performance margin provided by the OPA3681.

WIDEBAND DIFFERENTIAL AMPLIFIER

The differential amplifier (three amplifier instrumentation topology) on the front page of this data sheet shows a common application applied to this triple current feedback op amp. The two input stage amplifiers are configured for a relatively high differential gain of 10. Lowering the feedback resistor values in this input stage provides > 120MHz bandwidth, even at this high gain setting. The signal is applied to the high impedance, non-inverting inputs at the input stage. The differential gain is set by $(1 + 2R_F/R_G) = 10$ using the values shown on the front page. The third amplifier performs the differential-to-single-ended conversion in a standard single op amp differential stage. This differential stage, built using the 3rd wideband current-feedback op amp, in the OPA3681 will give lower CMRR at DC than using a voltage feedback part, but higher CMRR at higher frequencies. Measured performance, with no resistor value tuning, gave approximately 75dB at DC and > 55dB CMRR (input referred) through 10MHz. To maintain good distortion performance for the input stage amplifiers, the loading at each output has been matched while achieving the gain of 1 and differential characteristic of the output stage. To improve DC CMRR, tune the resistor to ground at the non-inverting input of the output stage amplifier.

WIDEBAND PROGRAMMABLE GAIN

By tying all three inputs together from a single source, and all three outputs together to drive a common load, a very wideband, programmable gain function may be implemented. Figure 8 shows an example of this application where the three channels have been set up for gains of 2, 4, and 8 to their output pins. When driving a doubly-terminated 50Ω load, this gives a user-selectable gain of 1, 2 and 4 to the matched load. The feedback resistor value has been optimized for maximum flat bandwidth in each channel. This will give an almost constant > 200MHz bandwidth at any of the three gain settings. The desired gain is selected by using the disable control lines to choose one of the three possible amplifiers as the active channel. An additional 10Ω resistor was included inside the loop on each output stage to limit output stage currents if more than one output is on during gain select transition. This will reduce the maximum available output voltage swing into the 100Ω total load shown in Figure 8 to approximately ±3.2V, but will provide surge current protection during channel switching. The 20Ω series resistors on each non-inverting input serves to isolate the input parasitic capacitance from the source.

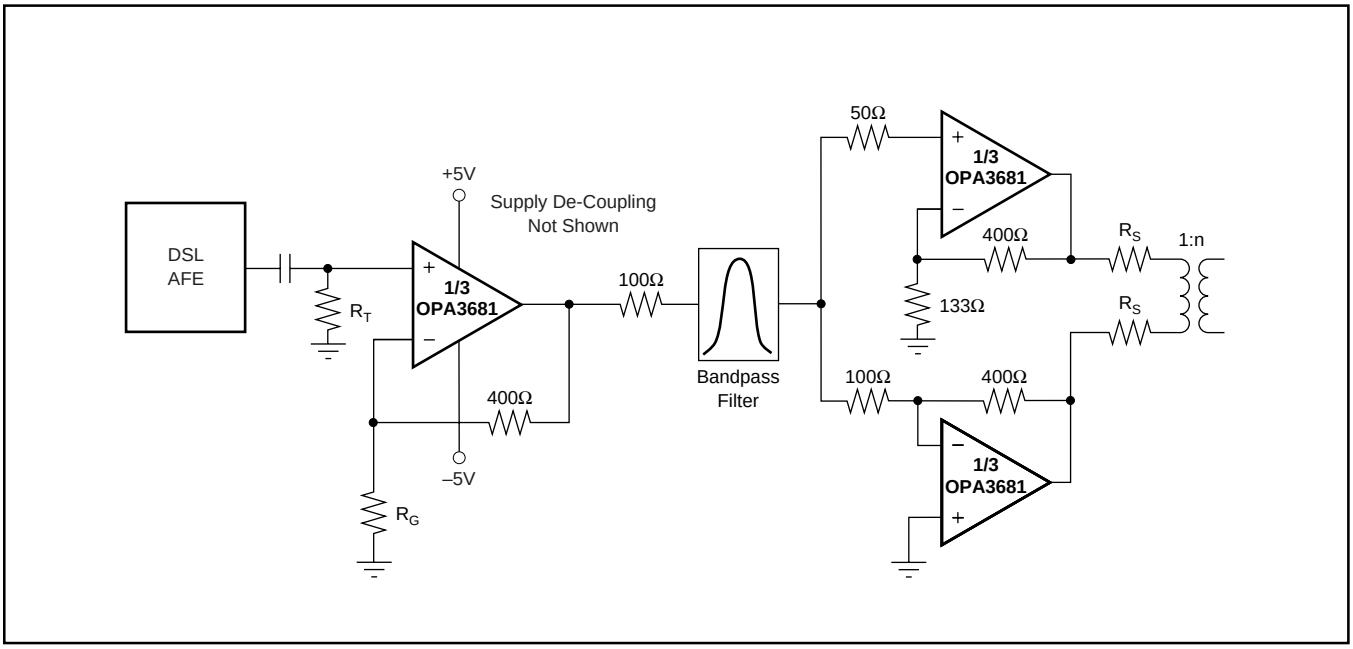


FIGURE 7. Single-to-Differential xDSL Line Driver.

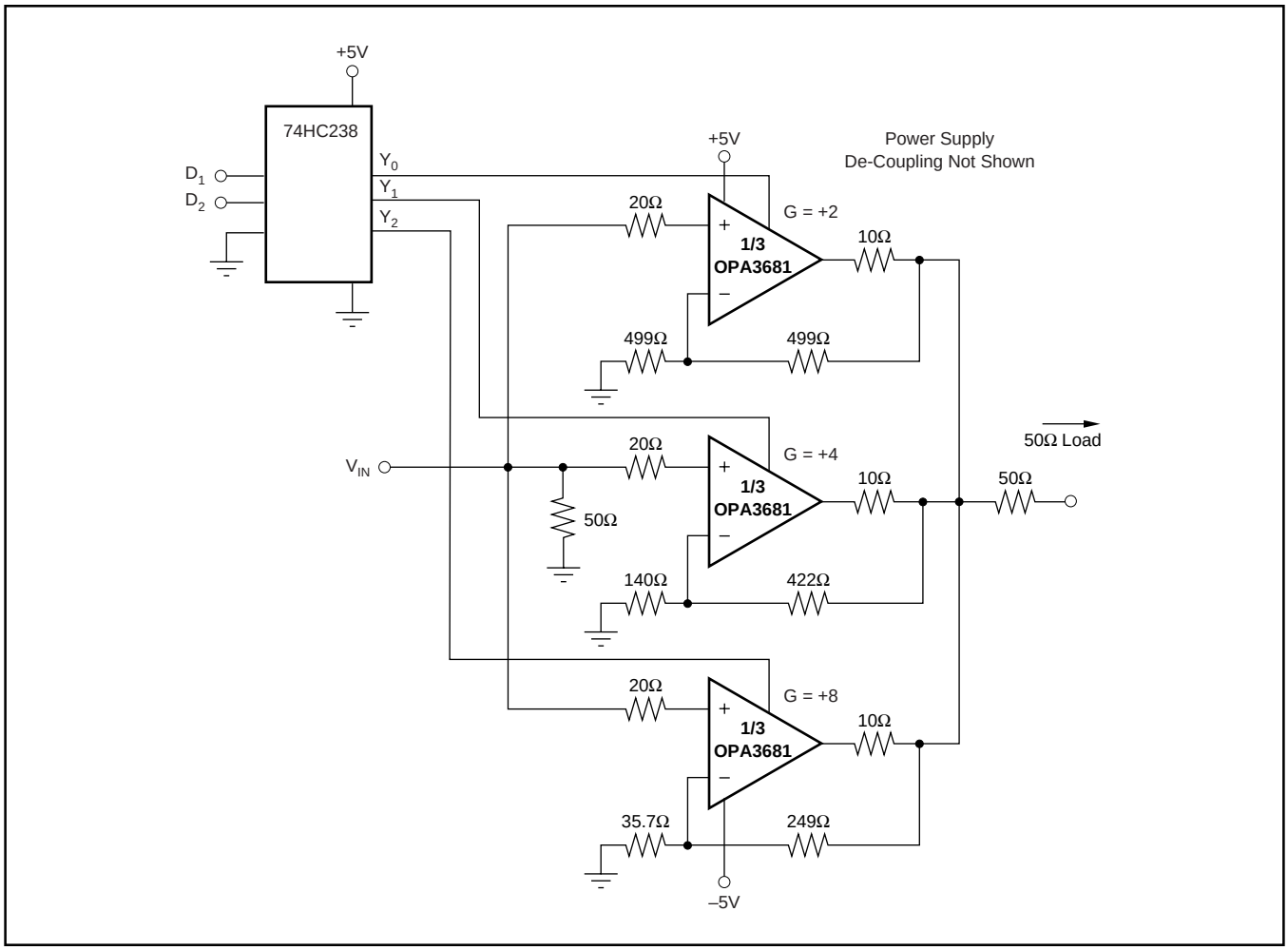


FIGURE 8. Wideband Programmable Gain.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp like the OPA3681 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This is shown in the Typical Performance Curves; the small signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor has been changed for each gain setting. The resistor "values" on the inverting side of the circuit for a current feedback op amp can be treated as frequency response compensation elements while their "ratios" set the signal gain. Figure 9 shows the small-signal frequency response analysis circuit for the OPA3681.

The key elements of this current-feedback op amp model are:

$\alpha \rightarrow$ Buffer gain from the non-inverting input to the inverting input

$R_I \rightarrow$ Buffer output impedance

$i_{ERR} \rightarrow$ Feedback error current signal

$Z(s) \rightarrow$ Frequency dependent open loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For a buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log (1- \alpha)$ dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA3681 is typically 42Ω.

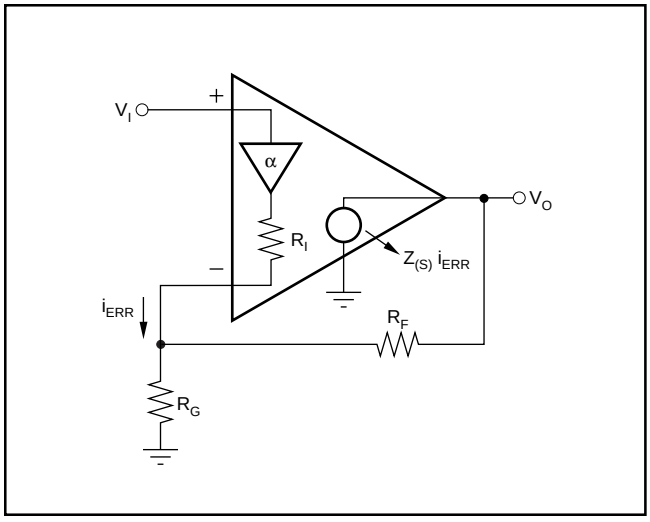


FIGURE 9. Current Feedback Transfer Function Analysis Circuit.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Performance Curves show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 9 gives Equation 1:

Eq. 1

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F + R_I\, NG}{Z_{(S)}}}$$

$$\left[NG \equiv \left(1+\frac{R_F}{R_G}\right)\right]$$

This is written in a loop gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) were infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop gain equation:

Eq. 2

$$\frac{Z_{(S)}}{R_F + R_I\, NG} = \text{Loop Gain}$$

If 20 • log (R_F + NG • R_I) were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 2 at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response, given by Equation 1, will start to roll off and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA3681 is internally compensated to give a maximally flat frequency response for R_F = 499Ω at NG = 2 on ±5V supplies. Evaluating the denominator of Equation 2 (which is the feedback transimpedance) gives an optimal target of 589Ω. As the signal gain changes, the contribution of the NG • R_I term in the feedback transimpedance will change, but the total can be held constant by adjusting R_F. Equation 3 gives an approximate equation for optimum R_F over signal gain:

Eq. 3

$$R_F = 589\Omega - NG\, R_I$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values will load both the buffer stage at the input and the output stage if R_F gets too low—actually decreasing the bandwidth. Figure 10 shows the recommended R_F vs NG for both ±5V and a single +5V operation. The values shown in Figure 10 give a good starting point for design where bandwidth optimization is desired.

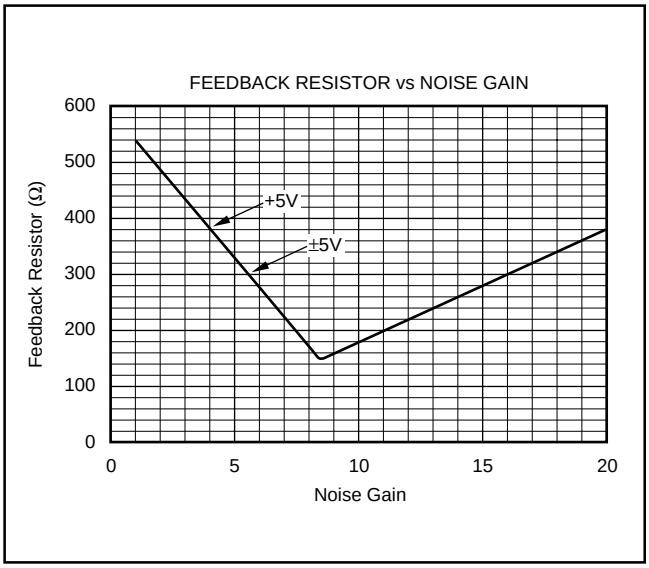


FIGURE 10. Recommended Feedback Resistor vs Noise Gain.

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction will increase the feedback impedance (denominator of Equation 2), decreasing the bandwidth. The internal buffer output impedance for the OPA3681 is slightly influenced by the source impedance looking out of the non-inverting input terminal. High source resistors will have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the non-inverting input through high valued resistors, the decoupling capacitor is essential for power supply ripple rejection, non-inverting input noise current shunting, and to minimize the high frequency value for R_I in Figure 9.

INVERTING AMPLIFIER OPERATION

Since the OPA3681 is a general purpose, wideband current-feedback op amp, most of the familiar op amp application circuits are available to the designer. Those triple op amp applications that require considerable flexibility in the feedback element (e.g., integrators, transimpedance, some filters) should consider the unity gain stable voltage-feedback OPA2680, since the feedback resistor is the compensation element for a current feedback op amp. Wideband inverting operation (especially summing) is particularly suited to the OPA3681. Figure 11 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

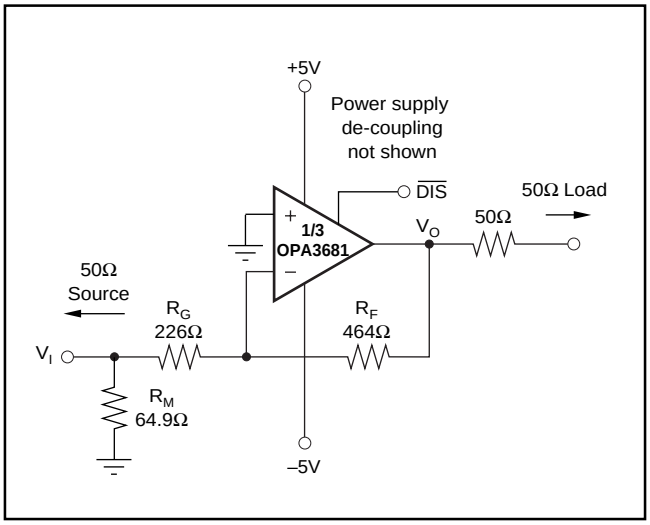


FIGURE 11. Inverting Gain of –2 with Impedance Matching.

In the inverting configuration, two key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace or other transmission line conductor), it is normally necessary to add an additional matching resistor to ground. R_G by itself is normally not set to the required input impedance since its value, along with the desired gain, will determine a R_F which may be non-optimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and will have slight effect on the bandwidth through Equation 1. The values shown in Figure 11 have accounted for this by slightly decreasing R_F (from Figure 1) to re-optimize the bandwidth for the noise gain of Figure 11 (NG = 2.82) In the example of Figure 11, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 64Ω = 28.1Ω. This impedance is added in series with R_G for calculating the noise gain—which gives NG = 2.82. This value, along with the R_F of Figure 10 and the inverting input impedance of 45Ω, are inserted into Equation 3 to get a feedback transimpedance nearly equal to the 589Ω optimum value.

Note that the non-inverting input in this bipolar supply inverting application is connected directly to ground. It is often suggested that an additional resistor be connected to ground on the non-inverting input to achieve bias current error cancellation at the output. The input bias currents for a current feedback op amp are not generally matched in either magnitude or polarity. Connecting a resistor to ground on the non-inverting input of the OPA3681 in the circuit of Figure 11 will actually provide additional gain for that input's bias and noise currents, but will not decrease the output DC error since the input bias currents are not matched.

OUTPUT CURRENT AND VOLTAGE

The OPA3681 provides output voltage and current capabilities that are unsurpassed in a low cost dual monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; the guaranteed swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is guaranteed to deliver more than ±135mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the "Output Voltage and Current Limitations" plot in the Typical Performance Curves. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA3681's output drive capabilities, noting that the graph is bounded by a "Safe Operating Area" of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA3681 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the Specifications Table.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the guaranteed tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}'s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. **However, shorting the output pin directly to the adjacent positive power supply pins will, in most cases, destroy the amplifier.** If additional short-circuit protection is required, consider a small series resistor in the power supply leads. Under heavy output loads, this will reduce the available output voltage swing. A 5Ω series resistor in each power supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.5V for up to 100mA desired load currents. Always place the 0.1µF power supply decoupling capacitors after these supply current-limiting resistors directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter—including additional external capacitance which may be recommended to improve A/D linearity. A high speed, high open-loop gain amplifier like the OPA3681 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Performance Curves show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3681. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA3681 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA3681 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic will dominate the distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the non-inverting configuration (Figure 1), this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Performance Curves show the 2nd harmonic increasing at a little less than the expected 2x rate while the 3rd harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd harmonic decreases less than the expected 6dB while the difference between it and the 3rd decreases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd- order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Performance Curves show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (i.e., 2Vp-p for each tone at the load, which requires 8Vp-p for the overall 2-tone envelope at the output pin), the Typical Performance Curves show 62dBc difference between the test tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

Wideband current feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA3681 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (15pA/$\sqrt{\text{Hz}}$) is significantly lower than earlier solutions while the input voltage noise (2.2nV/$\sqrt{\text{Hz}}$) is lower than most unity gain stable, wideband, voltage feedback op amps. This low input voltage noise was achieved at the price of higher non-inverting input current noise (12pA/$\sqrt{\text{Hz}}$). As long as the AC source impedance looking out of the non-inverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 12 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{\text{Hz}}$ or pA/$\sqrt{\text{Hz}}$.

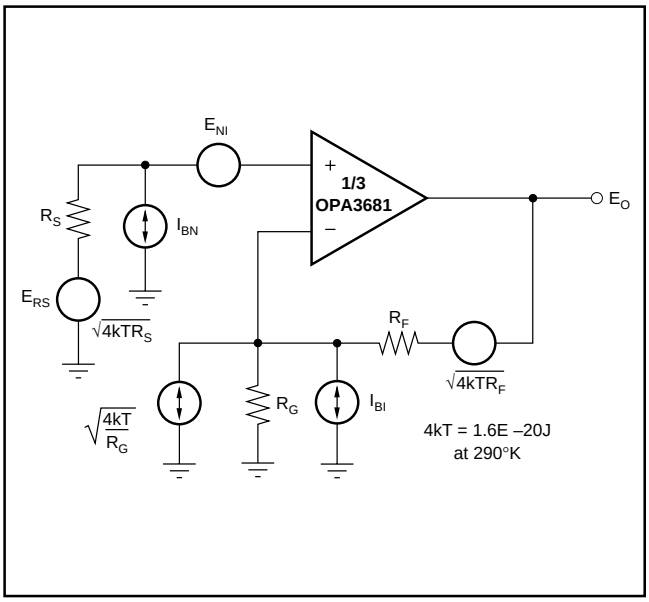


FIGURE 12. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 12.

Eq. 4

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = $(1+R_F/R_G)$) will give the equivalent input referred spot noise voltage at the non-inverting input as shown in Equation 5.

Eq. 5

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA3681 circuit and component values shown in Figure 1 will give a total output spot noise voltage of 8.4nV/$\sqrt{\text{Hz}}$ and a total equivalent input spot noise voltage of 4.2nV/$\sqrt{\text{Hz}}$. This total input-referred spot noise voltage is higher than the 2.2nV/$\sqrt{\text{Hz}}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high gain configurations (as suggested previously), the total input-referred voltage noise given by Equation 5 will approach just the 2.2nV/$\sqrt{\text{Hz}}$ of the op amp itself. For example, going to a gain of +10 using R_F = 182Ω will give a total input referred noise of 2.4nV/$\sqrt{\text{Hz}}$.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA3681 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Specifications Table shows an input offset voltage comparable to high-speed, voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm (NG \cdot V_{OS(MAX)}) + (I_{BN} \cdot R_S/2 \cdot NG) \pm (I_{BI} \cdot R_F)$

where NG = non-inverting signal gain

$= \pm (2 \cdot 5.0\text{mV}) + (55\mu\text{A} \cdot 25\Omega \cdot 2) \pm (499\Omega \cdot 40\mu\text{A})$

$= \pm 10\text{mV} + 2.75\text{mV} \pm 20\text{mV}$

$= -27.25\text{mV} \rightarrow +32.75\text{mV}$

DISABLE OPERATION

The OPA3681 provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{\text{DIS}}$ control pin is left unconnected, the OPA3681 will operate normally. To disable, the control pin must be asserted low. Figure 13 shows a simplified internal circuit for the disable control feature.

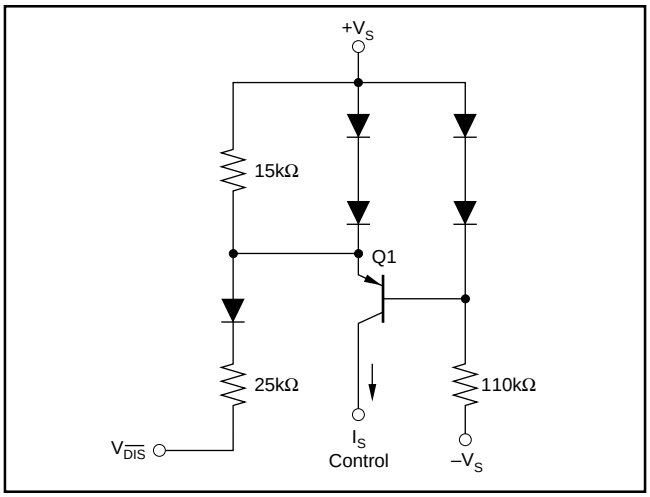


FIGURE 13. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{\text{DIS}}}$ is pulled low, additional current is pulled through the 15kΩ resistor eventually turning on these two diodes (≈ 100μA). At this point, any further current pulled out of $V_{\overline{\text{DIS}}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately zero volts. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode is that only required to operate the circuit of Figure 13. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high impedance state. If the OPA3681 is operating in a gain of +1, this will show a very high impedance (4pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

One key parameter in disable operation is the output glitch when switching in and out of the disable mode. Figure 14 shows these glitches for the circuit of Figure 1 with the input signal set to zero volts. The glitch waveform at the output pin is plotted along with the $\overline{\text{DIS}}$ pin voltage.

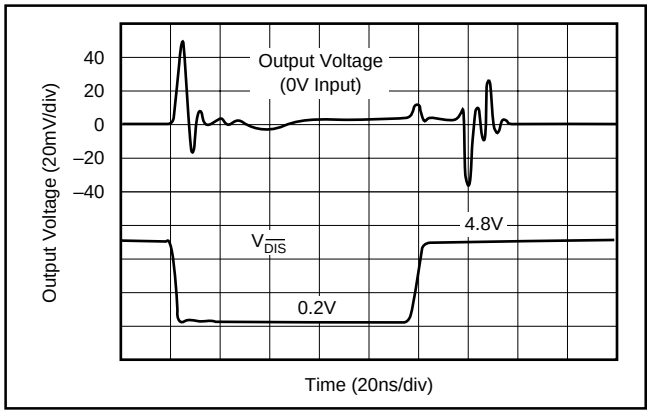


FIGURE 14. Disable/Enable Glitch.

The transition edge rate (dv/dt) of the $\overline{DIS}$ control line will influence this glitch. For the plot of Figure 14, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate may be achieved by adding a simple RC filter into the $V_{\overline{DIS}}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 2kΩ series resistor between the logic gate and the $V_{\overline{DIS}}$ input pin will provide adequate bandlimiting using just the parasitic input capacitance on the $V_{\overline{DIS}}$ pin while still ensuring adequate logic level swing.

THERMAL ANALYSIS

Due to the high output power capability of the OPA3681, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C. Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3681 SO-16 (in the circuit of Figure 1), operating at the maximum specified ambient temperature of +85°C with all three outputs driving a grounded 20Ω load to +2.5V:

$P_D = 10V \bullet 19.2mA + 3 \bullet [5^2/(4 \bullet (20\Omega \parallel 998\Omega))] = 1.15W$

Maximum $T_J = +85°C + (1.15 \bullet 100°C/W) = 200°C$

This absolute worst-case condition exceeds specified maximum junction temperature. Normally this extreme case will not be encountered. Careful attention to internal power dissipation is required and perhaps airflow considered under extreme conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA3681 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply de-coupling capacitor across the two power supplies (for bipolar operation) will improve 2nd harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA3681. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the bandwidth, while decreasing it will give a more peaked frequency response. The 499Ω feedback resistor used in the typical performance specifications at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 549Ω feedback resistor, rather than a direct short, is recommended for the unity gain follower application. A current feedback op amp requires a feedback resistor even in the unity gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA3681 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the Distortion vs Load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA3681 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA3681 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high speed part like the OPA3681 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3681 onto the board.

INPUT AND ESD PROTECTION

The OPA3681 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 15.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA3681), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

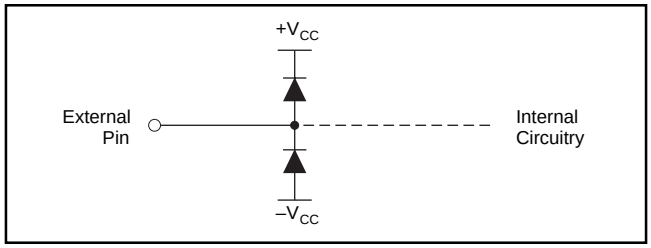


FIGURE 15. Internal ESD Protection.

DESIGN-IN TOOLS

APPLICATIONS SUPPORT

The Texas Instruments Applications Department is available for design assistance at phone number 1-800-548-6132 (US/Canada only). The TI web site (www.ti.com) has the latest data sheets and other design aids.

DEMONSTRATION BOARDS

A PC board will be available to assist in the initial evaluation of circuit performance of the OPA3681. This is available as an unpopulated PCB with descriptive documentation. See the demonstration board literature for more information. The summary information for this board is shown below:

PRODUCT	PACKAGE	DEMONSTRATION BOARD	LITERATURE REQUEST NUMBER
OPA3681E	SSOP-16	DEM-OPA368xE	MKT-354
OPA3681U	SO-16	DEM-OPA368xU	MKT-364

Check the TI web site for availability of these boards.

SPICE MODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for high speed active devices, like the OPA3681, where parasitic capacitance and inductance can have a major effect on frequency response.

SPICE models will be available through the TI web page or on a disk (call our Applications Department). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or differential gain and phase characteristics. These models do not distinguish between the AC performance of different package types.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265