Integrated Device Technology, Inc.

RISC CPU PROCESSOR

PRELIMINARY
IDT 79R2000A

T-49-17-32

FEATURES:

- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-chip Cache Control—The R2000A provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 64 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64 entry Transition Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space.
- Coprocessor Interface—The R2000A generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers available include: C, FORTRAN, Pascal, PL/1, COBOL, Ada
- UNIX™ System V.3 and BSD 4.3 operating systems supported.
- High-speed CEMOS™ technology
- Pin, function and software compatible with the MIPS Computer Systems R2000A RISC CPU.
- 12.5MHz or 16.7MHz clock rate yields 10 to 13 MIPS sustained throughput.
- Military product compliant to MIL-STD -883, Class B

DESCRIPTION:

Please see the 79R3000 data sheet for complete description. The R3000 is a superset of the R2000A and is available in 16.7, 20, and 25MHz clock rates. For the differences between the R2000A and R3000 please see the "R3000 Family Hardware User's Manual" or the R3000 data sheet section entitled "Backward Compatibility with 79R2000A".

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UNIX is a registered trademark of AT&T.

PIN CONFIGURATION

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	CpCond 2	CpCond 3	Intr* 2	Intr* 5	Wr Busy*	Reset*	VCC10
B	AdrLo 3	reser-ved2	AdrLo 7	AdrLo 9	AdrLo 12	reser-ved3	AdrLo 13	CpCond 1	Intr* 1	Intr* 3	Cp Busy*	Bus Error*	reser-ved4	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	Gnd13	Gnd12	VCC11	Intr* 0	Intr* 4	Rd Busy	Gnd11	Tag13	TagP0	Tag18
D	Data1	AdrLo 2	Gnd0										Tag14	Tag17	Tag19
E	Data P0	Data0	AdrLo 1										Tag16	Tag20	VCC9
F	VCC0	Data7	Data2										Gnd10	Tag21	Tag23
G	Data4	Data3	Gnd1										Gnd9	Tag22	TagP1
H	Data6	Data5	Data8										VCC8	Tag25	Tag24
J	Data 10	Data P1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	Gnd2										Gnd8	Tag P2	Tag27
L	VCC1	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	Data P2										Gnd7	Acc Typ1	VCC7
N	Data 14	Data 18	Data 19	Gnd3	Data 24	Data P3	VCC3	VCC4	Gnd5	Gnd6	DRd	MemWr*	MemRd*	Run*	TagV
P	Data 23	Data 20	reser-ved0	Data 22	Data 26	Data 27	reser-ved1	Data 30	Clk2x Sys	Clk2x Rd	Dclk*	IRd	IWr	Cp Sync*	Acc Typ0
Q	VCC2	Data 21	Data 25	Data 31	Data 28	Gnd4	Data 29	Exc*	Clk2x Phi	Clk2x Smp	Sys Out*	VCC5	IClk*	DWr	VCC6

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ABSOLUTE MAXIMUM RATINGS (1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage (2)	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} + 0.5 volts.
3. Not more than one output at a time should be shorted. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

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DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.5	–	0.5	V
V_{OHT}	Output HIGH Voltage(4)	V_{CC} = Min., I_{OH} = -8mA	2.4	–	2.4	–	V
V_{OLT}	Output LOW Voltage(4)	V_{CC} = Min., I_{OL} = 8mA	–	0.8	–	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 5)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	500	–	575	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.5	–	0.5	V
V_{OHT}	Output HIGH Voltage(4)	V_{CC} = Min., I_{OH} = -8mA	2.4	–	2.4	–	V
V_{OLT}	Output LOW Voltage(4)	V_{CC} = Min., I_{OL} = 8mA	–	0.8	–	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 5)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	575	–	675	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2sRd, Clk2xPhi, CpBusy, and RESET*.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals.
5. V_{IH} should not be held above V_{CC} + 0.5 Volts.

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AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = +5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
CLOCK							
TCkHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCkLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCkP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		11	tcyc/4	9	tcyc/4	ns
RUN OPERATION							
TDEn	Data Enable[3]		–	-2.5	–	-2	ns
TDDis	Data Disable[3]		–	-1.5	–	-1	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TWrDly	Write Delay	Load = 25pF	–	7.5	–	5	ns
TDS	Data Set-up		11.5	–	9	–	ns
TRSDS	Reset Pin Set-up		18	–	15	–	ns
TDH	Data Hold		-2.5	–	-2.5	–	ns
TCBS	CpBusy Set-up		15	–	13	–	ns
TCBH	CpBusy Hold		-2.5	–	-2.5	–	ns
TAcTy	Access Type (1:0)	Load = 25pF	–	10	–	7	ns
TAT2	Access Type (2)	Load = 25pF	–	20	–	17	ns
TMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TExe	Exception	Load = 25pF	–	10	–	7	ns
STALL OPERATION							
TSAVal	Address Valid	Load = 25pF	–	38	–	30	ns
TSAcTy	Access Type	Load = 25pF	–	35	–	27	ns
TMRdI	Memory Read Initiate	Load = 25pF	–	35	–	27	ns
TMRdT	Memory Read Terminate	Load = 25pF	–	10	–	7	ns
TSd	Run Terminate	Load = 25pF	–	25	–	17	ns
TRun	Run Initiate	Load = 25pF	–	15	–	12	ns
TSMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TSEx	Exception Valid	Load = 25pF	–	28	–	20	ns
RESET INITIALIZATION							
Trst	Reset Pulse Width		6	–	6	–	TckP
TrstPLL	Reset timing, Phase-lock on[5]		3000	–	3000	–	TckP
Trstop	Reset timing, Phase-lock off[5]		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual".
5. Those parameters apply only when the 79R2010A Floating Point Compression is connected to the CPU.

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AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
CLOCK							
TCkHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCkLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCkP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		11	tcyc/4	9	tcyc/4	ns
RUN OPERATION							
TDEn	Data Enable[3]		–	-2.5	–	-2	ns
TDDis	Data Disable[3]		–	-1.5	–	-1	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TWrDly	Write Delay	Load = 25pF	–	7.5	–	5	ns
TDS	Data Set-up		11.5	–	9	–	ns
TRSDS	Reset Pin Set-up		18	–	15	–	ns
TDH	Data Hold		-4	–	-4	–	ns
TCBS	CpBusy Set-up		15	–	13	–	ns
TCBH	CpBusy Hold		-4	–	-4	–	ns
TAcTy	Access Type (1:0)	Load = 25pF	–	10	–	7	ns
TAT2	Access Type (2)	Load = 25pF	–	20	–	17	ns
TMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TExe	Exception	Load = 25pF	–	10	–	7	ns
STALL OPERATION							
TSAVal	Address Valid	Load = 25pF	–	38	–	30	ns
TSAcTy	Access Type	Load = 25pF	–	35	–	27	ns
TMRdI	Memory Read Initiate	Load = 25pF	–	35	–	27	ns
TMRdT	Memory Read Terminate	Load = 25pF	–	10	–	7	ns
TSd	Run Terminate	Load = 25pF	–	25	–	17	ns
TRun	Run Initiate	Load = 25pF	–	15	–	12	ns
TSMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TSEx	Exception Valid	Load = 25pF	–	28	–	20	ns
RESET INITIALIZATION							
Trst	Reset Pulse Width		6	–	6	–	TckP
TrstPLL	Reset timing, Phase-lock on[5]		3000	–	3000	–	TckP
Trst	Reset timing, Phase-lock off[5]		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual".
5. Those parameters apply only when the 79R2010A Floating Point Compression is connected to the CPU.

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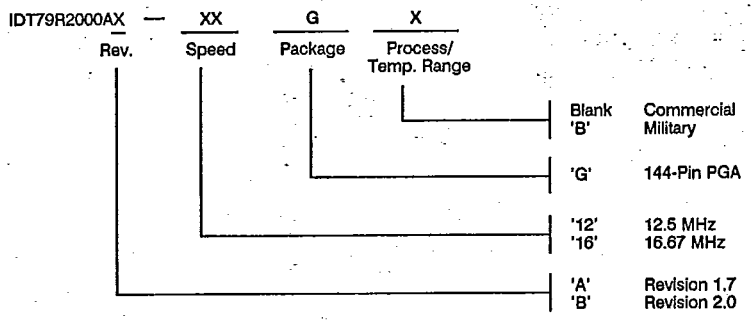
ORDERING INFORMATION



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