16Mx64 bits
PC100 SDRAM SO DIMM

based on 16Mx16 SDRAM with LVTTL, 4 banks & 8K Refresh

HYM72V16M656AT6 Series

DESCRIPTION

The HYM72V16M656AT6 -Series are high speed 3.3-Volt Synchronous DRAM Modules composed of four 16Mx16 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit EEPROM on a 144-pin Zig Zag Dual pin glass-epoxy printed circuit board. Three 0.1uF decoupling capacitors per each SDRAM are mounted on the module.

The HYM72V16M656T6 -Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 128M bytes memory. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- 1.00(31.75mm) PCB Height
- One Row of SDRAMs on SO DIMM
- 144-Pin SO DIMM
- Serial Presence Detect with Serial E^2PROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 8192 refresh cycles every 64ms
- All inputs and outputs referenced to positive edge of system clock
- Internal four banks operation
- Programmable Burst Length and Burst Type

  - 1,2,4,8 and Full page for Sequential Burst
  - 1,2,4 and 8 for Interleave Burst
- Programmable /CAS latency ; 2,3 clocks
- Data mask function by DQM

ORDERING INFORMATION

Part No.	Clock Frequency	Internal Bank	Ref.	Power	SDRAM Package	Plating
HYM72V16M656AT6-8	125MHz	4 Banks	8K	Normal	TSOP-II	Gold
HYM72V16M656AT6-P	100MHz					
HYM72V16M656AT6-S	100MHz					
HYM72V16M656ALT6-8	125MHz			Low Power		
HYM72V16M656ALT6-P	100MHz					
HYM72V16M656ALT6-S	100MHz					

PIN DESCRIPTION

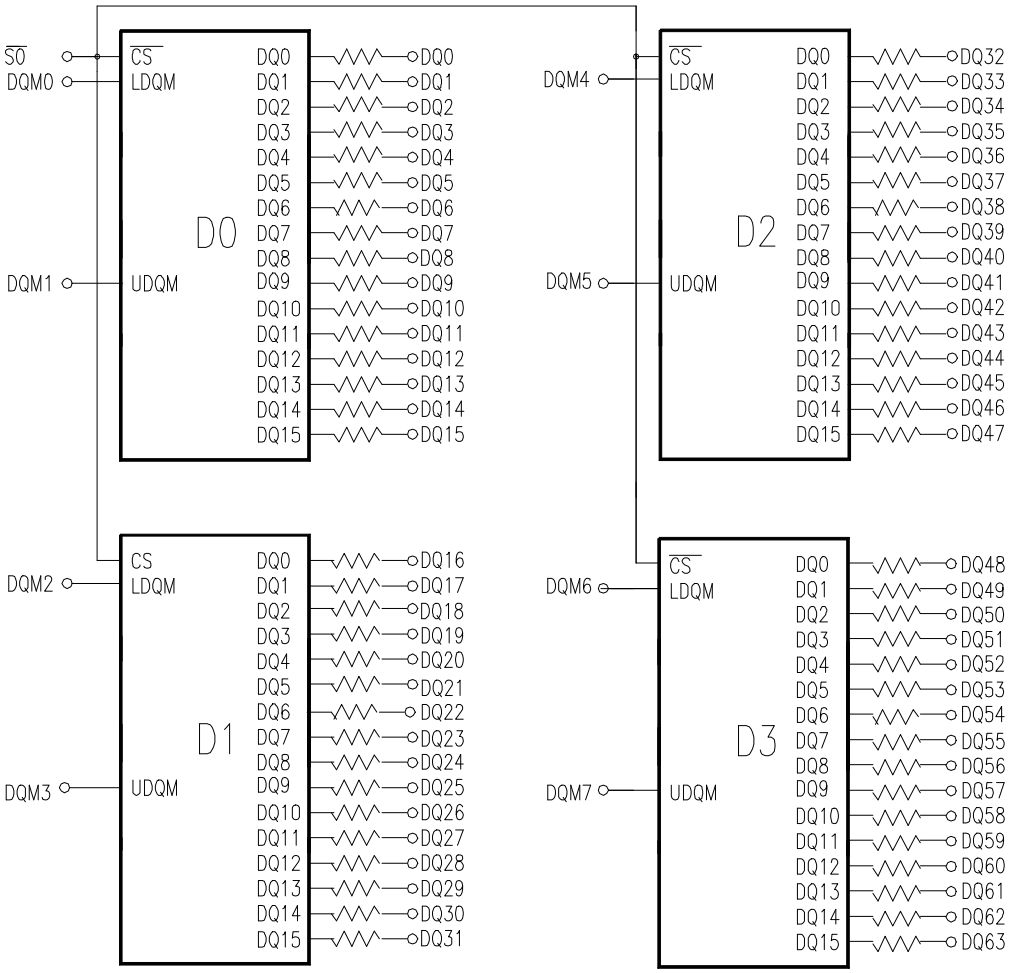
PIN	PIN NAME	DESCRIPTION
CK0, CK1	Clock Inputs	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
/S0	Chip Select	Enables or disables all inputs except CK, CKE and DQM
BA0, BA1	SDRAM Bank Address	Selects bank to be activated during /RAS activity Selects bank to be read/written during /CAS activity
A0 ~ A12	Address	Row Address : RA0 ~ RA12, Column Address : CA0 ~ CA8 Auto-precharge flag : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation Refer function truth table for details
DQM0~DQM7	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ63	Data Input/Output	Multiplexed data input / output pin
VCC	Power Supply (3.3V)	Power supply for internal circuits and input buffers
VSS	Ground	Ground
SCL	SPD Clock Input	Serial Presence Detect Clock input
SDA	SPD Data Input/Output	Serial Presence Detect Data input/output
SA0~2	SPD Address Input	Serial Presence Detect Address Input
WP	Write Protect for SPD	Write Protect for Serial Presence Detect on DIMM
NC	No Connection	No connection

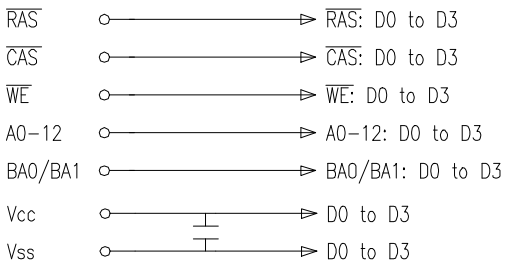
PIN ASSIGNMENTS

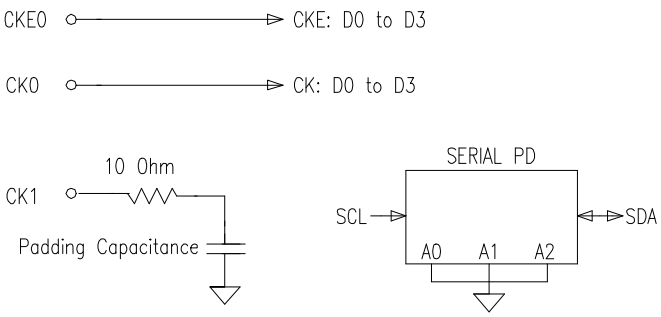
FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VSS	2	VSS	71	NC	72	NC
3	DQ0	4	DQ32	73	NC	74	*CK1
5	DQ1	6	DQ33	75	VSS	76	VSS
7	DQ2	8	DQ34	77	NC	78	NC
9	DQ3	10	DQ35	79	NC	80	NC
11	VCC	12	VCC	81	VCC	82	VCC
13	DQ4	14	DQ36	83	DQ16	84	DQ48
15	DQ5	16	DQ37	85	DQ17	86	DQ49
17	DQ6	18	DQ38	87	DQ18	88	DQ50
19	DQ7	20	DQ39	89	DQ19	90	DQ51
21	VSS	22	VSS	91	VSS	92	VSS
23	DQM0	24	DQM4	93	DQ20	94	DQ52
25	DQM1	26	DQM5	95	DQ21	96	DQ53
27	VCC	28	VCC	97	DQ22	98	DQ54
29	A0	30	A3	99	DQ23	100	DQ55
31	A1	32	A4	101	VCC	102	VCC
33	A2	34	A5	103	A6	104	A7
35	VSS	36	VSS	105	A8	106	BA0
37	DQ8	38	DQ40	107	VSS	108	VSS
39	DQ9	40	DQ41	109	A9	110	BA1
41	DQ10	42	DQ42	111	A10/AP	112	A11
43	DQ11	44	DQ43	113	VCC	114	VCC
45	VCC	46	VCC	115	DQM2	116	DQM6
47	DQ12	48	DQ44	117	DQM3	118	DQM7
49	DQ13	50	DQ45	119	VSS	120	VSS
51	DQ14	52	DQ46	121	DQ24	122	DQ56
53	DQ15	54	DQ47	123	DQ25	124	DQ57
55	VSS	56	VSS	125	DQ26	126	DQ58
57	NC	58	NC	127	DQ27	128	DQ59
59	NC	60	NC	129	VCC	130	VCC
Voltage Key				131	DQ28	132	DQ60
				133	DQ29	134	DQ61
61	CK0	62	CKE0	135	DQ30	136	DQ62
63	VCC	64	VCC	137	DQ31	138	DQ63
65	/RAS	66	/CAS	139	VSS	140	VSS
67	/WE	68	NC	141	SDA	142	SCL
69	/S0	70	A12	143	VCC	144	VCC

Note : * CK1 are connected with termination R/C (Refer to the Block Diagram)

BLOCK DIAGRAM







Note : 1. The serial resistor values of DQs are 10ohms
2. The padding capacitance of termination R/C for CK1 is 10pF

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION			VALUE			NOTE
		-8	-P	-S	-8	-P	-S	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes			80h			
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes			08h			
BYTE2	Fundamental Memory Type	SDRAM			04h			
BYTE3	# of Row Addresses on This Assembly	13			0Dh			1
BYTE4	# of Column Addresses on This Assembly	9			09h			
BYTE5	# of Module Banks on This Assembly	1 Bank			01h			
BYTE6	Data Width of This Assembly	64 Bits			40h			
BYTE7	Data Width of This Assembly (Continued)	-			00h			
BYTE8	Voltage Interface Standard of This Assembly	LVTTL			01h			
BYTE9	SDRAM Cycle Time @/CAS Latency=3	8ns	10ns	10ns	80h	A0h	A0h	
BYTE10	Access Time from Clock @/CAS Latency=3	6ns	6ns	6ns	60h	60h	60h	
BYTE11	DIMM Configuration Type	None			00h			
BYTE12	Refresh Rate/Type	7.8125us / Self Refresh Supported			82h			
BYTE13	Primary SDRAM Width	x16			10h			
BYTE14	Error Checking SDRAM Width	None			00h			
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD = 1 CLK			01h			
BYTE16	Burst Lenth Supported	1,2,4,8,Full Page			8Fh			2
BYTE17	# of Banks on Each SDRAM Device	4 Banks			04h			
BYTE18	SDRAM Device Attributes, /CAS Lataency	/CAS Latency=2,3			06h			
BYTE19	SDRAM Device Attributes, /CS Lataency	/CS Latency=0			01h			
BYTE20	SDRAM Device Attributes, /WE Lataency	/WE Latency=0			01h			
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered			00h			
BYTE22	SDRAM Device Attributes, General	+/- 10% voltage tolerence, Burst Read Single Bit Write, Precharge All, Auto Precharge, Early RAS Precharge			0Eh			
BYTE23	SDRAM Cycle Time @/CAS Latency=2	12ns	10ns	12ns	C0h	A0h	C0h	
BYTE24	Access Time from Clock @/CAS Latency=2	6ns	6ns	6ns	60h	60h	60h	
BYTE25	SDRAM Cycle Time @/CAS Latency=1	-	-	-	00h	00h	00h	
BYTE26	Access Time from Clock @/CAS Latency=1	-	-	-	00h	00h	00h	
BYTE27	Minimum Row Precharge Time (tRP)	20ns	20ns	20ns	14h	14h	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	20ns	20ns	20ns	14h	14h	14h	
BYTE30	Minimum /RAS Pulse Width (tRAS)	48ns	50ns	50ns	30h	32h	32h	
BYTE31	Module Bank Density	128MB			20h			
BYTE32	Command and Address Signal Input Setup Time	2ns	2ns	2ns	20h	20h	20h	
BYTE33	Command and Address Signal Input Hold Time	1ns	1ns	1ns	10h	10h	10h	
BYTE34	Data Signal Input Setup Time	2ns	2ns	2ns	20h	20h	20h	
BYTE35	Data Signal Input Hold Time	1ns	1ns	1ns	10h	10h	10h	
BYTE36 ~61	Superset Information (may be used in future)	-			00h			
BYTE62	SPD Revision	Intel SPD 1.2B			12h			3, 8
BYTE63	Checksum for Byte 0~62	-			07h	0Dh	2Dh	
BYTE64	Manufacturer JEDEC ID Code	Hynix JEDED ID			ADh			
BYTE65 ~71	....Manufacturer JEDEC ID Code	Unused			FFh			
BYTE72	Manufacturing Location	Hynix (Korea Area) HSA (United States Area) HSE (Europe Area) HSJ (Japan Area) Asia Area			0*h 1*h 2*h 3*h 4*h			10

Continued

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION			VALUE			NOTE
		-8	-P	-S	-8	-P	-S	
BYTE73	Manufacturer's Part Number (Component)	7 (SDRAM)			37h			4, 5
BYTE74	Manufacturer's Part Number (128Mb based)	2			32h			4, 5
BYTE75	Manufacturer's Part Number (Voltage Interface)	V (3.3V, LVTTL)			56h			4, 5
BYTE76	Manufacturer's Part Number (Memory Width)	1			38h			4, 5
BYTE77	.... Manufacturer's Part Number (Memory Width)	6			36h			4, 5
BYTE78	Manufacturer's Part Number (Module Type)	M (SO DIMM)			4Dh			4, 5
BYTE79	Manufacturer's Part Number (Data Width)	6			36h			4, 5
BYTE78	....Manufacturer's Part Number (Data Width)	5			35h			4, 5
BYTE79	Manufacturer's Part Number (Refresh, SDRAM Bank)	6 (8K Refresh, 4Banks)			36h			4, 5
BYTE80	Manufacturer's Part Number (Generation)	A			41h			4, 5
BYTE81	Manufacturer's Part Number (Package Type)	T			54h			4, 5
BYTE82	Manufacturer's Part Number (Component Configuration)	6 (x16 based)			36h			4, 5
BYTE83	Manufacturer's Part Number (Hyphent)	- (Hyphen)			2Dh			4, 5
BYTE84	Manufacturer's Part Number (Min. Cycle Time)	8	P	S	38h	50h	53h	4, 5
BYTE85 ~90	Manufacturer's Part Number	Blanks			20h			4, 5
BYTE91	Revision Code (for Component)	Process Code			-			4, 6
BYTE92	....Revision Code (for PCB)	Process Code			-			4, 6
BYTE93	Manufacturing Date	Work Week			-			3, 6
BYTE94	....Manufacturing Date	Year			-			3, 6
BYTE95 ~98	Assembly Serial Number	Serial Number			-			6
BYTE99 ~125	Manufacturer Specific Data (may be used in future)	None			00h			
BYTE126	System Frequency Support	100MHz			64h			7, 8
BYTE127	Intel Specification Details for 100MHz Support	Refer to Note7			A7h	A7h	A5h	7, 8
BYTE128 Note : ~256	Unused Storage Locations	-			00h			

1. The bank address is excluded
2. 1, 2, 4, 8 for Interleave Burst Type
3. BCD adopted
4. ASCII adopted
5. Basically Hynix writes Part No. except for HYM'in Byte 73~90 to use the limited 18 bytes from byte 73 to byte 90
6. Not fixed but dependent
7. CK0, CK2 connected to DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support
8. Refer to Intel SPD Specification 1.2B
9. In the case of L-Part, character L'will be added between byte 80 and byte 81

10, Refer to Hynix web site

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	4	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input Low voltage	VIL	-0.3	0	0.8	V	1,3

Note :
1.All voltages are referenced to VSS = 0V
2.VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

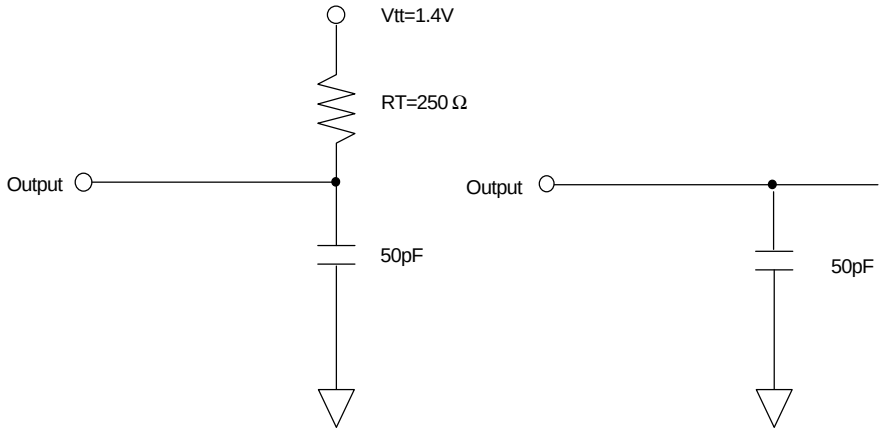
Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	-8/P/S		Unit
			Min	Max	
Input Capacitance	CK0, CK1	C_{I1}	15	30	pF
	CKE0	C_{I2}	20	35	pF
	/S0, /S1	C_{I3}	15	35	pF
	A0~12, BA0, BA1	C_{I4}	30	60	pF
	/RAS, /CAS, /WE	C_{I5}	30	60	pF
	DQM0~DQM7	C_{I6}	5	25	pF
Data Input / Output Capacitance	DQ0 ~ DQ63	$C_{I/O}$	5	20	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit

AC Output Load Circuit

DC CHARACTERISTICS I (TA=0 to 70°C, V_{DD}=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	I_{LI}	-4	4	uA	1
Output Leakage Current	I_{LO}	-1	1	uA	2
Output High Voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +4mA

Note :
1.V_{IN} = 0 to 3.6V, All other pins are not tested under V_{IN} =0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6

DC CHARACTERISTICS II

Parameter	Symbol	Test Condition		Speed			Unit	Note
				-8	-P	-S		
Operating Current	I_{DD1}	Burst length=1, One bank active $t_{RC} \geq t_{RC}$(min), I_{OL}=0mA		400	400	400	mA	1
Precharge Standby Current in Power Down Mode	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = min		4			mA	
	I_{DD2PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		4				
Precharge Standby Current in Non Power Down Mode	I_{DD2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = min Input signals are changed one time during 2clks. All other pins ≥ V_{DD}-0.2V or ≤ 0.2V		80			mA	
	I_{DD2NS}	CKE ≥ V_{IH}(min), t_{CK} = ∞ Input signals are stable.		16				
Active Standby Current in Power Down Mode	I_{DD3P}	CKE ≤ V_{IL}(max), t_{CK} = min		12			mA	
	I_{DD3PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		12				
Active Standby Current in Non Power Down Mode	I_{DD3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = min Input signals are changed one time during 2clks. All other pins ≥ V_{DD}-0.2V or ≤ 0.2V		100			mA	
	I_{DD3NS}	CKE ≥ V_{IH}(min), t_{CK} = ∞ Input signals are stable.		60				
Burst Mode Operating Current	I_{DD4}	$t_{CK} \geq t_{CK}$(min), I_{OL}=0mA All banks active	CL=3	480	400	400	mA	1
			CL=2	440	480	480		
Auto Refresh Current	I_{DD5}	$t_{RRC} \geq t_{RRC}$(min), All banks active		720			mA	2
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V		8			mA	3
				4			mA	4

Note :
1. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3. HYM72V16M656AT6-8/P/S
4. HYM72V16M656ALT6-/8/P/S

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	tCK3	8	1000	10	1000	10	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	10		10		12		ns	
Clock High Pulse Width		tCHW	3	-	3	-	3	-	ns	1
Clock Low Pulse Width		tCLW	3	-	3	-	3	-	ns	1
Access Time From Clock	$\overline{CAS}$ Latency = 3	tAC3	-	6	-	6	-	6	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	6	-	6	-	6	ns	
Data-Out Hold Time		tOH	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	1	-	1	-	1	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	1	-	ns	
CLK to Data Output in High-Z Time	$\overline{CAS}$ Latency = 3	tOHZ3	3	6	3	6	3	6	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	3	6	3	6	3	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns
If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter

2.Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

AC CHARACTERISTICS II

Parameter		Symbol	-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	68	-	70	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	20	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	48	100K	50	100K	50	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	20	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	16	-	20	-	20	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	4	-	3	-	3	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE

HYM72V16M656T6A(L)T-8

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM72V16M656A(L)T6-P

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM72V16M656A(L)T6-S

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/ AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

PACKAGE DEMENSION