HB66A2568A Series

262,144-Word × 8-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66A2568A is a high speed 256K × 8 Static RAM module, mounted 8 pieces of 256K bit SRAM (HM6207HJP) sealed in SOJ package. An outline of the HB66A2568A is 60-pin zigzag in-line package. Therefore, the HB66A2568A makes high density mounting possible without surface mount technology. The HB66A2568A provides separate data inputs and output. Its module board has decoupling capacitors to reduce noise.

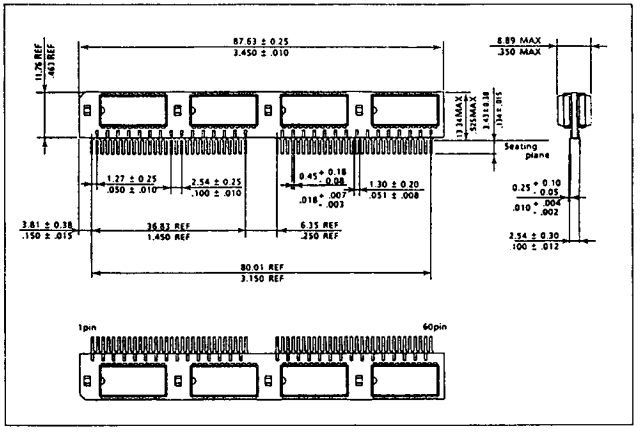
■ FEATURES

- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .2400mW typ.
  - Standby Mode . . . . . .800mW typ. (TTL level)
    0.8mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

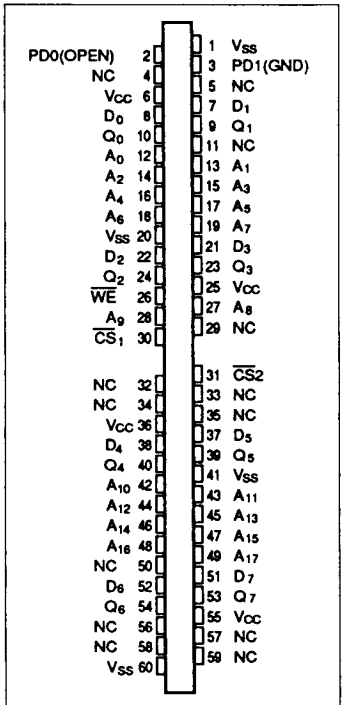
■ ORDERING INFORMATION

Part No.	Access	Package
HB66A2568A-25	25ns	60-pin zigzag in-line leaded type
HB66A2568A-35	35ns	

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_{17}	Address Input
D_0 ~ D_7	Data-in
Q_0 ~ Q_7	Data-out
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

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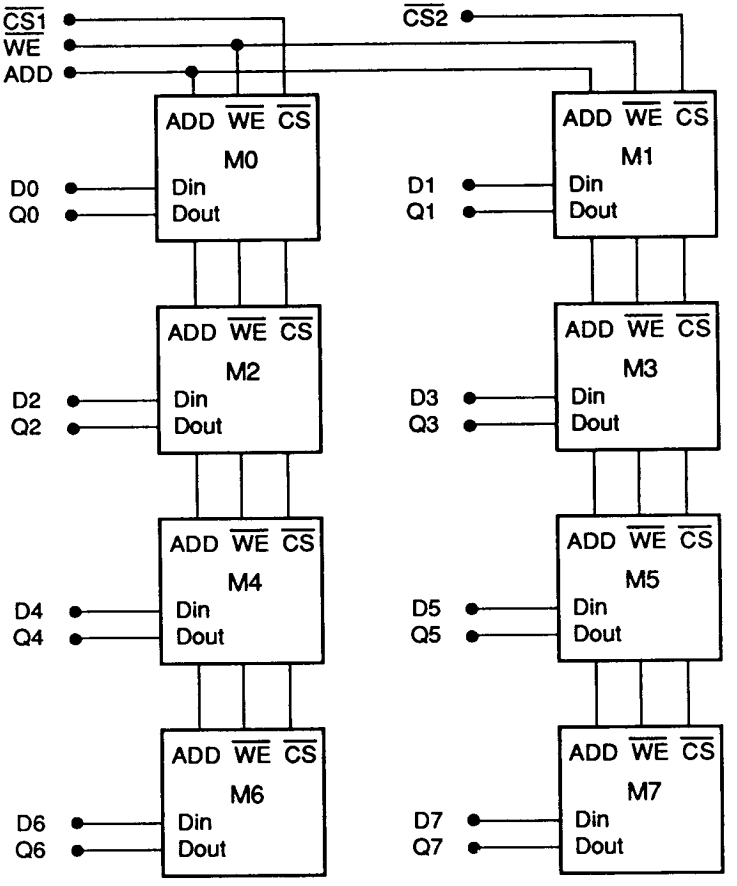
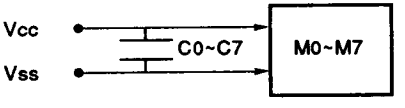
■ BLOCK DIAGRAM





C=0.22μF

* M0~M7 : HM6207HJP

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	−0.5[1] to +7.0	V
Power Dissipation	P_T	8.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: 1. V_{in} min. = −2.5V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}_1$, $\overline{CS}_2$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5[1]	—	0.8	V

NOTE: 1. V_{IL} min. = −2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.[1]	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	−10	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle, Duty = 100%	—	480	960	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH} Min. Cycle	—	160	320	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}_1$, $\overline{CS}_2$ = ≥ V_{CC} −0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} −0.2V	—	0.16	16	mA
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)[1]

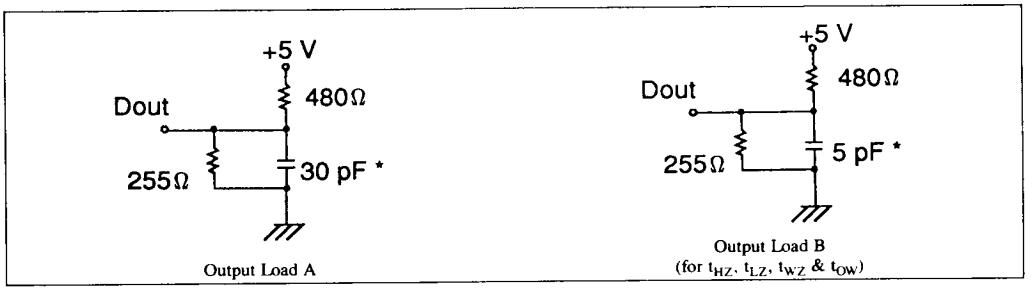
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{WE}$)	C_{I1}	V_{in} = 0V	—	70	pF
Input Capacitance ($\overline{CS}$)	C_{I2}	V_{in} = 0V	—	45	pF
Input Capacitance (Data in)	C_{I3}	V_{in} = 0V	—	12	pF
Output Capacitance (Data out)	C_O	V_{out} = 0V	—	16	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Levels: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figures



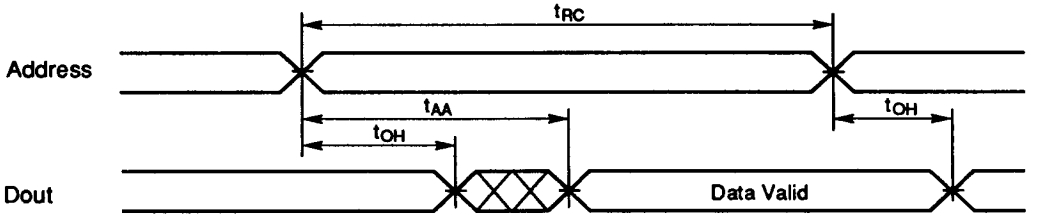
*Including scope and jig capacitance.

• Read Cycle

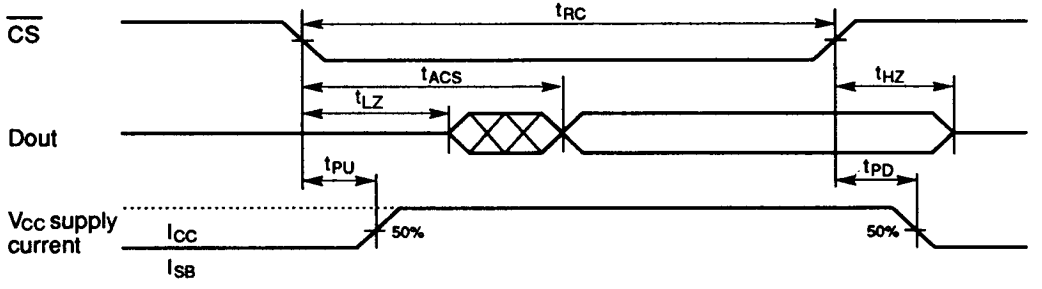
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}(1)	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}(1)	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	ns

NOTE: 1. Transition is measured ±200mV from steady state voltage with Load (B)
This parameter is sampled and not 100% tested.

• **Timing Waveform of Read Cycle (1)** (1) (2)



• **Timing Waveform of Read Cycle (2)** (1) (3)



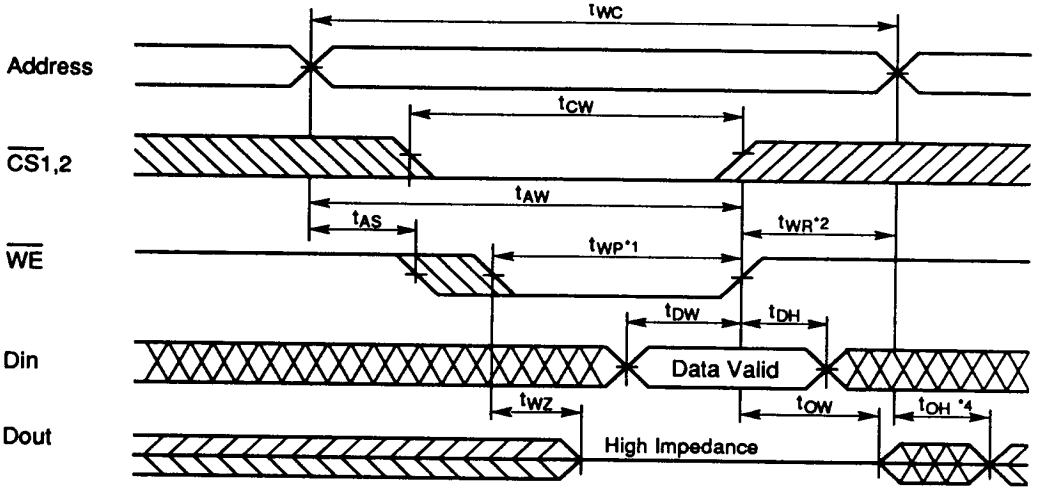
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle**

Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High-Z	t_{WZ}(1)	0	8	0	10	ns
Output Active from End of Write	t_{OW}(2)	0	—	0	—	ns

NOTE: 1. Transition is measured ±200mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• **Timing Waveform of Write Cycle (1)** ($\overline{WE}$ Controlled)



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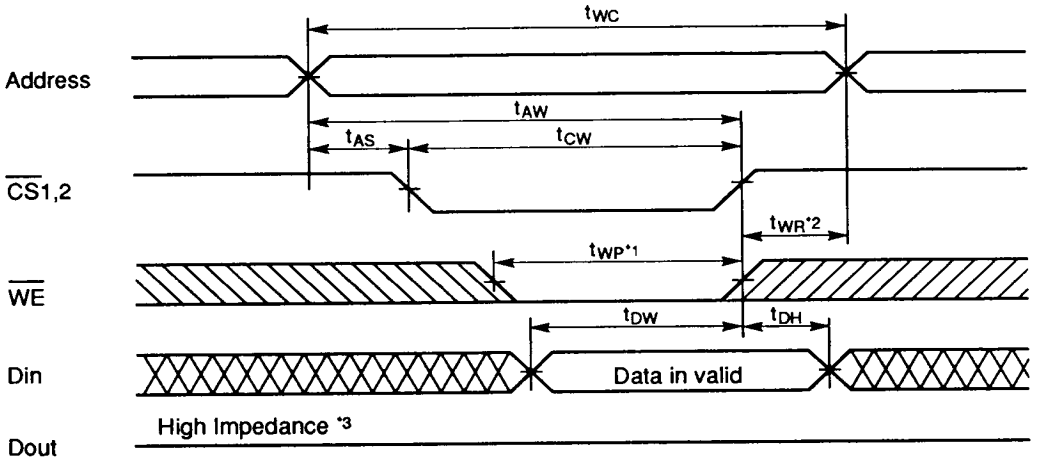
• **Timing Waveform of Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

4. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.