Edge728
Very High-Speed Dual- and Quad-Channel ECL Delay Lines

Description

The Edge728 is a quad delay and deskew element. Manufactured in a high performance bipolar process, it is designed primarily for channel deskew applications in Memory Test Equipment.

The part offers a full scale delay range of ≥ 8.0 ns with independent ± 750 ps adjustment of the falling edge.

The Edge728 has a drive mode, where one input signal is routed to all of the outputs. This mode is particularly useful in a fanout application.

The delay value (and resolution) is controlled via an external voltage DAC.

This deskew element is designed specifically to be monotonic and stable while delaying a very narrow pulse over a wide delay range.

The Edge728 is a pin and functionally compatible upgrade to the Edge628 with the following differences:

- greater net usable delay range
- greater net usable falling edge adjustment range
- only one external bias resistor required
- only one external compensation capacitor required

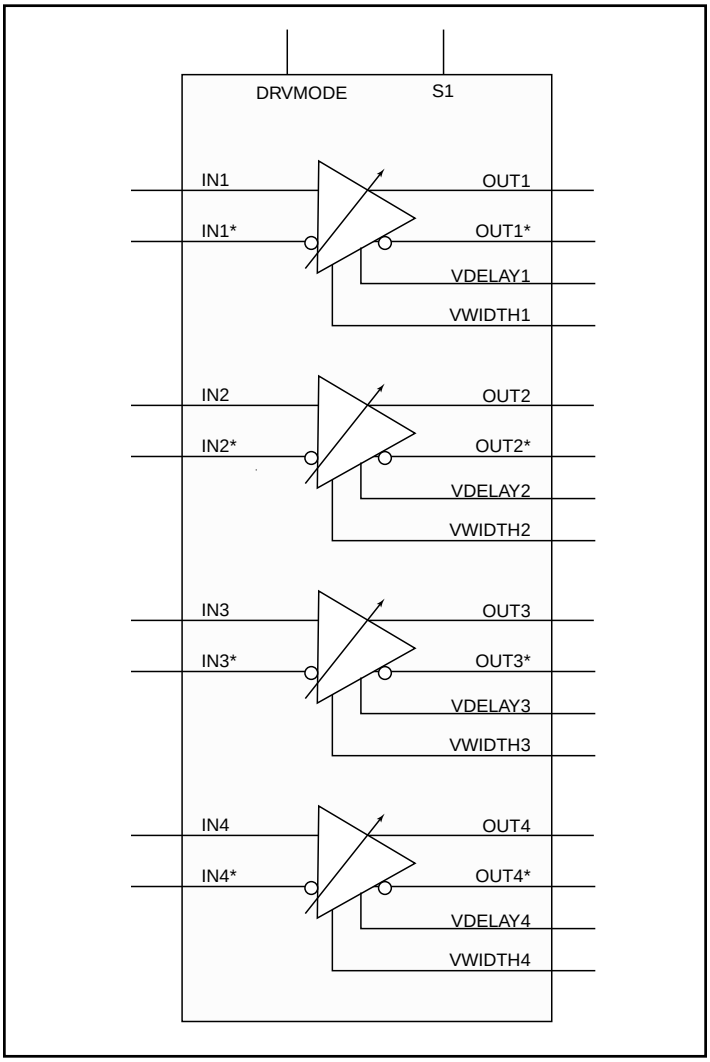
Applications

- Automatic Test Equipment
- Memory Tester Drive On Channel Deskew

Features

- Pin and Functionally Compatible with the Edge 628 and Edge624 in Modes 0 and 2
- Independent Delay Adjustments for Positive and Negative Transitions
- Fanout Mode for One Input Distributed to All Channels
- 44-pin MQFP Package with Internal Heat Spreader, 44-pin PLCC with Internal Heat Spreader, or Die Form

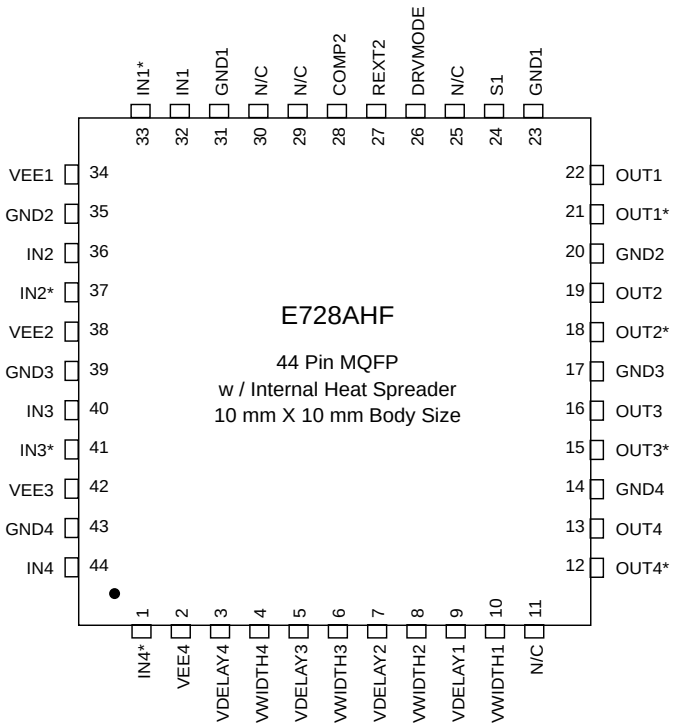
Functional Block Diagram



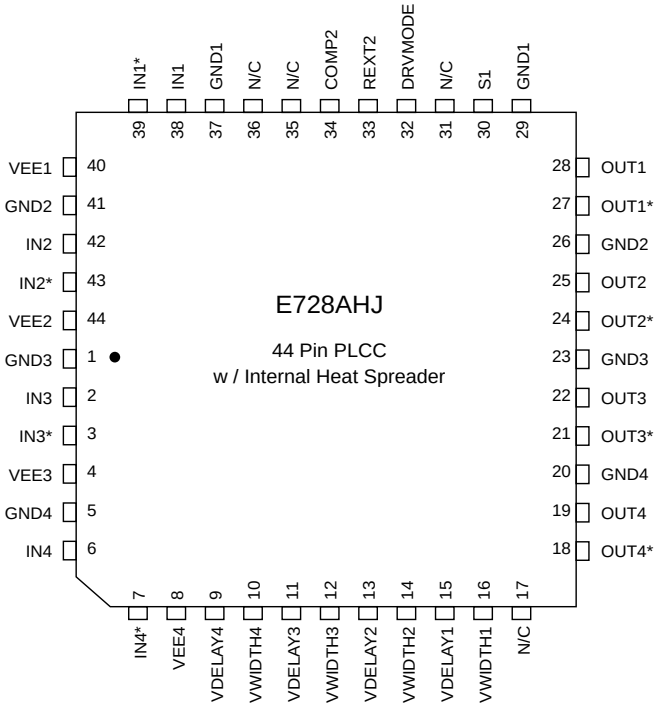
PIN Description

Pin Name	MQFP Pin #	PLCC Pin #	Description
DIGITAL			
IN, IN*	32, 33 36, 37 40, 41 44, 1	38, 39 42, 43 2, 3 6, 7	The input signal to be delayed. (Differential digital inputs.)
OUT, OUT*	22, 21 19, 18 16, 15 13, 12	28, 27 25, 24 22, 21 19, 28	The corresponding delayed output signal. (Differential ECL compatible outputs.)
DRVMODE	26	32	Single-ended 10KH ECL compatible input which determines whether the part is in fanout mode.
S1	24	30	Single-ended 10 KH ECL compatible input which defines the operating mode.
ANALOG			
VDELAY	9, 7, 5, 3	15, 13, 11, 9	Analog voltage input which controls the amount of propagation delay for each channel.
VWIDTH	10, 8, 6, 4	16, 14, 12, 10	Analog voltage input which controls the amount of falling edge delay for each channel.
REXT2	27	33	Analog input current used to establish the bias level for the delay cells.
COMP2	28	34	Compensation pin.
POWER			
GND	39, 43, 14, 17, 20, 23, 31, 35	1, 5, 20, 23, 26, 29, 37, 41	Device ground.
VEE	42, 2, 34, 38	4, 8, 40, 44	Device power supply.
N/C	11, 25, 29, 30	17, 31, 35, 36	No connect. There is no circuitry connected to these pins inside the package. These pins are not wire bonded to the die.

PIN Description *(continued)*



E728AHF
44-Pin MQFP
w/Internal Heat Spreader



E728AHJ
44-Pin PLCC
w/Internal Heat Spreader

Circuit Description

Chip Overview

The Edge728 is a quad delay line and deskew element offering a 8.0 ns minimum delay (Tspan), where the VDELAY inputs adjust the overall propagation delay of the part. In addition, the parts support a separate rising and falling edge delay of ± 750 ps (Twidth), where the VWIDTH inputs control the falling edge delay. There is also a drive mode, where the channel 2 input drives all four Edge728 outputs, with all other inputs ignored.

The Edge728 is designed to be monotonic and very stable in all modes of operation. Figure 1 shows a simplified block diagram.

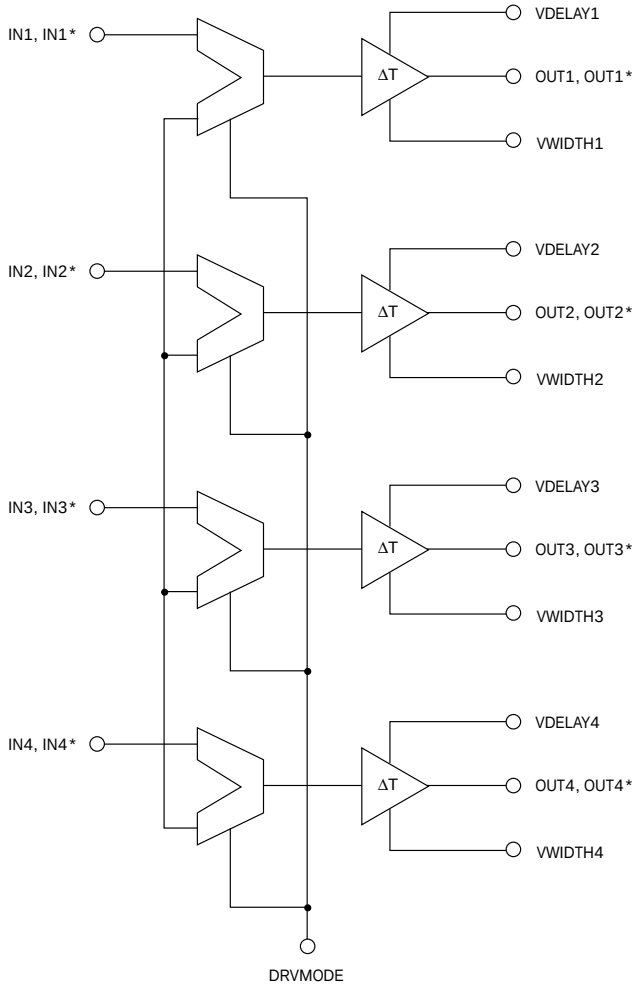


Figure 1. Edge728 Block Diagram

Operating Modes

The Edge728 has two modes of operation (described in Table 1.)

Mode	S1	TSPAN	TWIDTH
0	0	>= 8.0 ns	N/A
2	1	>= 8.0 ns	±750 ps

Table 1. Delay Ranges Versus Mode

Mode 0

Mode 0 is a simple delay mode (see Figures 2 and 3). The input signal for each channel is delayed by some programmable amount determined by the analog input VDELAY.

The rising and falling edges are delayed equally. The VWIDTH analog input has no function in mode 0, and should be connected to device GND when used exclusively in this mode. The propagation delay for a rising and falling edge is defined as

$$Tpd+, Tpd- = Tpd(min) + Tspan$$

where Tpd(min) is the raw propagation delay of the part with minimum programmed delay, and Tspan is the additional delay programmed via the VDELAY input.

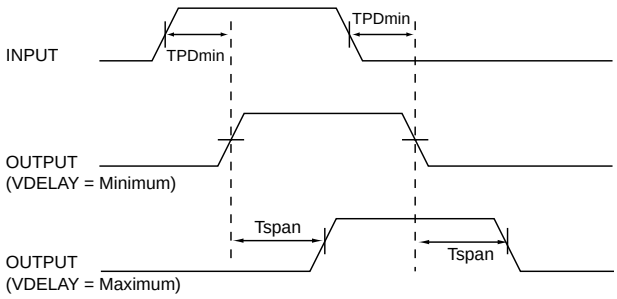


Figure 2. Mode 0 VDELAY Control

Circuit Description *(continued)*

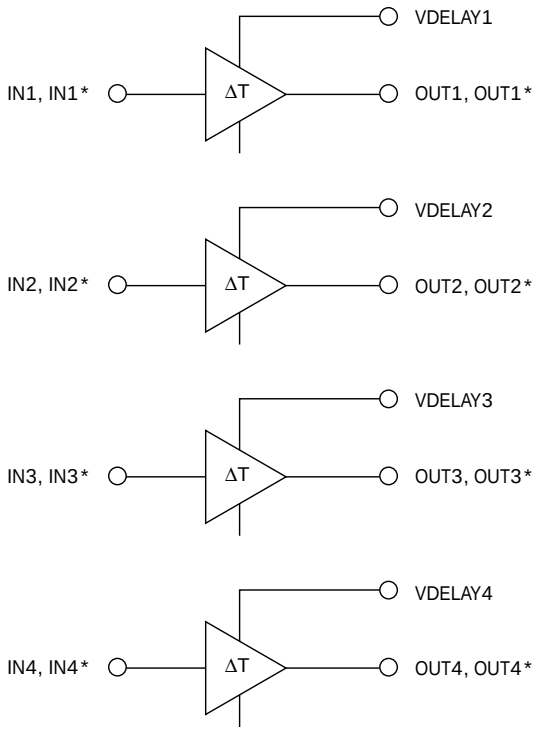


Figure 3. Mode 0 Functional Diagram

Analog Delay Inputs

VDELAY and VWIDTH are high input impedance analog voltage inputs which control the delay of the rising and falling edge. VWIDTH can vary from –0.1V to –1.1V, and VDELAY can vary from –0.2V to –1.1V. When both inputs are –1.1V, a maximum delay results.

If mode 0 is used, connect all VWIDTH inputs to GND. Also, connect any unused VDELAY and VWIDTH inputs to GND.

Mode 2

Mode 2 allows independent adjustment of the rising and falling edges (see Figures 4 and 5). The propagation delay for a rising edge is defined as

$$Tpd+ = Tpd(min) + Tspan$$

where Tpd(min) is the raw propagation delay of the part with minimum programmed delay, and Tspan is the additional delay programmed via the VDELAY input.

The propagation delay for a falling edge is defined as

$$Tpd- = Tpd(min) + Tspan + Twidth$$

where Twidth is defined as the additional delay incurred by adjusting the VWIDTH input. Notice that Twidth can be either positive or negative, allowing the part to either expand or contract an input signal (see Figure 4).

Notice also that Tpd+ is a function of VDELAY only, while Tpd– is a function of VDELAY and VWIDTH. The transfer function for Tspan vs. VDELAY is shown for both modes in Figure 4. The transfer function for Twidth vs. VWIDTH and VDELAY is shown in Figure 6.

REXT2

REXT2 is an analog current input used to establish the bias current of the delay cells. An external resistor of 2.74 KΩ should be connected between REXT2 and ground. The voltage on REXT2 is forced to ~ –1.34V, producing an input current of (1.34V) / 2.74 KΩ = 489 µA.

COMP2

COMP2 is an op amp compensation pin and requires an external capacitor of 0.01 µF (X7R type) connected to either VEE or ground.

Circuit Description *(continued)*

Programming Sequence

VDELAY, in addition to affecting the placement of the rising edge, also affects the falling edge. Therefore, when calibrating a system, VDELAY should be adjusted first. As VWIDTH affects only the falling edge, it should be adjusted only after VDELAY is established.

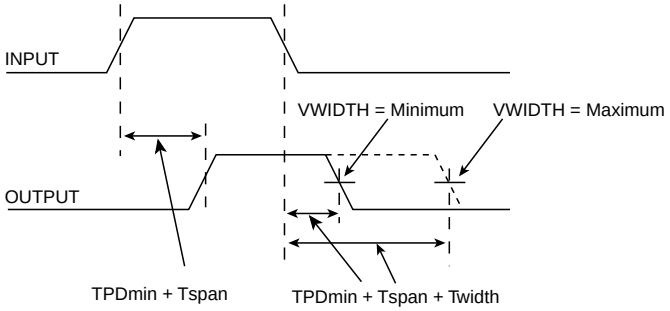


Figure 4. Mode 2 VDELAY and VWIDTH Controls

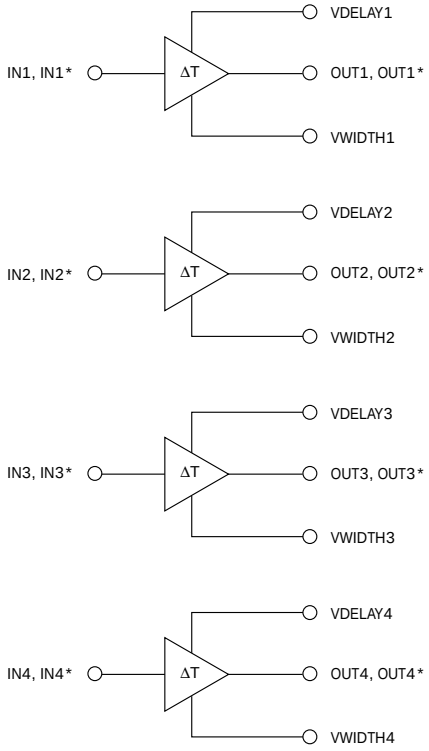


Figure 5. Function Model in Mode 2

Circuit Description *(continued)*

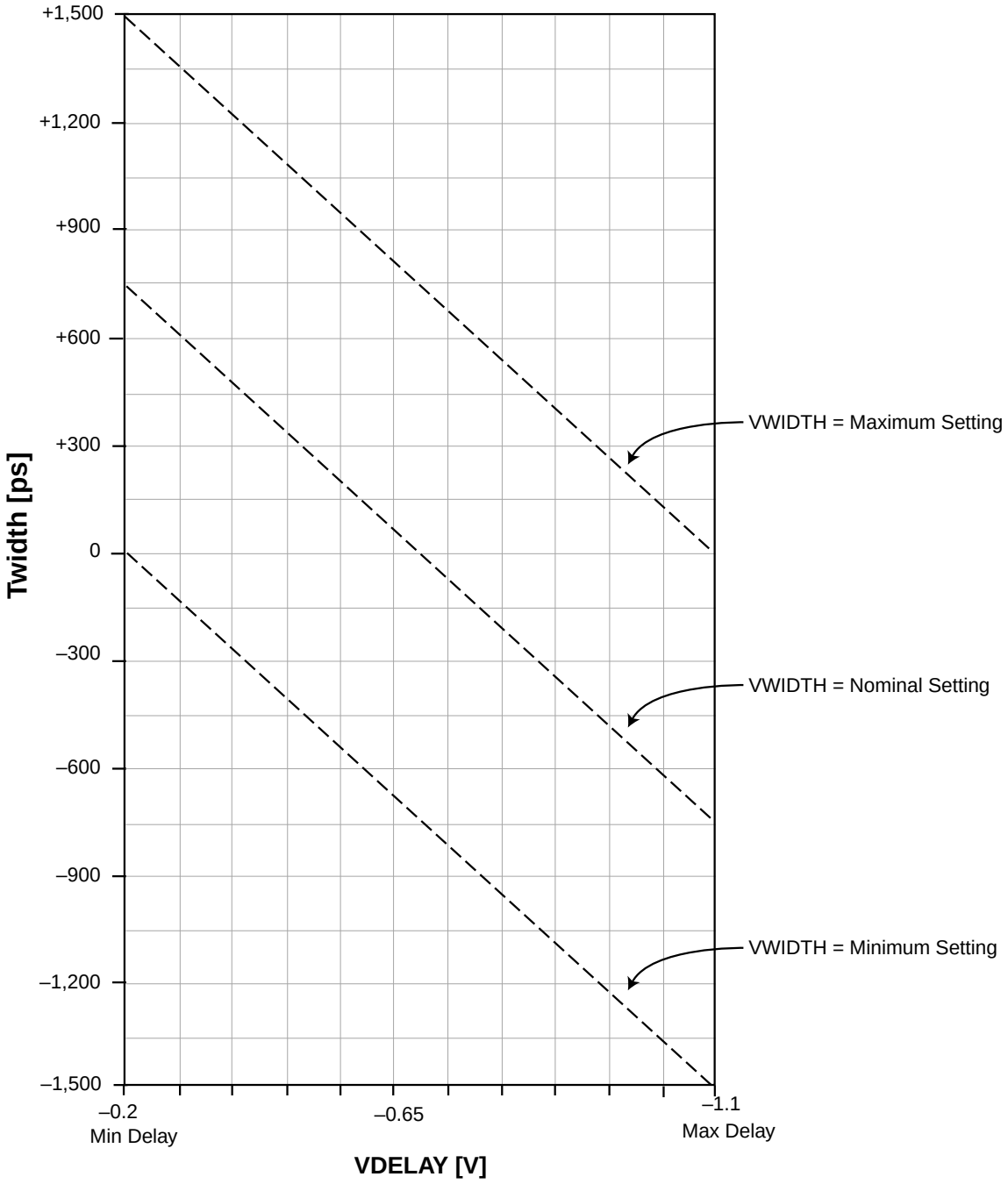


Figure 6. Mode 2 Transfer Function

Circuit Description *(continued)*

Drive Mode

With DRVMODE = 1, the input signal on channel 2 will be routed to all Edge728 delay paths. In drive mode, operating mode 0 and 2 still offer the same delay range and edge control features. The only difference is that the input signal now comes from channel 2, while all other inputs (IN1 / IN1*, IN3 / IN3*, and IN4 / IN4*) are ignored.

Figures 7 and 8 show a simplified model for drive mode.

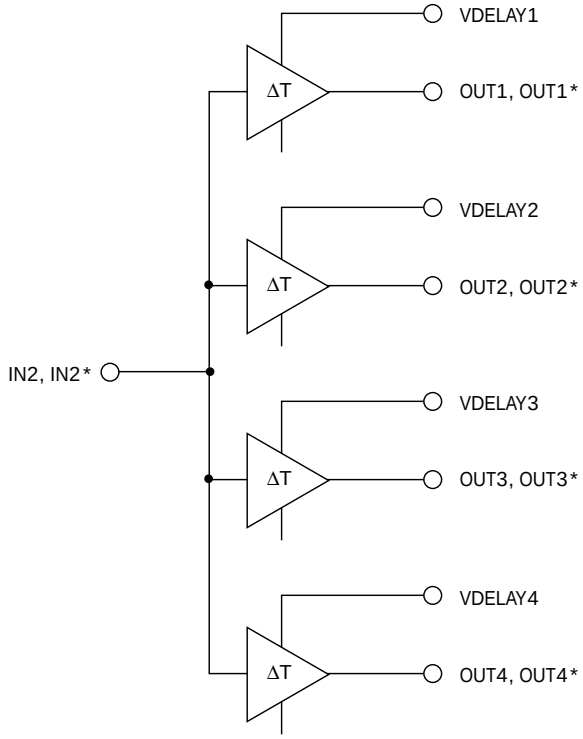


Figure 7. Edge728 Drive Mode for Operating Mode 0

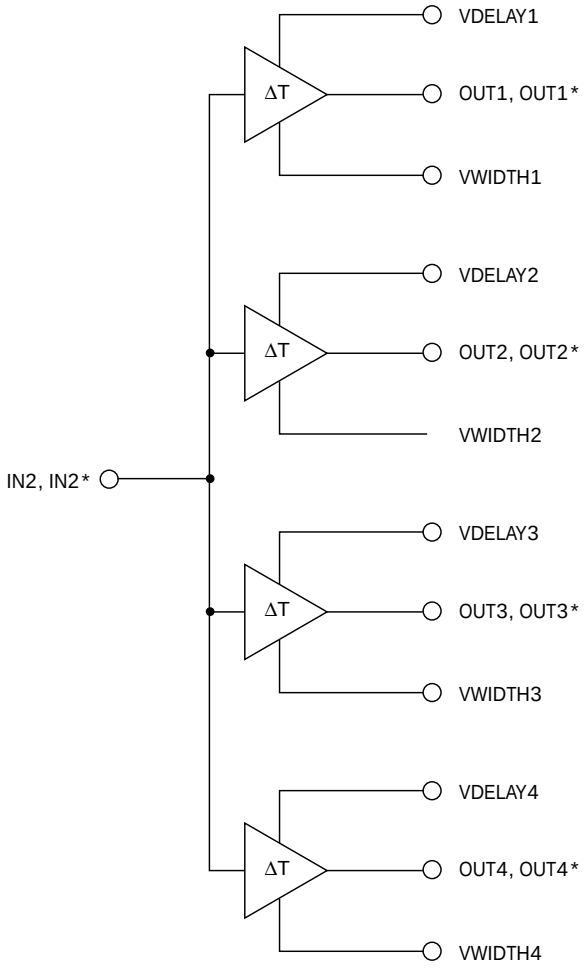


Figure 8. Edge728 Drive Mode for Operating Mode 2

Application Information

Power Up Initialization

Note: Mode 2 uses an SR flip-flop at the output stage; mode 0 does not. Therefore, upon power-up in mode 2, or when operating modes are being changed into mode 2, the SR flip-flop is in an indeterminate state and the output may not reflect the input condition. A rising or falling edge that propagates through the channel will correctly reset the part. Therefore, in mode 2, a dummy edge should be applied before calibration or real time execution.

Notice also that in mode 0 there are NO flip-flops. The outputs will, therefore, always reflect the status of the inputs.

PECL Operation

It is possible to use the part with positive voltage supplies. GND becomes VCC and VEE becomes GND. All voltages are then referenced off of the positive supply level.

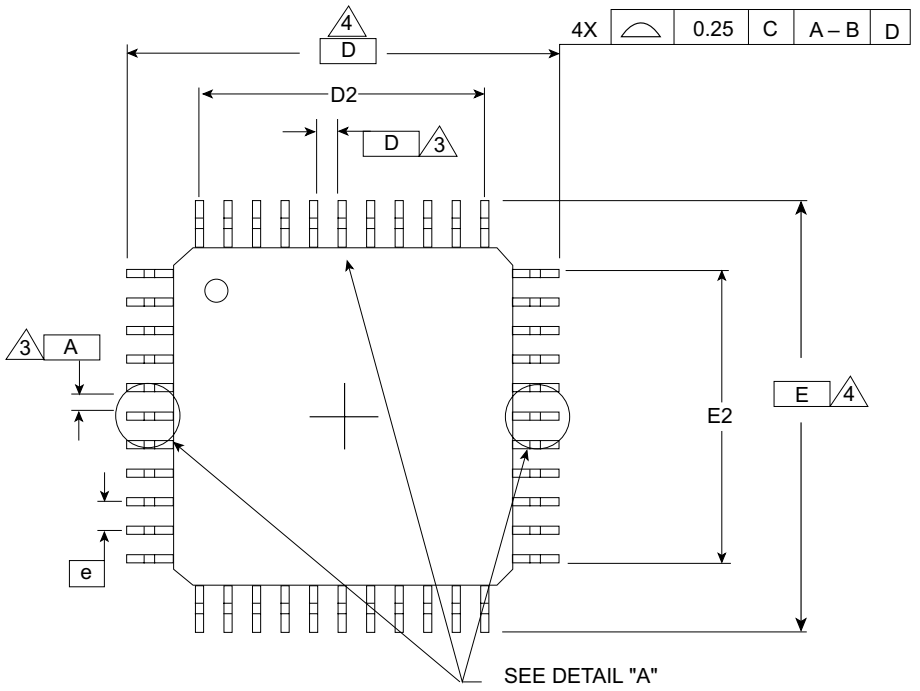
Analog Voltage Inputs

The VWIDTH input has a normal operating range between –0.1V and –1.1V, and the VDELAY input has a normal operating range between –0.2V and –1.1V. However, the on-board ESD diodes are rated to allow the direct connection of a voltage DAC that can range from +7.5V to –4V, through a resistance of ≥ 600Ω, with no damage

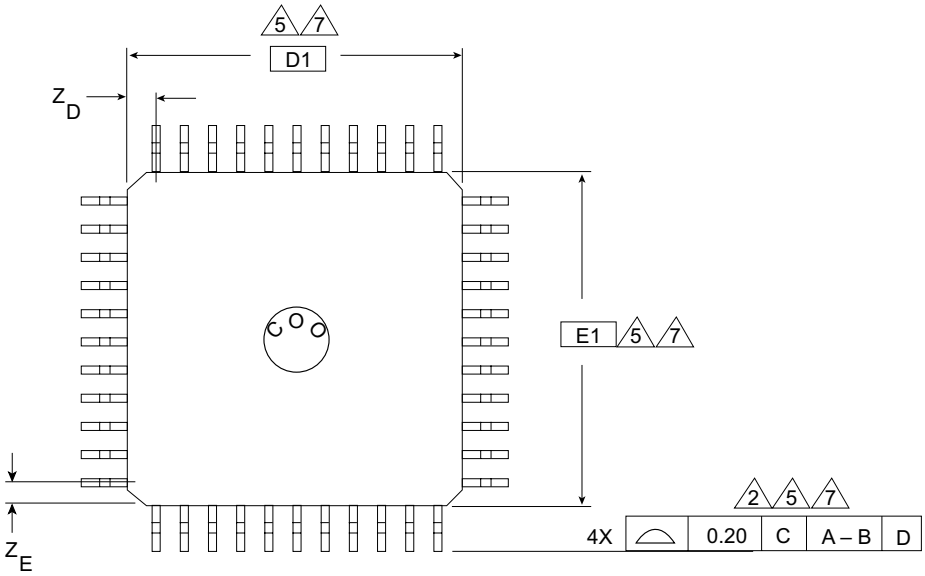
Package Thermal Data

Parameter	Symbol	Min	Typ	Max	Units
Thermal Resistance					
PLCC w/Heat Spreader					
Junction to Air					
Still Air	θJA		41		°C/W
50 LFPM of Airflow	θJA		33		°C/W
400 LFPM of Airflow	θJA		21		°C/W
MQFP w/Heat Spreader					
Junction to Air					
Still Air	θJA		38		°C/W
50 LFPM of Airflow	θJA		36		°C/W
400 LFPM of Airflow	θJA		32		°C/W
Junction to Case	θJC		16		°C/W

44-Pin MQFP (10mm x 10mm)

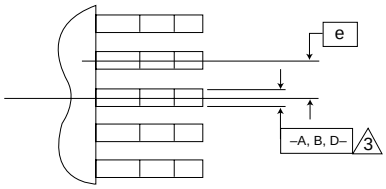


TOP VIEW

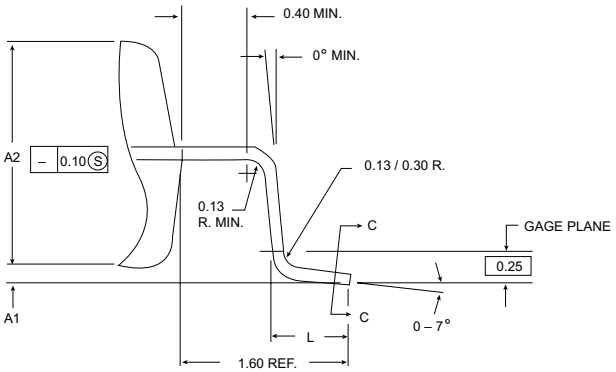


BOTTOM VIEW

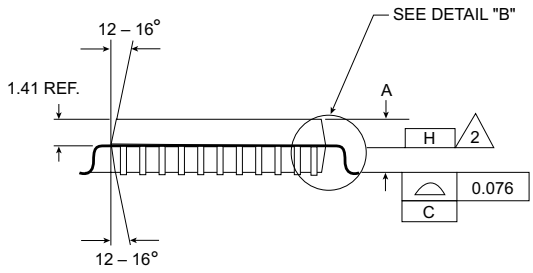
Package Information *(continued)*

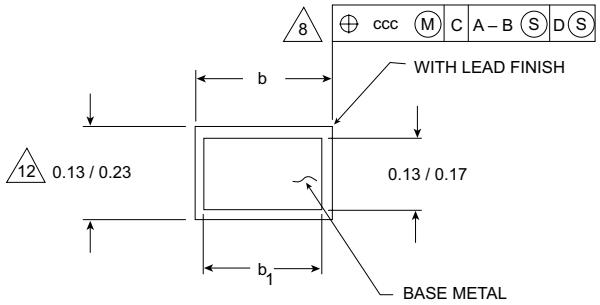


DETAIL "A"



DETAIL "B"





SECTION C-C

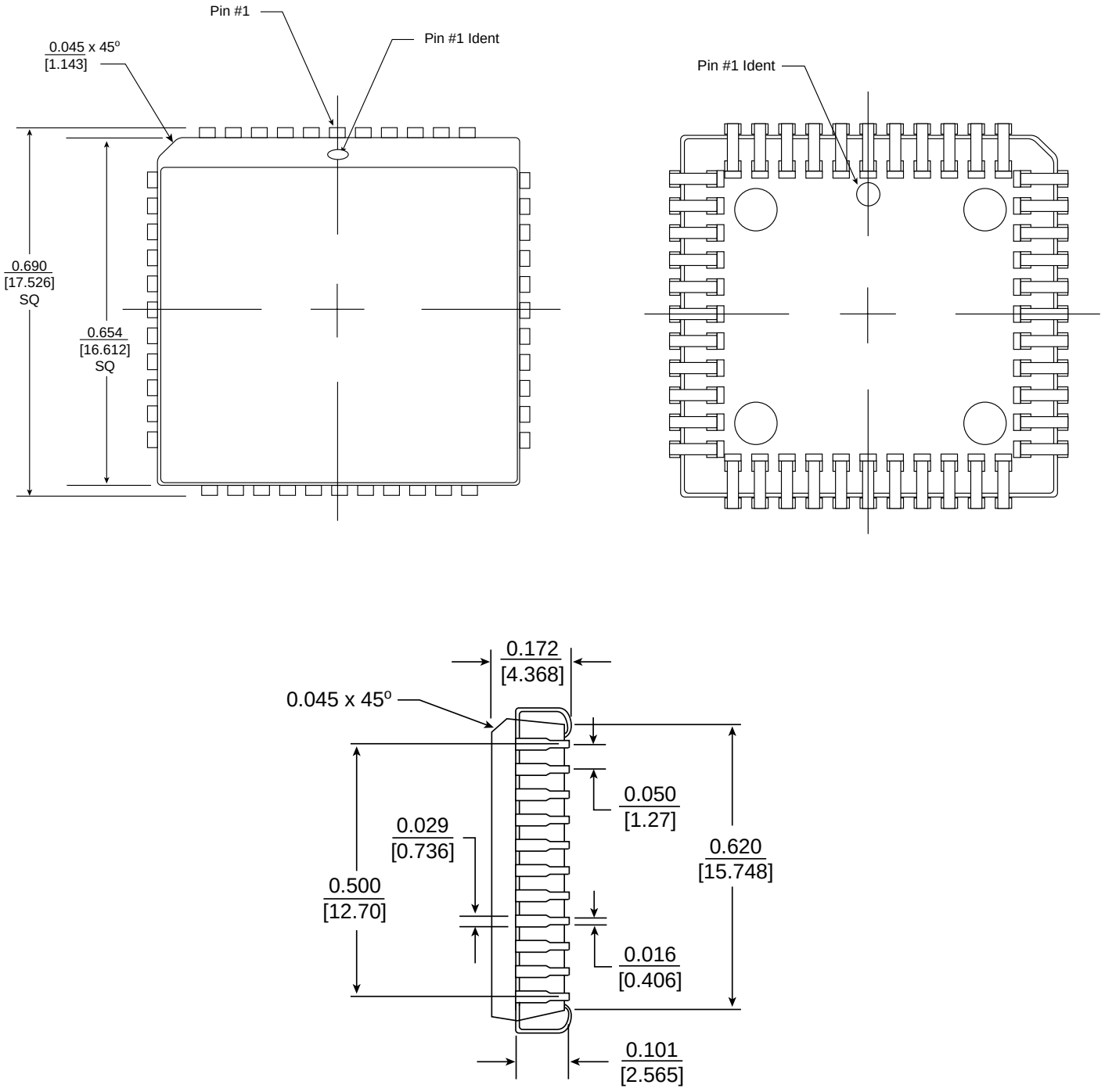
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined where centerline between leads exits plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions by 0.20 mm, and top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outline MS-108.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Symbol	Min	Nom	Max	Note	Comments
A		2.15	2.35		Height above PCB
A1	0.10	0.15	0.25		PCB Clearance
A2	1.95	2.00	2.10		Body Thickness
D		13.20 BSC		4	
D1		10.00 BSC		5	Body Length
D2		8.00 REF			
ZD		1.00 REF			
E		13.20 BSC		4	
E1		10.00 BSC		5	Body Width
E2		8.00 REF			
ZE		1.00 REF			
L	0.73	0.88	1.03		
N		44		6	Pin Count
e		0.80			Lead Pitch
b	0.30		0.45	8	
b1	0.30	0.30	0.40		
aaa		0.16			

Package Information *(continued)*

44 Pin PLCC Package



Notes: (unless otherwise specified)

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	V
Negative Power Supply	VEE	–4.9	–5.2	–5.5	V
Analog Input Voltage Range					
VDELAY (1–4)	Vin_delay	–1.1		–0.2	V
WIDTH (1–4)	Vin_width	–1.1		–0.1	V
Case Temperature	TC	5		65	˚C
Input Clamp Current on Analog Inputs	I_{CL}	–15		+15	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (relative to GND)		–6.0		0.4	V
Voltage on any Digital Pin		VEE – 0.4		0.4	V
Voltage on any Analog Pin		VEE – 0.4		0.4	V
Input Clamp Current on Analog Inputs VDELAY (1–4), VWIDTH (1–4)	I_{CL}	–20		+20	mA
Output Current		–50		0	mA
Ambient Operating Temperature	TA	–55		125	˚C
Storage Temperature	TS	–65		150	˚C
Junction Temperature	TJ			150	˚C
Soldering Conditions					
Lead Temperature During Soldering for < = 20 seconds				285	˚C
Case Temperature During Soldering for < = 15 seconds				225	˚C
Temperature Ramp Up or Down		–4		+4	˚C/sec

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Differential Inputs (IN1/IN1* – IN4/IN4*)					
Digital Input High Voltage	IN – IN*	250			mV
Digital Input Low Voltage	IN* – IN	250			mV
Input Common Mode Range	VIH, VIL	–2.0		–0.5	V
Single-Ended Inputs (DRVMODE, S1)					
Digital Input High Voltage	VIH	–1070		0	mV
Digital Input Low Voltage	VIL	VEE		–1450	mV
Input High Current (Vin = VIHmax)	IIH	–1	1.5	250	µA
Input Low Current (Vin = VILmin)	IIL	–1	0	150	µA
Outputs					
Digital Output High Voltage	OUT – OUT*	0.500		1.0	V
Digital Output Low Voltage	OUT* – OUT	0.500	0.753	1.0	V
Output Common Mode Range	$\frac{OUT + OUT^*}{2}$	–1.5	–1.3	–1.1	V
VEE Supply Current	IEE	–320		–250	mA
Analog Inputs VDELAY (1–4), VWIDTH (1–4)					
Input Current (tested @ –0.1V, –1.1V)	Iin	0		15	µA
Voltage Level at REXT2	VEXT2	–1.55	–1.34	–1.25	V
Temperature Coefficient (Note 1)	$\Delta Iin/\Delta T$	–.1		.1	µA/˚C

Test conditions: All outputs terminated with 50 Ω to –2.0 V in parallel with 5 pF. Tested @ VEE = –4.9V and VEE = –5.5V. REXT2 = 2.74KΩ ± 1%, with temp. co. ≤ 100 ppm.

Note 1: Based upon characterization data. Not production tested. Specified over 5 to 65˚C case temperature range.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Modes 0 and 2 Operation					
Programmable Delay Range (VDELAY from –0.2 to –1.1V)	Tspan	8.25	9.4	13.0	ns
Minimum Pulse Width (Note 1) @ VDELAY = –1.1V, VWIDTH = –1.1V	PWmin	1.8			ns
Maximum Operating Frequency (Note 1) @ VDELAY = –1.1V, VWIDTH = –1.1V	Fmax	250	260		MHz
Output Rise/Fall Time (20% / 80%) (Note 1)	Tr/Tf		232	300	ps
Rising Edge/Falling Edge Propagation Delay Variation (Note 1, Mode 0)	$\lvert Tpd^{+} - Tpd^{-} \rvert$		15	30	ps
Temperature Coefficient (Notes 1, 2) –1.1V < = VDELAY < = –0.2V –1.1V < = VWIDTH < = –0.1V	ΔTpd/ΔT			4.5	ps / ˚C
–1.1V < = VDELAY < = –0.2V –1.3V < = VWIDTH < = –0.1V	ΔTpd/ΔT			6	ps / ˚C
Total Timing Error (for any pulse > = 2.3 ns at the input) (Note 1) 1) vs. Pulse Width 2) vs. Frequency 3) vs. Duty Cycle 4) Channel to Channel Crosstalk 5) –1.1V < = VDELAY < = –0.2V 6) –1.1V < = VWIDTH < = –0.2V	ΔTpd	–55		+55	ps
Total Timing Error (for any 2.3 ns > pulse > = 1.8 ns at the input) (Note 1) 1) vs. Pulse Width 2) vs. Frequency 3) vs. Duty Cycle 4) Channel to Channel Crosstalk 5) VDELAY = –0.2V 6) –0.2V < VWIDTH < = –0.1V	ΔTpd	–75		+75	ps
Power Supply Induced Jitter (Note 1) <100 mV Pk-to-Pk 5 Hz < = F < = 2 MHz	PSRR			30 ps 5 ps	pk-to-pk 1σ

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Mode 0 Operation Propagation Delay (VDELAY = –0.2V)	Tpdmin	3.95		5.2	ns
Mode 2 Operation Propagation Delay (VDELAY = –0.2V)	Tpdmin	4.15		5.4	ns
Output Pulse Width Test Input Pulse Width = 10.0 ns VWIDTH = –0.1V VDELAY = –1.1V	PW	6.5	7.25	8.5	ns
Output Pulse Width Test Input Pulse Width = 10.0 ns VWIDTH = –1.3V VDELAY = –0.2V	PW	11.5	12.1	14.0	ns

Test conditions: All outputs terminated with 50 Ω to –2.0 V in parallel with 5 pF. Tested @ VEE = –4.9V and VEE = –5.5V. REXT2 = 2.74KΩ ± 1%, with temp. co. ≤ 100 ppm.

Note 1: Based upon characterization data. Not production tested.
Note 2: Specified over a 5 to 65˚C case temperature range.

Ordering Information

Model Number	Package
E728AHF	44 Pin MQFP w/Internal Heat Spreader 10 mm X 10 mm Body Size
E728AHF-T	44 Pin MQFP w/Internal Heat Spreader 10 m x 10 mm Body Size (Tape and Reel)
E728AHJ	44 Pin PLCC w/Internal Heat Spreader
D728	Die

Contact Information

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10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633

Revision Histor y

Current Revision Date: February 18, 2002
Previous Revision Date: November 14, 2001

Page #	Section Name	Previous Revision	Current Revision
All	Package Info		*Add:* 44 Pin PLCC Package

Current Revision Date: November 14, 2001
Previous Revision Date: July 12, 2001

Page #	Section Name	Previous Revision	Current Revision
14	AC Characteristics		*Add:* Rising Edge/Falling Edge Propagation Delay Variation

Current Revision Date: July 12, 2001
Previous Revision Date: April 26, 2001

Page #	Section Name	Previous Revision	Current Revision
14	AC Characteristics	Programmable Delay Range, Min: 8.0	Programmable Delay Range, Min: 8.25
		Temperature Coefficient –1.1V < = VDELAY < = –0.2V, Max: 4	Temperature Coefficient –1.1V < = VDELAY < = –0.2V, Max: 4.5
		Power Supply Induced Jitter, Max: 24 ps, 4 ps	Power Supply Induced Jitter, Max: 30 ps, 5 ps
		Mode 0 Propagation Delay, Min: 4.1, Max: 5.1	Mode 0 Propagation Delay, Min: 3.95, Max: 5.2
		Mode 2 Propagation Delay, Min: 4.25, Max: 5.25	Mode 2 Propagation Delay, Min: 4.15, Max: 5.4

Current Revision Date: April 26, 2001
Previous Revision Date: April 17, 2001

Page #	Section Name	Previous Revision	Current Revision
14	AC Characteristics	Power Supply Induced Jitter < 150 mV Pk-to-Pk	Power Supply Induced Jitter < 100 mV Pk-to-Pk