TEMIC

MATRA MHS

M 65698

64 K × 4 Ultimate CMOS SRAM

Introduction

The M 65698 is a very low power CMOS static RAM organized as 65536 × 4 bits. It is manufactured using the MHS high performance CMOS technology named SCMOS.

With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M 65698 combines an extremely low standby supply current (Typical value = 0.1 µA) with a fast access time at 40 ns. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

The M 67698 is 100 % processed following the test methods of MIL STD 883 and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

Features

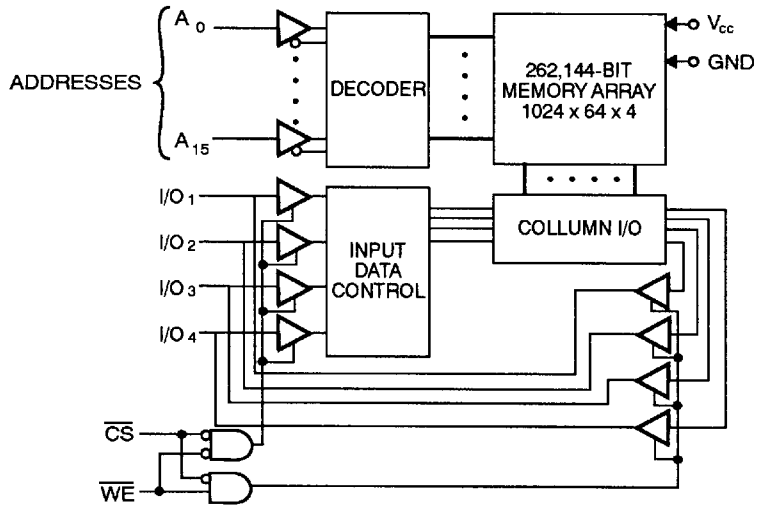
- Access time
  commercial : 35(*), 40, 45, 55 ns
  industrial and military : 40(*), 45, 55 ns
- Very low power consumption
  active : 50 mW (typ)
  standby : 0.5 W (typ)
  data retention : 0.4 W (typ)
- Wide temperature range : -55 to + 125 °C

(*) Preliminary. Consult sales.

- 300 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Single 5 volt supply
- Equal cycle and access time
- Gated inputs : no pull-up/down resistors are required

Interface

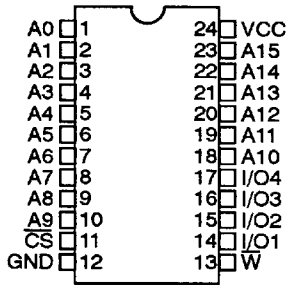
Block Diagram



M 65698

Pin Configuration

Side Brazed 300 mils 24 pins



(Top View)

(*) SOIC 300 mils 28 pins
(*) Multilayer Flat Pack 28 pins
(*) Consult sales for availability

Pin Description

A_0-A_{15}	:	Address inputs	$\overline{CS}$	:	Chip-Select
I/O1-I/O4	:	Input/Output	$\overline{W}$	:	Write Enable
V_{CC}	:	Power			
V_{SS}	:	Ground			

Truth Table

$\overline{CS}$	$\overline{W}$	INPUTS/ OUTPUTS	MODE
H	X	Z	Deselect/ POWER-DOWN
L	H	DATA OUT	Read
L	L	DATA IN	Write

L = low, H = high, X = H or L, Z = high impedance

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : ..... -0.5 V to + 7.0 V
Input or Output voltage applied : ..... (Gnd - 0.3 V) to (Vcc + 0.3 V)
Storage temperature : ..... -65 °C to + 150 °C
Electro static discharge voltage ..... > 1250 V (MIL STD 883, METHOD 3015)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	V_{CC} = 5 V ± 10 %	- 55 °C to + 125 °C
Industrial	V_{CC} = 5 V ± 10 %	- 40 °C to 85 °C
Commercial	V_{CC} = 5 V ± 10 %	0 °C to 70 °C

DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	- 0.3	0.0	0.8	V
VIH(1)	Input high voltage	2.2	-	Vcc + 0.3	V

Note : 1. VIH max = Vcc + 0.3 V, VIL min = -0.3 V or -1.0 pulse 50 ns.

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	8	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

DC Parameter

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	- 1.0	–	1.0	µA
IOZ(3)	Output leakage current	- 1.0	–	1.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4 mA, IOH = –1.0 mA.

Consumption for Commercial Specification

SYMBOL	PARAMETER	M 65698 L-35(*)	M 65698 V-35(*)	M 65698 L - 40	M 65698 V - 40	M 65698 L - 45	M 65698 V - 45	M 65698 L - 55	M 65698 V - 55	UNIT	VALUE
ICCSB (5)	Standby supply current	10	5	10	5	10	5	10	5	mA	max
ICCSB1 (6)	Standby supply current	75	5	75	5	75	5	75	5	µA	max
ICCOP (7)	Operating supply current	90	70	90	70	90	70	90	70	mA	max

Consumption for Industrial Specification

SYMBOL	PARAMETER	M 65698 L - 40(*)	M 65698 V - 40(*)	M 65698 L - 45	M 65698 V - 45	M 65698 L - 55	M 65698 V - 55	UNIT	VALUE
ICCSB (5)	Standby supply current	10	5	10	5	10	5	mA	max
ICCSB1 (6)	Standby supply current	100	10	100	10	100	10	µA	max
ICCOP (7)	Operating supply current	90	70	90	70	90	70	mA	max

Consumption for Military Specification

SYMBOL	PARAMETER	M 65698 L - 40(*)	M 65698 V - 40(*)	M 65698 L - 45	M 65698 V - 45	M 65698 L - 55	M 65698 V - 55	UNIT	VALUE
ICCSB (5)	Standby supply current	10	5	10	5	10	5	mA	max
ICCSB1 (6)	Standby supply current	500	100	500	100	500	100	µA	max
ICCOP (7)	Operating supply current	90	70	90	70	90	70	mA	max

Notes : 5. $\overline{CS} \geq$ VIH, Vin ≥ VIH or Vin ≤ VIL.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA. Vin ≥ Vcc – 0.3 V or Vin ≤ 0.3 V.
7. Vcc max, Iout = 0 mA, Vin = Gnd/Vcc. Duty cycle 100 %, f = 5 MHz, derating = 10 mA/MHz.
(*) Preliminary. Please consult sales.

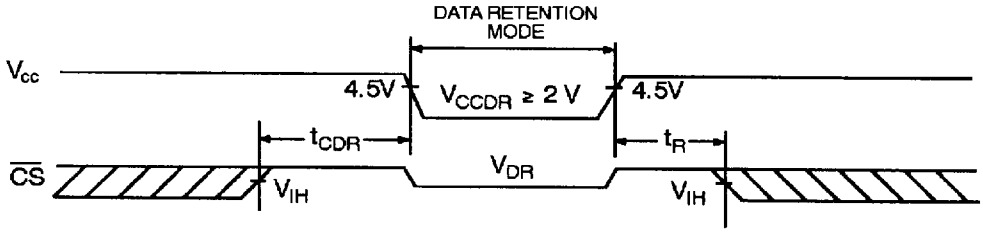
M 65698

Data Retention Mode

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc - 0.2 V.
2. $\overline{CS}$ must be kept between Vcc - 0.3 V and 70 % of Vcc during the power up and power down transitions.
3. The RAM can begIn operation > 45 ns after Vcc reaches the minimum operating voltage (4.5 V).

Timing



Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (8)	MAXIMUM			UNIT
VCCDR	Vcc for data retention	2.0	-	-			V
TCDR	Chip deselect to data retention time	0.0	-	-			ns
TR	Operation recovery time	TAVAV (9)	-	-			ns
ICCDR1 (10)	Data retention current			COM	IND	MIL	
	@ 2.0 V : M-65698 V	-	0.1	3	8	80	µA
	M-65698 L	-	0.1	60	80	300	µA
ICCDR2 (10)	Data retention current						
	@ 3.0 V : M-65698 V	-	0.3	4	9	90	µA
	M-65698 L	-	0.3	70	90	400	µA

Notes : 8. TA = 25°C.
9. TAVAV = Read cycle time.
10. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested at Vcc = 2 V.

AC Parameters

AC Conditions :

Input pulse levels : ..... Gnd to 3.0 V
Input rise : ..... 5 ns
Input timing reference levels : ..... 1.5 V
Output load : ..... See fig. 1a, 1b

Write Cycle : Commercial Specifications (note 12)

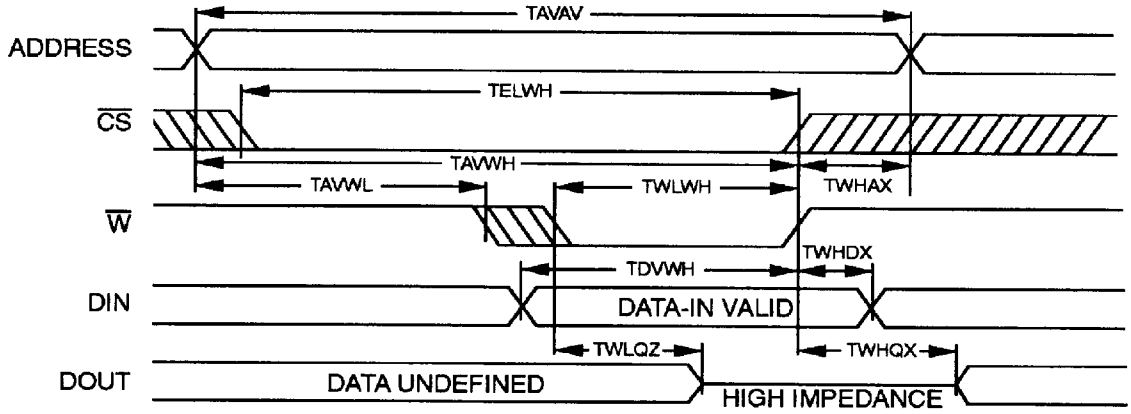
SYMBOL	PARAMETER	M 65698 L/V - 35(*)	M 65698 L/V - 40	M 65698 L/V - 45	M 65698 L/V - 55	UNIT	VALUE
TAVAV	Write cycle time	35	40	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	30	30	40	50	ns	min
TDVWH	Data set-up time	20	22	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	30	40	50	ns	min
TWLQZ (11)	Write low to high Z	15	15	15	20	ns	max
TWLWH	Write pulse width	30	30	40	50	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	0	0	ns	min

Write Cycle : Industrial and Military Specification (note 12)

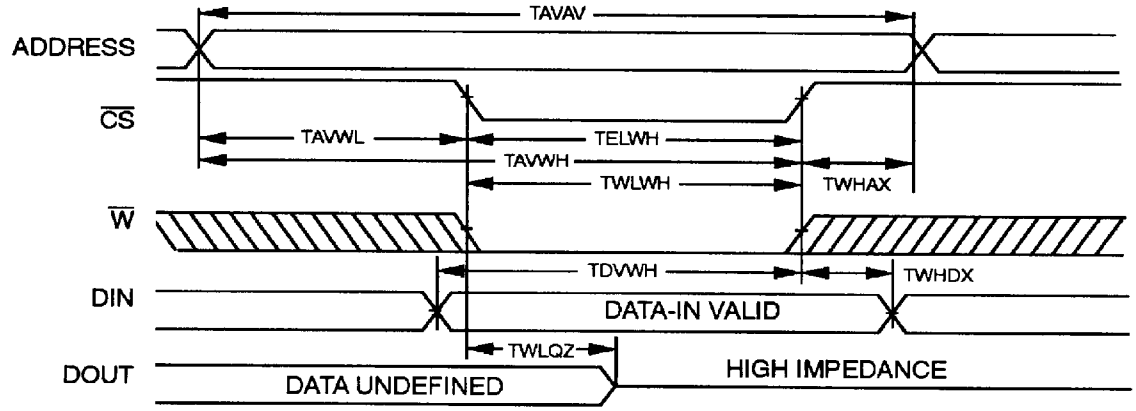
SYMBOL	PARAMETER	M 65698 L/V - 40(*)	M 65698 L/V - 45	M 65698 L/V - 55	UNIT	VALUE
TAVAV	Read cycle time	40	45	55	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	40	50	ns	min
TDVWH	Data set-up time	22	25	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	40	50	ns	min
TWLQZ (11)	Write low to high Z	15	15	20	ns	min
TWLWH	Write pulse width	30	40	50	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	0	ns	min

Notes : 11. Specified with $C_L = 5$ pF (see figure 1b). Guaranteed. Not tested.
(*) Preliminary. Consult sales.

Write Cycle 1 : $\overline{W}$ Controlled (note 12)



Write Cycle 2 : $\overline{CS}$ Controlled (note 12)



Note : 12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms

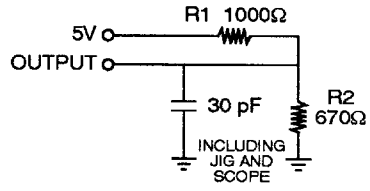


Figure 1 a

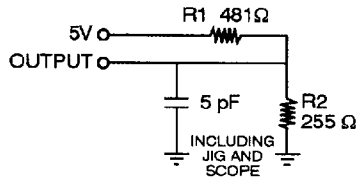


Figure 1 b

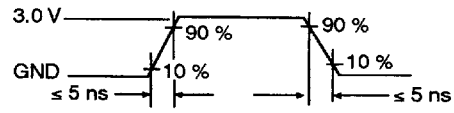
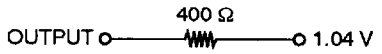


Figure 2

Equivalent to : THEVENIN EQUIVALENT



Read Cycle : Commercial Specification

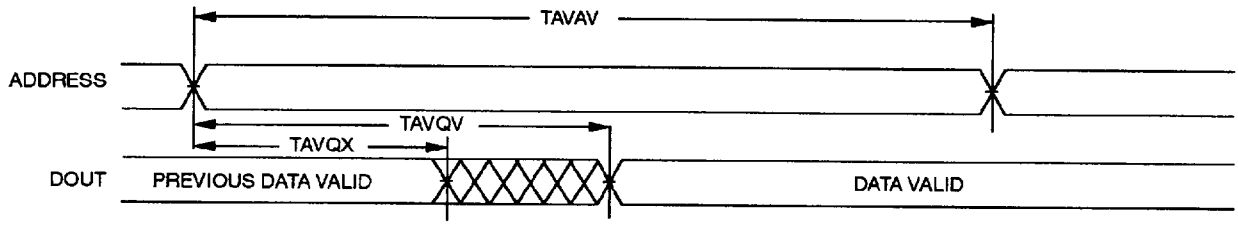
SYMBOL	PARAMETER	M 65698 L/V - 35(*)	M 65698 L/V - 40	M 65698 L/V - 45	M 65698 L/V - 55	UNIT	VALUE
TAVAV	Write cycle time	35	40	45	55	ns	min
TAVQV	Address access time	35	40	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	35	40	45	55	ns	max
TELQX (13)	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ (13)	$\overline{CS}$ high to high Z	20	20	20	20	ns	max

Read Cycle : Industrial and Military Specification

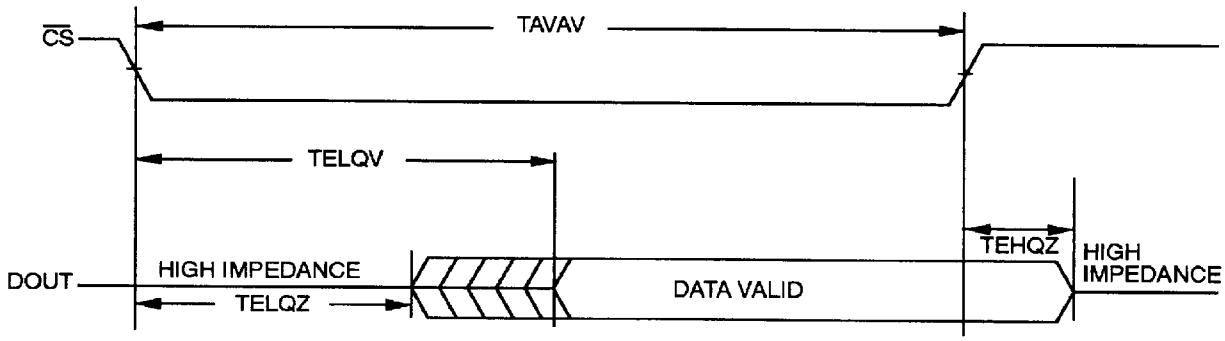
SYMBOL	PARAMETER	M 65698 L/V - 40(*)	M 65698 L/V - 45	M 65698 L/V - 55	UNIT	VALUE
TAVAV	Read cycle time	40	45	55	ns	min
TAVQV	Address access time	40	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	40	45	55	ns	max
TELQX (13)	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ (13)	$\overline{CS}$ high to high Z	20	20	20	ns	max

Notes : 13. Specified with CL = 5 pF (see figure 16). Guaranteed but not tested.
(*) Preliminary. Consult sales.

Read Cycle nb 1 (notes 14, 15)



Read Cycle nb 2 (notes 14, 16)



Notes : 14. W is high for read cycle.
15. Device is continuously selected $\overline{CS}$ = VIL.
16. Address valid prior to or coincident with $\overline{CS}$ transition low.

Ordering Information