BLF6G20-40

Power LDMOS transistor

Rev. 01 — 19 January 2009 Product data sheet

1. Product profile

1.1 General description

40 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1805 to 1880	28	2.5	18.8	15	–46 [1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

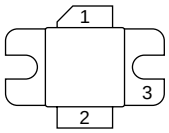
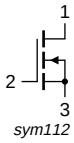
- Typical 2-carrier W-CDMA performance at frequencies of 1805 MHz and 1880 MHz, a supply voltage of 28 V and an I_{Dq} of 360 mA:
  - Average output power = 2.5 W
  - Power gain = 18.8 dB (typ)
  - Efficiency = 15 %
  - ACPR = –46 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1800 MHz to 2000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

sym112

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G20-40	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT608A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	13	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; $P_{L(AV)}$ = 12.5 W	1.7	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 72 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 300 mA	1.70	2.30	2.79	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.5	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	12.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	150	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.6 A	-	5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2.5 A	-	0.2	-	Ω

7. Application information

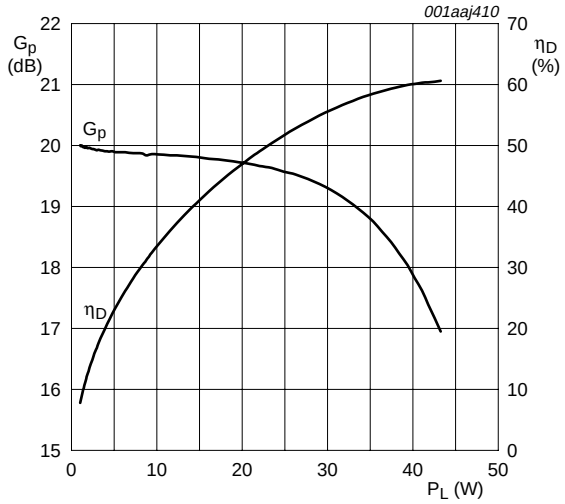
Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH; f_1 = 1802.5 MHz; f_2 = 1807.5 MHz; f_3 = 1872.5 MHz; f_4 = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 360 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 2.5 W	17.5	18.8	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 2.5 W	13	15	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 2.5 W	-	–46	–42	dBc

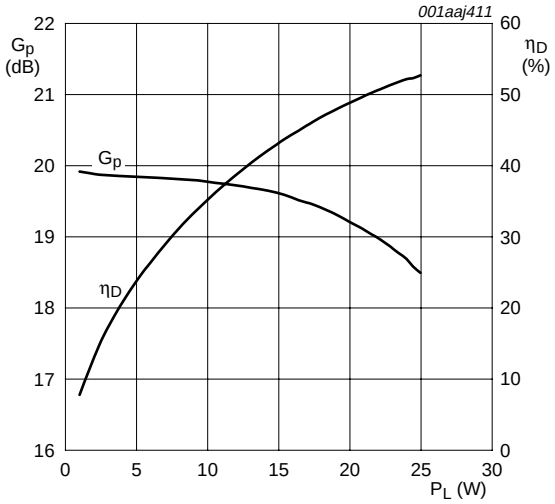
7.1 Ruggedness in class-AB operation

The BLF6G20-40 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 360 mA; P_L = 40 W (CW); f = 1880 MHz.



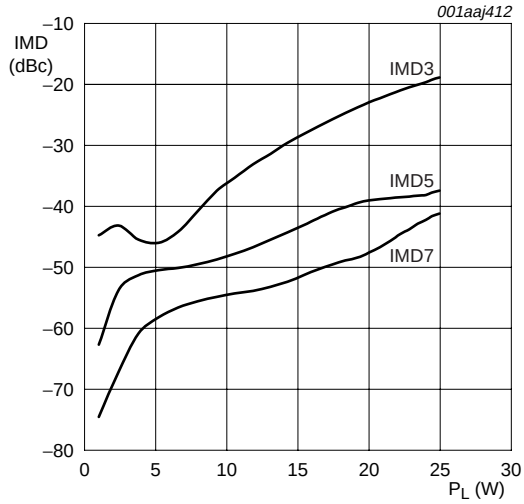
V_{DS} = 28 V; I_{Dq} = 360 mA; f = 1842 MHz.

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



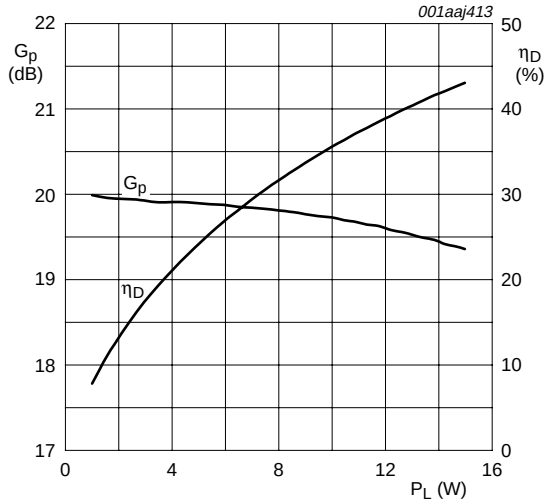
V_{DS} = 28 V; I_{Dq} = 360 mA; f_1 = 1843 MHz; f_2 = 1843.1 MHz.

Fig 2. Two-tone CW power gain and drain efficiency as functions of peak envelope load power; typical values



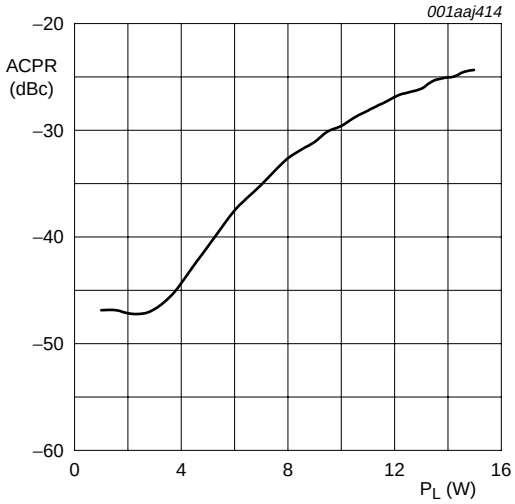
V_{DS} = 28 V; I_{Dq} = 360 mA; f_1 = 1843 MHz; f_2 = 1843.1 MHz.

Fig 3. Two-tone CW intermodulation distortion as a function of peak envelope load power; typical values



V_{DS} = 28 V; I_{Dq} = 360 mA; f_1 = 1840.5 MHz; f_2 = 1845.5 MHz; carrier spacing 5 MHz.

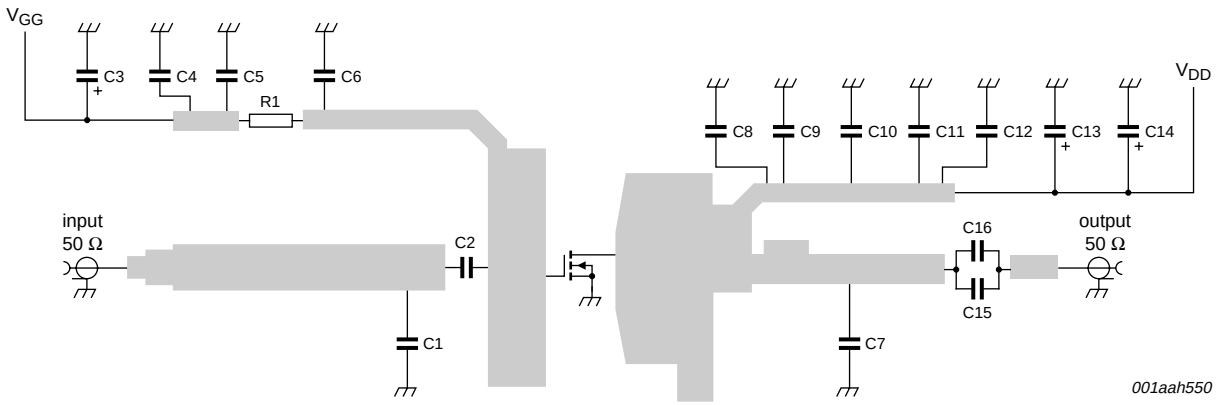
Fig 4. 2-carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 360 mA; f_1 = 1840.5 MHz; f_2 = 1845.5 MHz; carrier spacing 5 MHz.

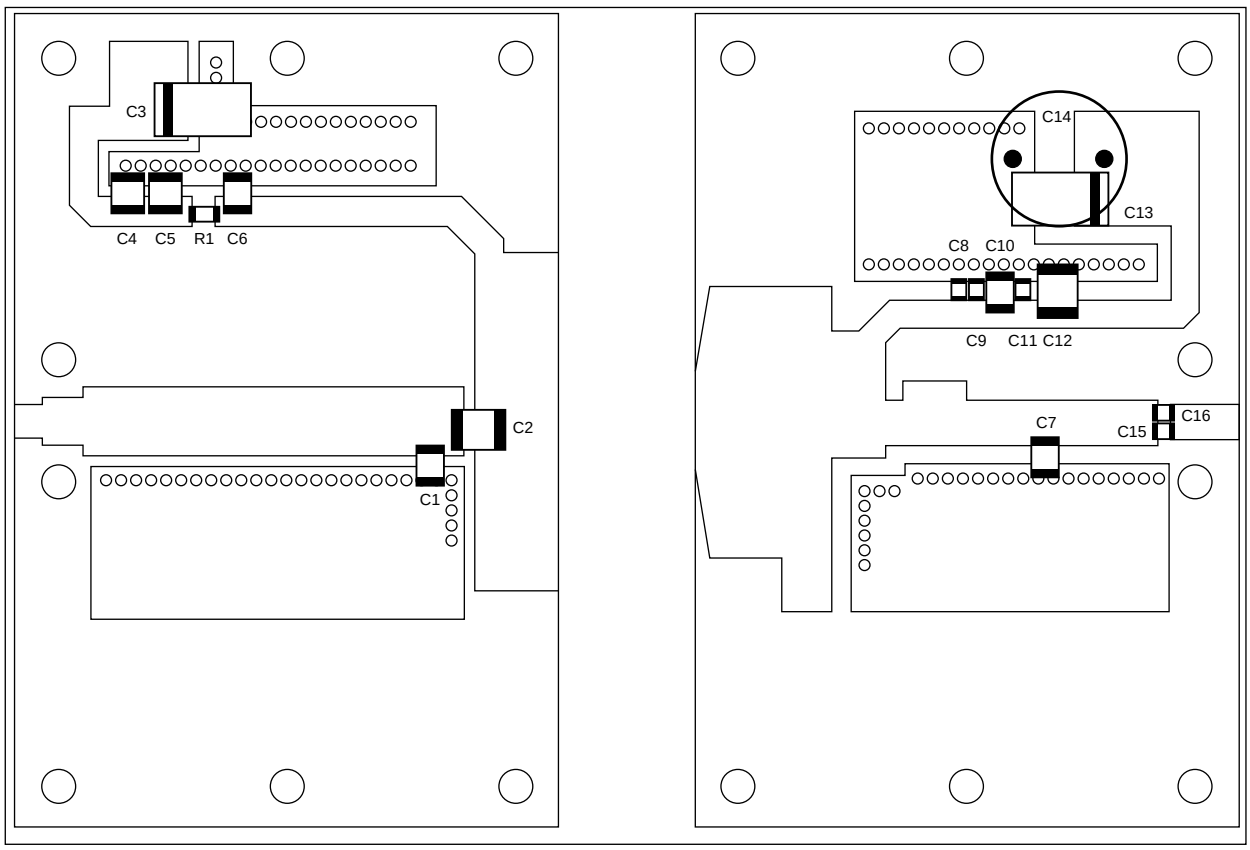
Fig 5. 2-carrier W-CDMA adjacent power channel ratio as function of average load power; typical values

8. Test information



See Table 8 for list of components.

Fig 6. Test circuit for operation at 1805 MHz and 1880 MHz



Striplines are on a double copper-clad Rogers Duroid 5880 Printed-Circuit Board (PCB) (ε_r = 2.2), thickness = 0.79 mm.

See Table 8 for list of components.

Fig 7. Component layout for 1805 MHz and 1880 MHz test circuit

Table 8. List of components

For test circuit, see Figure 6 and Figure 7.

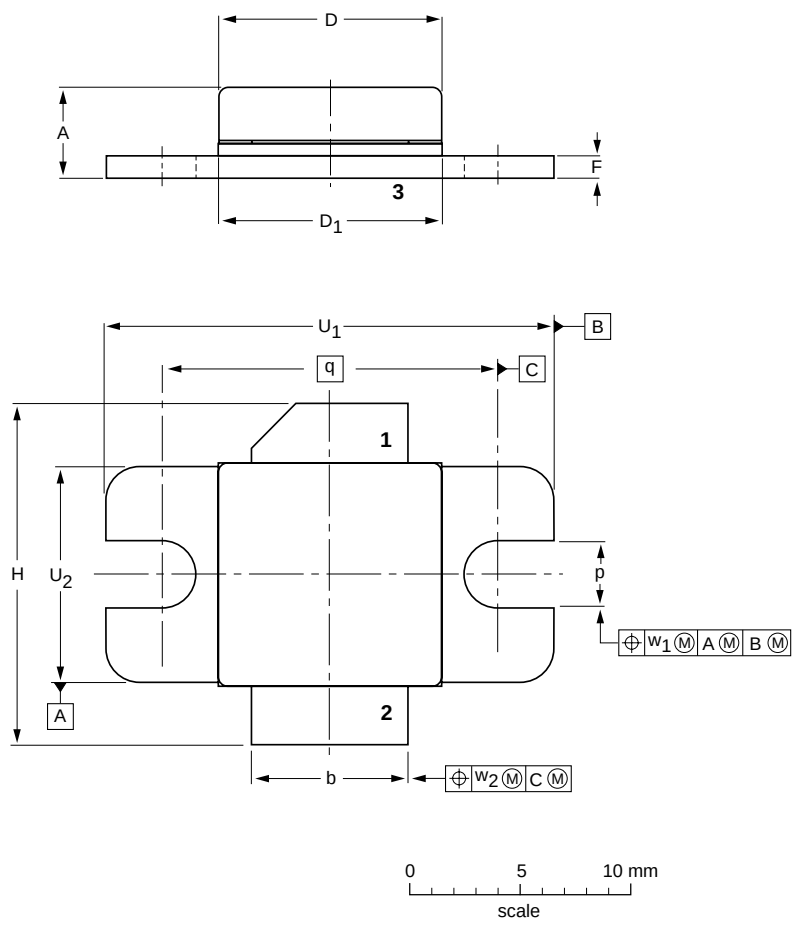
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	0.7 pF	[1]
C2	multilayer ceramic chip capacitor	3.9 pF	[1]
C3, C13	tantalum capacitor	10 µF	
C4, C5	multilayer ceramic chip capacitor	1.5 µF	
C6, C10	multilayer ceramic chip capacitor	10 pF	[1]
C7	multilayer ceramic chip capacitor	1.2 pF	[1]
C8, C9	multilayer ceramic chip capacitor	100 nF	
C11	multilayer ceramic chip capacitor	220 nF	
C12	multilayer ceramic chip capacitor	4.7 µF	
C14	Philips electrolytic capacitor	220 µF, 63 V	
C15, C16	multilayer ceramic chip capacitor	6.8 pF	[2]
R1	Philips chip resistor	5.6 Ω	

[1] American technical ceramics type 100B or capacitor of same quality.

[2] American technical ceramics type 100A or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT608A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.62 3.76	7.24 6.99	0.15 0.10	10.21 10.01	10.29 10.03	10.21 10.01	10.29 10.03	1.14 0.89	15.75 14.73	3.30 2.92	1.70 1.35	15.24	20.45 20.19	9.91 9.65	0.25	0.51
inches	0.182 0.148	0.285 0.275	0.006 0.004	0.402 0.394	0.405 0.395	0.402 0.394	0.405 0.395	0.045 0.035	0.620 0.580	0.130 0.115	0.067 0.053	0.600	0.805 0.795	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT608A						~~01-02-22~~ 02-02-11

Fig 8. Package outline SOT608A

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G20-40_1	20090119	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1	**Product profile**	**1**
1.1	General description	1
1.2	Features	1
1.3	Applications	2
2	**Pinning information**	**2**
3	**Ordering information**	**2**
4	**Limiting values**	**2**
5	**Thermal characteristics**	**2**
6	**Characteristics**	**3**
7	**Application information**	**3**
7.1	Ruggedness in class-AB operation	3
8	**Test information**	**5**
9	**Package outline**	**8**
10	**Abbreviations**	**9**
11	**Revision history**	**9**
12	**Legal information**	**10**
12.1	Data sheet status	10
12.2	Definitions	10
12.3	Disclaimers	10
12.4	Trademarks	10
13	**Contact information**	**10**
14	**Contents**	**11**

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