REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
26 FEBRUARY 1990

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, A/D CONVERTER, 10-BIT SAMPLING, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89698
A	67268	

SHEET 1

DESC FORM 193
SEP 87

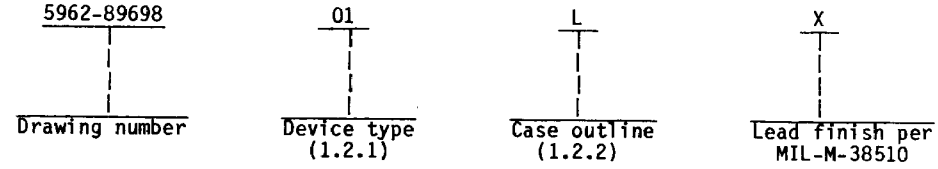
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1442

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7579	10-bit ADC with an (8+2) read interfacing structure
02	AD7580	10-bit ADC with a 10-bit parallel word

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package

1.3 Absolute maximum ratings.

V_{DD} to AGND, DGND	-0.3 V dc to +7.0 V dc
AGND to DGND	-0.3 V dc to V_{DD}
Digital input voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital output voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
CLK input voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
V_{REF} to AGND	-0.3 V dc to V_{DD}
$V_{IN}(\pm)A$, $V_{IN}(\pm)B$ to AGND (see figure 1)	-0.3 V dc to V_{DD} +0.3 V dc
$V_{IN}(\pm)A$ to AGND (see figure 2)	-0.6 V dc to $2V_{DD}$ + 0.6 V dc
$V_{IN}(\pm)A$ to AGND (see figure 3)	V_{DD} - 0.3 V dc to V_{DD} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation at $T_A \leq 75°C$ (P_D) 1/	450 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Derate above T_A = +75°C at 6.0 mW/°C.

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1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.75 V dc to +5.25 V dc
Reference voltage (V_{REF})	+2.5 V
Analog and digital ground voltage (AGND and DGND)	0 V
Clock frequency (f_{CLK})	2.5 MHz
Analog input range (see figure 1):	
Span	V_{REF}
Common mode range	0 V to V_{DD}
Analog input range (see figure 2):	
Span	$2V_{REF}$
Common mode range	0 V to $2V_{DD}$
Analog input range (see figure 3):	
Span	$2V_{REF}$
Common mode range	$-V_{REF}$ to ($2V_{DD}$ - V_{REF})
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 4.

3.2.2 Truth tables. The truth tables shall be as specified on figure 5.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C < T_A < +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Integral nonlinearity 2/	INL		All	1,2,3		±1.0	LSB
Differential nonlinearity 2/	DNL	No missing codes guaranteed over the full temperature range	All	1,2,3		±0.9	LSB
Full scale error 2/	AE		All	1,2,3		±5.0	LSB
Zero code error 2/ 3/	A_{ZCE}	Connected as on figure 1	All	1,2,3		±3.0	LSB
		Connected as on figure 2	All			±3.0	
Power supply rejection 4/	PSR	4.75 V < V_{DD} < 5.25 V	All	1,2,3		±0.5	LSB
Power supply current	I_{DD}	V_{DD} = +5.0 V	All	1,2,3		10	mA
Attenuator input resistance 5/	$R_{IN(AT)}$		All	1,2,3	5.0	15	MΩ
Comparator input resistance	R_{IN} (comp)	Connected as on figure 1	All	1,2,3	10		MΩ
Reference input current	I_{REF}		All	1,2,3		1.5	mA
Digital input low voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, HBEN and CLK HBEN, device 01 only	All	1,2,3		0.8	V
Digital input high voltage	V_{INH}				2.4		
Digital input current	I_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, HBEN, and CLK, V_{IN} = 0 V to V_{DD} HBEN, device 01 only	All	1		±1.0	µA
				2,3		±10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

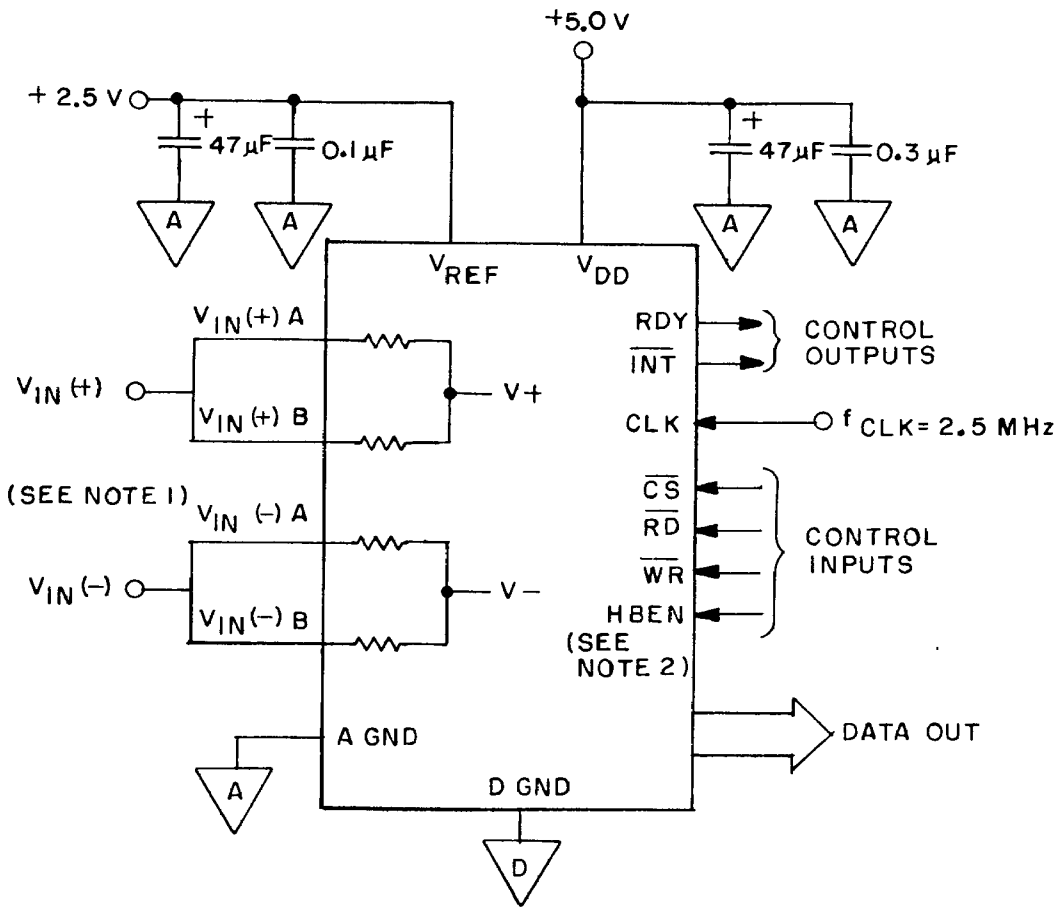
Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Input capacitance 6/	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, HBEN, and CLK see 4.3.1b, $T_A = +25°C$ HBEN, device 01 only.	All	4		10	pF
Digital output low voltage	V_{OL}	DB0 to DB7, I_{SINK} = 1.6 mA	All	1,2,3		0.4	V
Digital output high voltage	V_{OH}	DB0 to DB7, I_{SOURCE} = 400 µA	All	1,2,3	4.0		V
Floating state leakage current	I_{LG}	DB0 - DB7, V_{OUT} = 0 to V_{DD}	All	1,2,3		±10	µA
Floating state output capacitance 6/	C_{OUT}	DB0 - DB7, see 4.3.1b $T_A = +25°C$	All	4		10	pF
Output low voltage	V_{OL}	RDY, INT, I_{SINK} = 1.6 mA	All	1,2,3		0.4	V
Conversion time 7/	T_{CONV}	f_{CLK} = 2.5 MHz, t_{WR} = 100 µs	All	1,2,3	16.9	18.5	µs
Sampling rate 7/	t_{SAMP}		All	7,8		50	kHz
Functional test		See 4.3.1c	All	7,8			
Signal-to-noise ratio 6/ 7/	SNR		All	4,5,6	55		dB
$\overline{CS}$ to $\overline{WR}$ setup time 6/	t_1	See figure 6 8/	All	9,10,11	0		ns
$\overline{WR}$ pulse width	t_2			9	40		ns
				10,11	50		
$\overline{CS}$ to $\overline{WR}$ hold time 6/	t_3			9,10,11	0		ns
$\overline{WR}$ to $\overline{INT}$ propagation delay time 6/	t_4	See figures 6, 8, and 9 9/	All	9		100	ns
				10,11		120	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

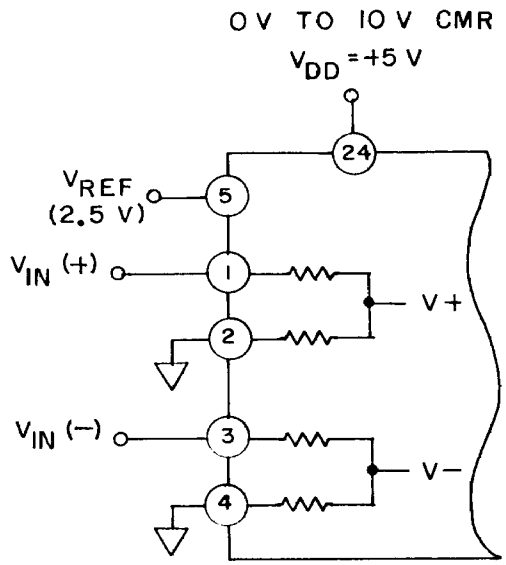
Test	Symbol	Conditions 1/ $-55°C < T_A < +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
$\overline{CS}$ to $\overline{RD}$ setup time 6/	t_5	See figure 7 8/	All	9,10,11	0		ns
$\overline{RD}$ pulse width 6/	t_6		All	9,10,11	t_{12}		ns
$\overline{CS}$ to $\overline{RD}$ hold time 6/	t_7		All	9,10,11	0		ns
HBEN to $\overline{RD}$ setup time	t_8		01	9	20		ns
				10,11	30		
HBEN to $\overline{RD}$ hold time	t_9		01	9,10,11	10		ns
RDY access time 6/	t_{10}	See figures 7, 8, and 9 9/	All	9	110		ns
				10,11	150		
$\overline{RD}$ to $\overline{INT}$ propagation delay time 6/	t_{11}		All	9		100	ns
				10,11		120	
Data access time after $\overline{RD}$	t_{12}		All	9		110	ns
				10,11		150	
Data hold time, RDY hold time	t_{13}	See figures 7 and 10 6/ 10/	All	9	10	65	ns
				10,11	10	90	

1/ V_{DD} = +5.0 V ±5.0%, V_{REF} = +2.5 V, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz, and connected as shown on figure 1, unless otherwise specified.
2/ Specification applies for the three Analog Input Ranges: 0 to V_{DD}, 0 to $2V_{DD}$, $-V_{REF}$ to $(2V_{DD} - V_{REF})$. INL tested using figure 1, DNL tested using figure 2, configuration B.
3/ Zero code error is measured with respect to an ideal first code transition which occurs at 0.5 LSB.
4/ Power supply rejection is tested for full scale error only.
5/ Resistance is measured between $V_{IN}(+)A$, $V_{IN}(+)B$ or $V_{IN}(-)A$, $V_{IN}(-)B$.
6/ Measured only for the initial test and after any process or design changes which may affect these parameters.
7/ These specifications apply for full scale input signals up to 20 kHz.
8/ All input control signals are specified with $t_r = t_f$ = 20 ns (10 percent to 90 percent of +5.0 V) and timed from a voltage level of +1.6 V.
9/ t_4, t_{10}, t_{11} and t_{12} are measured with the load circuits of figures 8 and 9 and defined as the time required for an output to cross 0.8 V or 2.4 V.
10/ t_{13} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 10.

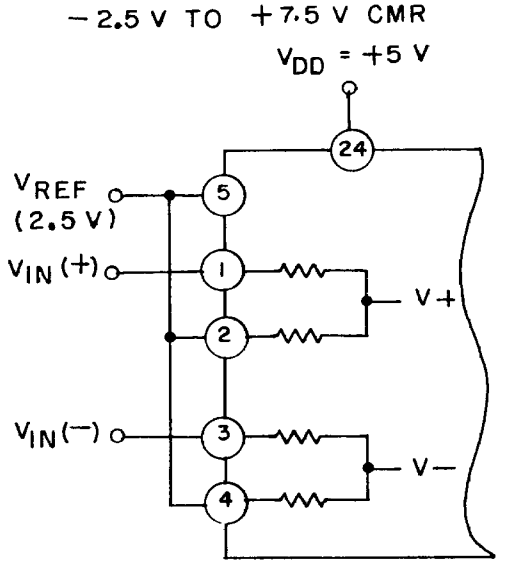


NOTES:
1. $V_{IN}(+)$ must always be equal to or more positive than $V_{IN}(-)$.
2. HBEN input applies only to device type 01.

FIGURE 1. Unipolar 2.5 V operation.



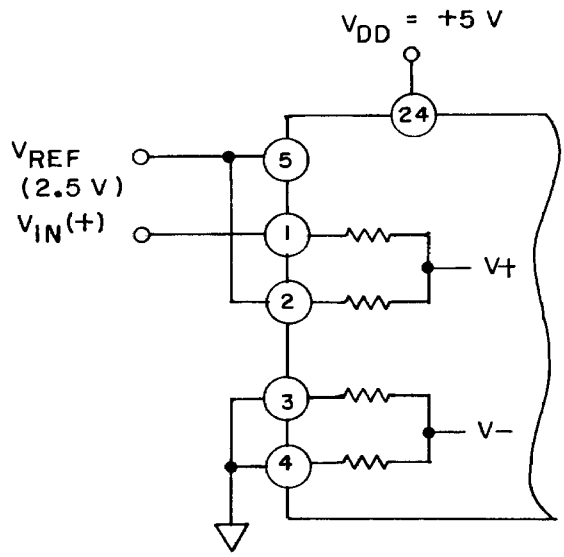
CONFIGURATION A



CONFIGURATION B

NOTES:
1. $V_{IN}(+)$ must always be equal to or more positive than $V_{IN}(-)$.
2. Decoupling and control circuitry are shown on figure 1.

FIGURE 2. 5.0 V span operation.



NOTES:
1. $V_{IN}(+)$ must always be equal to or more positive than $V_{IN}(-)$.
2. Decoupling and control circuitry are as shown on figure 1.

FIGURE 3. Single ended bipolar operation, -2.5 V to +2.5 V.

Device types	01	02
Case outline	L	
Terminal number	Terminal symbol	
1	$V_{IN}(+)A$	$V_{IN}(+)A$
2	$V_{IN}(+)B$	$V_{IN}(+)B$
3	$V_{IN}(-)A$	$V_{IN}(-)A$
4	$V_{IN}(-)B$	$V_{IN}(-)B$
5	V_{REF}	V_{REF}
6	AGND	AGND
7	CS	CS
8	WR	WR
9	RD	RD
10	INT see note	INT see note
11	CLK	CLK
12	DGND	DGND
13	HBEN	RDY see note
14	RDY see note	DBO(LSB)
15	DBO (LSB)	DB1
16	DB1	DB2
17	DB2	DB3
18	DB3	DB4
19	DB4	DB5
20	DB5	DB6
21	DB6	DB7
22	DB7 (MSB)	DB8
23	I.C.	DB9 (MSB)
24	V_{DD}	V_{DD}

NOTES:
1. $\overline{INT}$ and RDY are open-drain outputs and need 3.0 kΩ external pull-up resistors for operation.
2. I.C. = internally connected.

FIGURE 4. Terminal connections.

Device type 01

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	HBEN	Function
1	X	X	X	Not selected
0	1	1	X	Selected, wait for $\overline{WR}$, $\overline{RD}$
0	⊤_⊤	1	X	Start conversion on falling edge of $\overline{WR}$
0	1	0	0	Enable ADC data (8 LSB's), data is right justified
0	1	0	1	Enable ADC data (2 LSB's), data is right justified

Device type 02

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Function
1	X	X	Not selected
0	1	1	Selected, wait for $\overline{WR}$, $\overline{RD}$
0	⊤_⊤	1	Start conversion on falling edge $\overline{WR}$
0	1	0	Enable ADC data (10 bits)

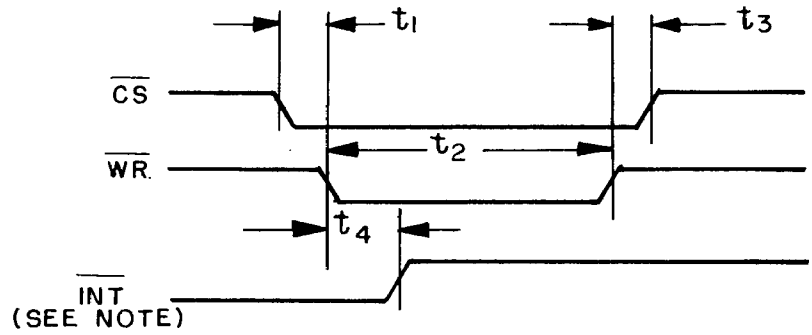
1 = high logic level

0 = low logic level

X = irrelevant

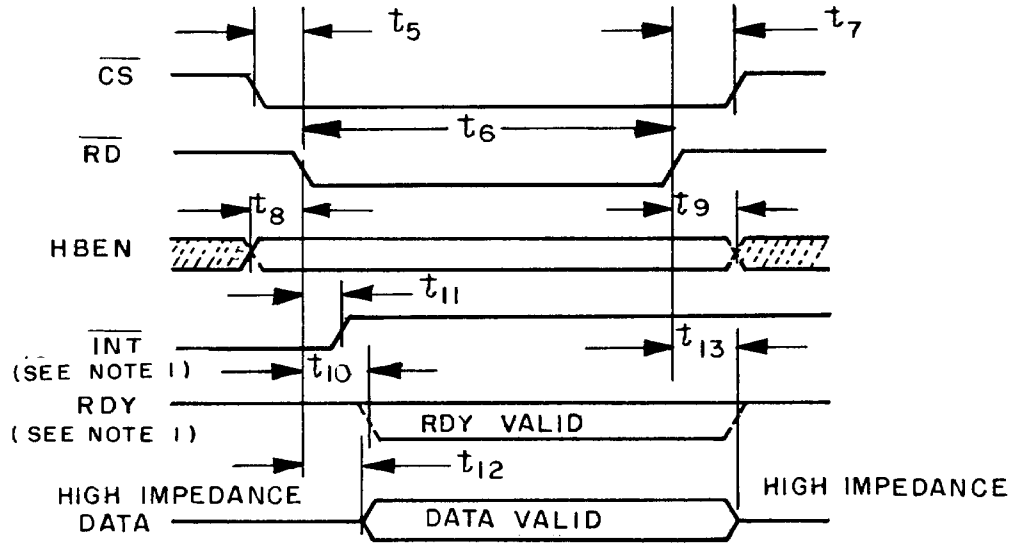
⊤_⊤ = one clock cycle

FIGURE 5. Truth tables.



NOTE: INT has a 3.0 kΩ external pull-up resistor.

FIGURE 6. Start cycle timing diagram.



NOTES:
1. INT and RDY have 3.0 kΩ external pull-up resistors.
2. HBEN applies to device 01 only.

FIGURE 7. Read cycle timing diagram.

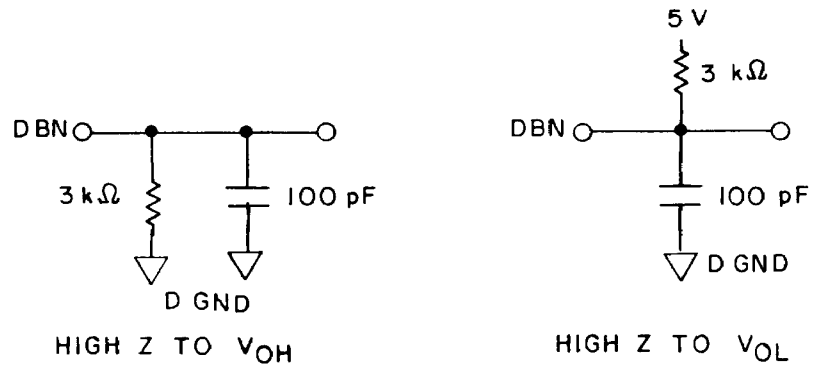


FIGURE 8. Load circuits for access time tests.

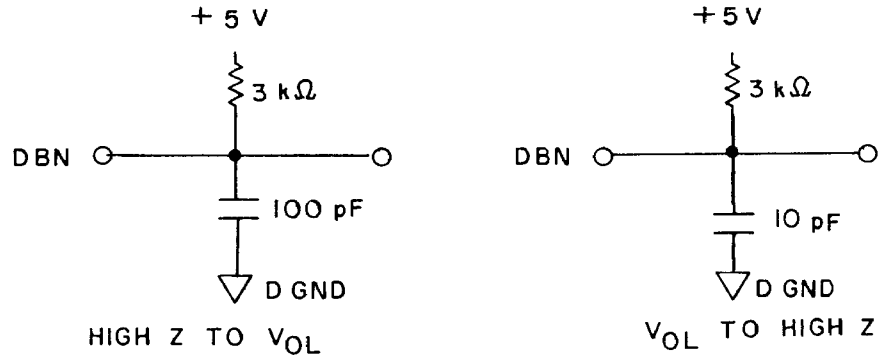


FIGURE 9. Load circuits for $\overline{INT}$ propagation delays.

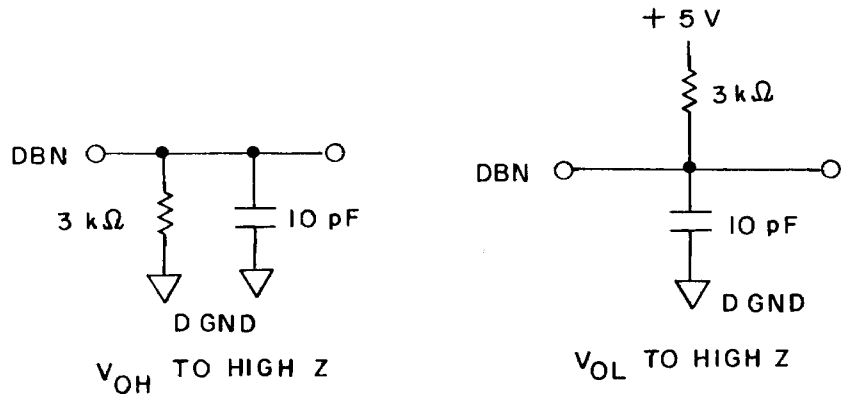


FIGURE 10. Load circuits for output float delay.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8
Group A test requirements (method 5005)	1,2,3,4,5,6,7, 8,9,10**,11**
Group C and D end-point electrical parameters (method 5005)	1

*PDA applies to subgroup 1.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be measured only for the initial test and after process or design changes which may affect the parameters specified in table I.

c. Subgroup 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8969801LX	24355	AD7579SQ/883B
5962-8969802LX	24355	AD7580SQ/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887