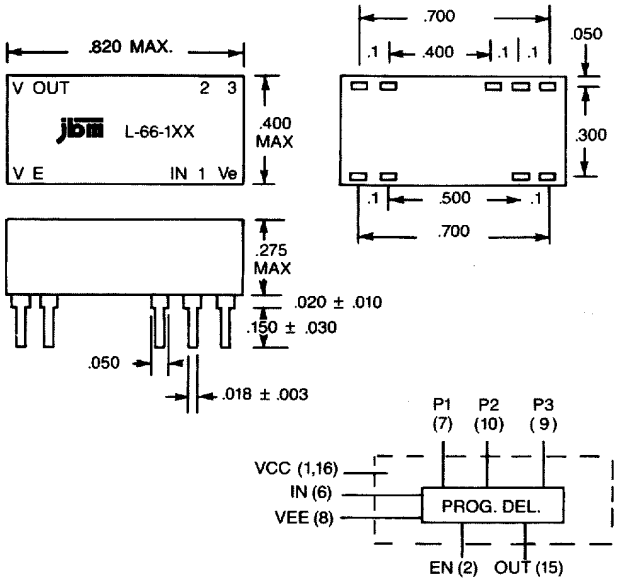
T-47-17

L-66-100 SERIES

10K ECL 3 Bit Programmables



DELAY LINE CHARACTERISTICS

Input Characteristics:

V_{IH} Logic "1" Input Voltage . . . . . –.98V Min.
V_{IL} Logic "0" Input Voltage . . . . . –1.63V Max.
I_{IH} Logic "1" Input Current . . . . . 265 μA Max.
I_{IL} Logic "0" Input Current . . . . . .5μA Max.

Output Characteristics:

V_{OH} Logic "1" Output Voltage . . . . . –.96V Min.
V_{OL} Logic "0" Output Voltage . . . . . –1.65V Max.

I_{CC} . . . . . 55mA Max.
V_{EE} . . . . . –5.2V ±5%

Environment:

Operating temperature . . . . . –30°C to +85°C
Storage temperature . . . . . –55°C to +125°C

Test Conditions:

Delays at 25°C with PWI @ 2× Programmed Delay with –5.2V TO Vee.

DELAY SPECIFICATIONS IN (ns) NANOSECONDS

Program Pins 3		0	1	2	3	4	5	6	7	Tol. of	Delay Time	Delay Time	Maximum Delay
Part	2	0	0	1	1	0	0	1	1	Prog.	Per	Step	Nominal
Numbers	1	0	1	0	1	0	1	0	1	Delay	Step	Tol.	Ref. IN
L-66-121		3 ± 1 ns	1	2	3	4	5	6	7	± 1 ns	1 ns	± .3 ns	10 ns
L-66-122		3 ± 1 ns	2	4	6	8	10	12	14	± 1 ns	2 ns	± .4 ns	17 ns
L-66-123		3 ± 1 ns	3	6	9	12	15	18	21	± 1 ns	3 ns	± .5 ns	24 ns
L-66-124		3 ± 1 ns	4	8	12	16	20	24	28	± 1.5 ns	4 ns	± .5 ns	31 ns
L-66-125		3 ± 1 ns	5	10	15	20	25	30	35	± 1.7 ns	5 ns	± .5 ns	38 ns
L-66-126		3 ± 1 ns	6	12	18	24	30	36	42	± 2 ns	6 ns	± .6 ns	45 ns
L-66-127		3 ± 1 ns	7	14	21	28	35	42	49	± 2.4 ns	7 ns	± .7 ns	52 ns
L-66-128		3 ± 1 ns	8	16	24	32	40	48	56	± 2.6 ns	8 ns	± .8 ns	59 ns
L-66-129		3 ± 1 ns	9	18	27	36	45	54	63	± 3.1 ns	9 ns	± .9 ns	66 ns
L-66-130		3 ± 1 ns	10	20	30	40	50	60	70	± 3.5 ns	10 ns	± 1 ns	73 ns
L-66-131		3 ± 1 ns	12	24	36	48	60	72	84	± 4.2 ns	12 ns	± 1.2 ns	87 ns

*Steps 1 to 7 Reference to Zero