Triple video driver hybrid amplifiers CR6728A; CR6728AB

FEATURES

- Transition times (10 to 90%) with 45 V (p-p) swing and C_L = 10 pF:
  rise time (typ.) 2.5 ns
  fall time (typ.) 2.1 ns
- Low power consumption:
  11 W with 25 MHz square wave
- Minimum small signal bandwidth:
  140 MHz at 1 V (p-p) or 120 MHz at 40 V (p-p)
- Very fast slew rate: 16000 V/µs
- Internal smearing compensation
- Excellent grey-scale linearity
- Unconditional stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Cathode-ray tube (CRT) drivers in high-resolution colour monitors.

DESCRIPTION

The CR6728A and CR6728AB are triple video driver hybrid amplifier modules encapsulated in the SOT347 and SOT347B packages respectively. The difference between the packages is the lead length.

PINNING

PIN	DESCRIPTION
1, 5, 9	V_S
2	input 1
3, 7, 11	ground
4	output 1
6	input 2
8	output 2
10	input 3
12	output 3

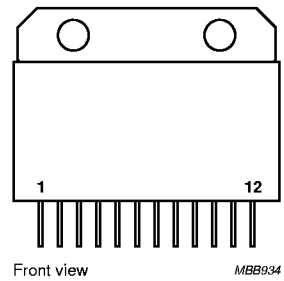


Fig.1 Simplified outline SOT347.

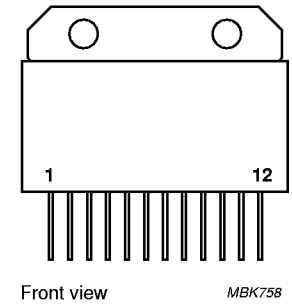


Fig.2 Simplified outline SOT347B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	supply voltage (DC)	–	90	V
T_{mb}	operating mounting base temperature	−20	+110	°C
T_{stg}	storage temperature	−40	+125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	supply voltage (DC)	–	70	V
T_{mb}	operating mounting base temperature	−20	+100	°C
T_{stg}	storage temperature	−40	+125	°C

CHARACTERISTICS

V_S = 65 V; T_{mb} = 25 °C; C_L = 10 pF; output swing = 45 V (p-p) with 32.5 V DC offset (see Fig.4); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	supply current	open input and open output	105	120	135	mA
P_{tot}	total power dissipation	25 MHz sine wave	–	11	11.5	W
t_r	rise time transient response	10 to 90%; note 1	–	2.5	3.1	ns
t_f	fall time transient response	10 to 90%; note 1	–	2.1	2.5	ns
BW	small signal bandwidth	between −3 dB points; note 2	140	150	–	MHz
V_{tilt}	low frequency tilt voltage	10 kHz square wave	–	1.3	1.5	V
V_{os}	overshoot voltage (rise and fall time)	adjustable by C1 and C2; see Fig. 4	–	3	10	%
NLN	non-linearity	V_O = 15 to 75 V	–	2	5	%
A_V	DC voltage gain	50 Ω source; note 3	11.2	12.4	13.6	
V_G	insertion gain	50 Ω source; note 4	160	180	200	

Notes

1. Input signal is a 100 kHz square wave of 3.78 V (p-p) with 1.28 V DC offset (50 Ω source), without R_{level}.
2. Sinewave output signal: 1 V (p-p).
3. Measured V_O/V_I at input test circuit.
4. Measured V_O/V_I at input module.

APPLICATION NOTES

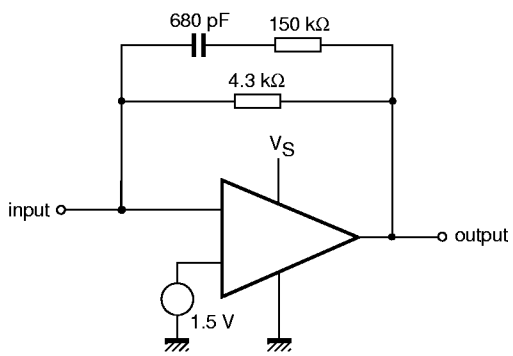
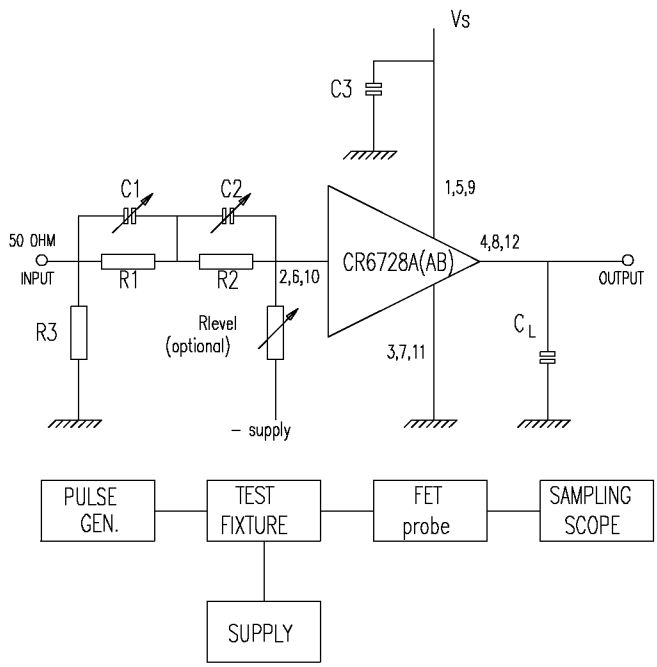


Fig.3 Block diagram; single amplifier.



Speed-up circuit (R1, C1; R2, C2) ensures flat gain over the whole frequency range.

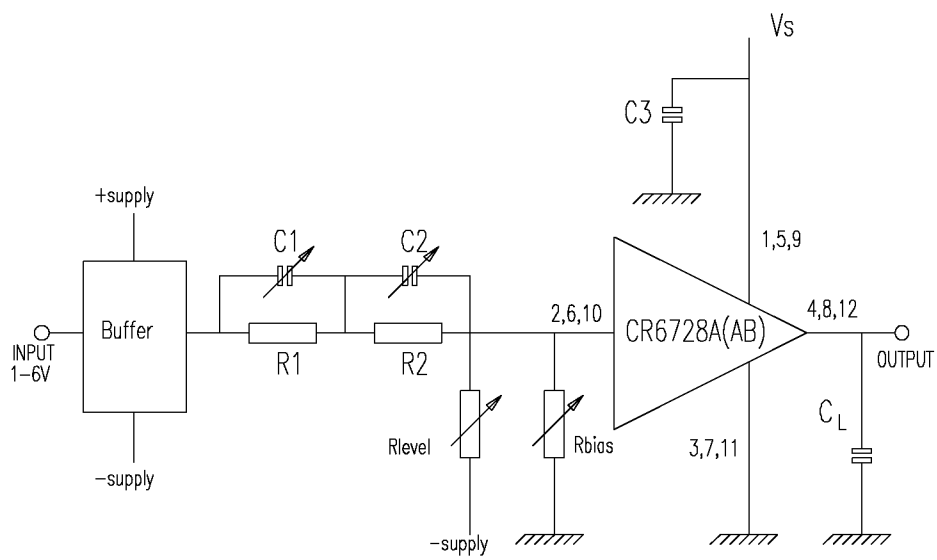
Fig.4 Test circuit and block diagram of the CR6728A and CR6728AB.

Components used in test circuit (see Fig.4)

COMPONENT	DESCRIPTION	VALUE
C1	variable capacitor	10 to 160 pF (typ. 50 pF)
C2	variable capacitor	10 to 160 pF (typ. 82 pF)
C3	chip capacitor and electrolytic capacitor	10 nF and 4.7 μF; 160 V
R1	resistor	275 Ω
R2	resistor	62 Ω
R3	resistor	50 Ω

Test equipment (see Fig.4)

EQUIPMENT	TYPE DESCRIPTION
Pulse generator	Le Croy; model 9210 with unit 9211
	Philips; model PM5785B (125 MHz) with internal DC offset
Power supply	Philips; model PE1542, 80 V
FET probe	Philips; model PM8943, attenuation 100 : 1
Sampling oscilloscope	Tektronix; model 11801B, sampling head SD26



R_{level} and R_{bias} are intended to achieve the required output level and to optimize the frequency smearing performance.
R_{level} has to be adjusted to the required output level (approx. 2kΩ at V_S = – 12 V).
R_{bias} has to be tuned for the best high frequency smearing performance (200 MHz burst at R_{bias} = 300 to 1000 Ω).

Fig.5 Application test circuit of the CR6728A and CR6728AB.

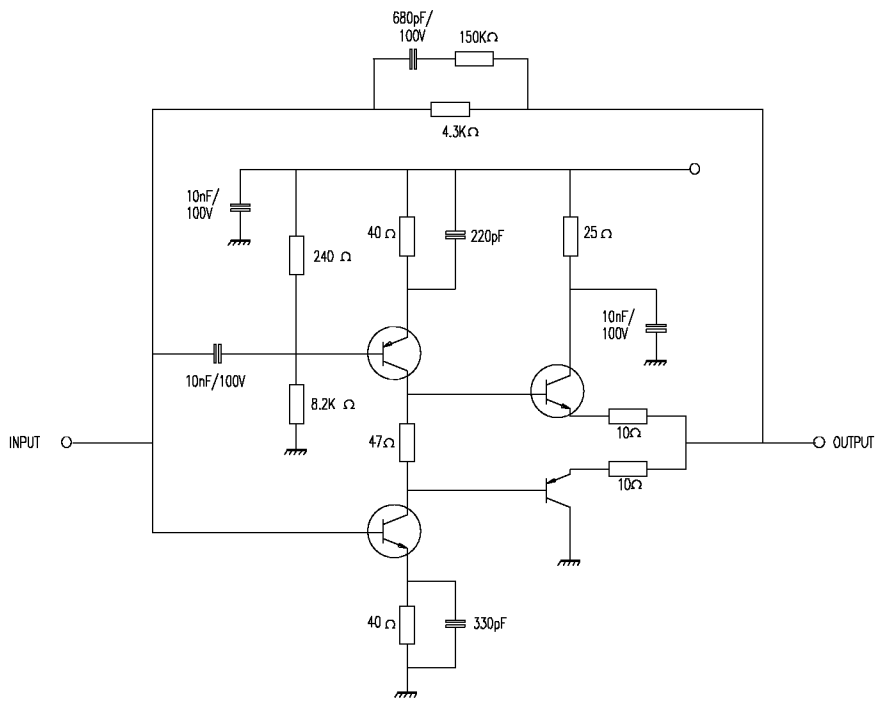
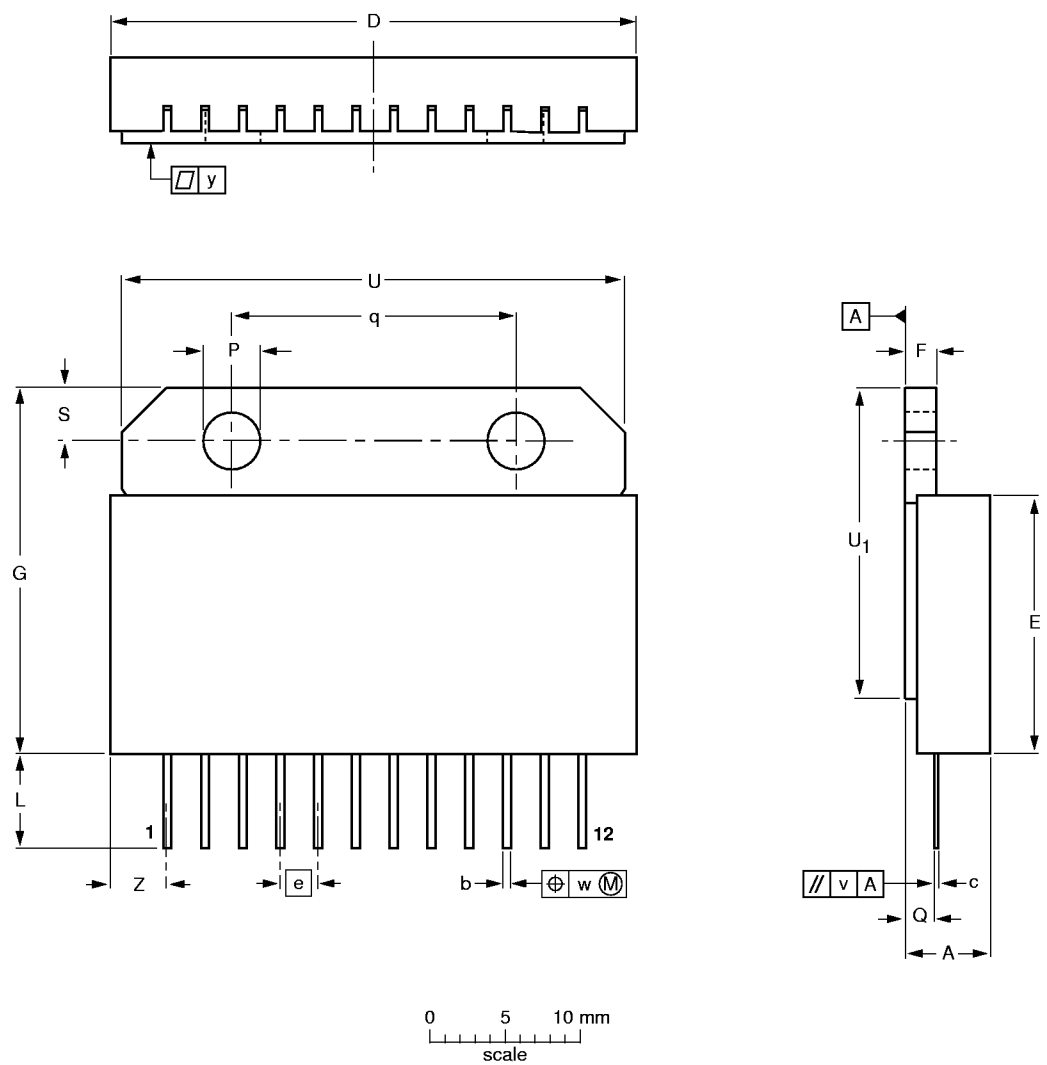


Fig.6 Internal circuit diagram of the CR6728A and CR6728AB.

PACKAGE OUTLINE

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads **SOT347**



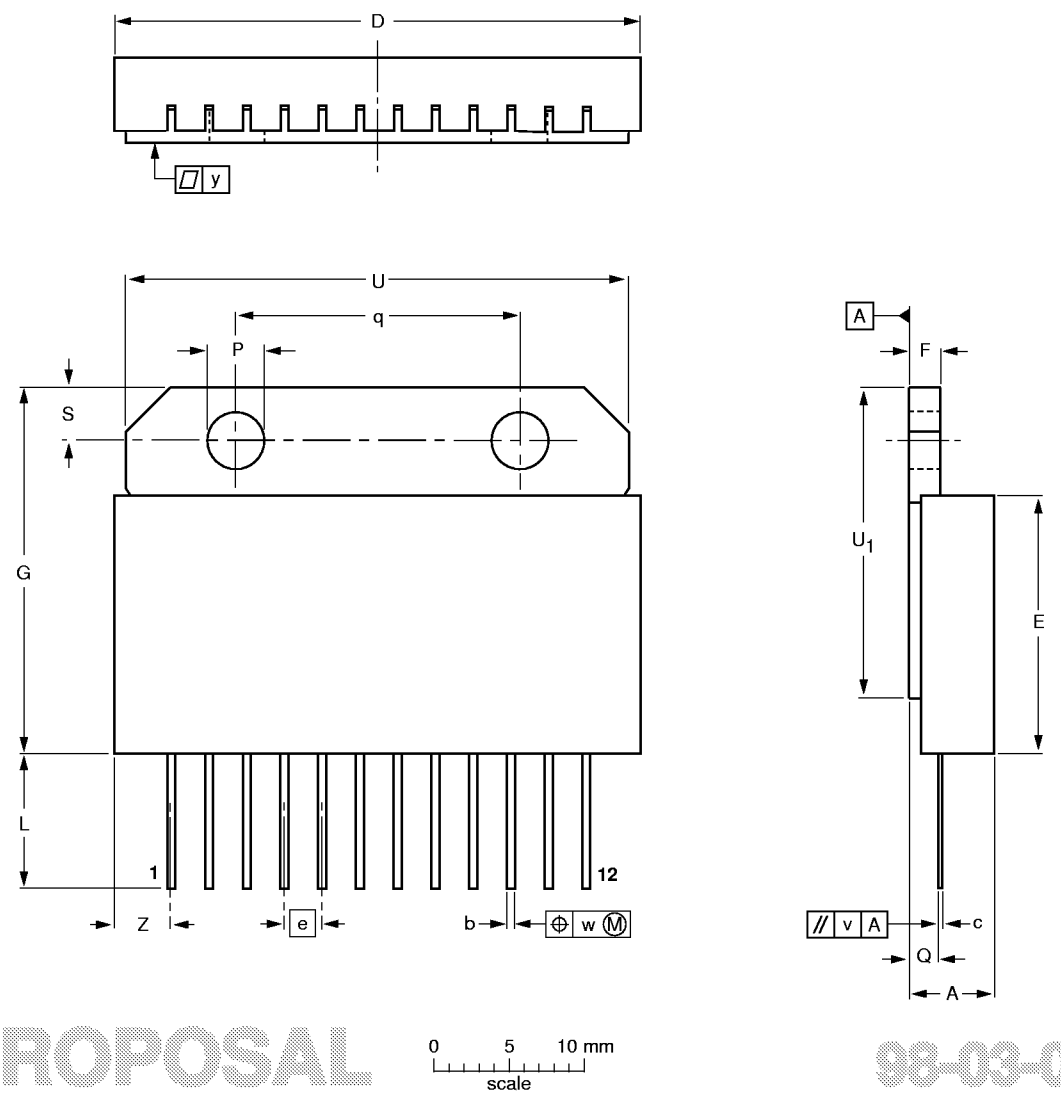
DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L min.	P	Q	q	S	U	U_1	v	w	y	Z max.
mm	6.0 5.6	0.51 0.38	0.25	36.2 35.8	18.2 17.8	2.54	2.0	25.5 24.5	6	4.15 3.85	1.8	19	3.5 3.4	34.4 34.0	22.2 21.8	0.3	0.25	0.1	4.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT347						97-06-28

PACKAGE OUTLINE

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads **SOT347B**



PROPOSAL

0 5 10 mm
scale

98-03-03

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L min.	P	Q	q	S	U	U_1	v	w	y	Z max.
mm	6.0 5.6	0.51 0.38	0.25	36.2 35.8	18.2 17.8	2.54	2.0	25.5 24.5	9	4.15 3.85	1.8	19	3.5 3.4	34.4 34.0	22.2 21.8	0.3	0.25	0.1	4.1

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	IEC	JEDEC	EIAJ			
SOT347B						98-03-03