REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Sheet 6, changed I_{CC2} from 85 mA to 90 mA. Sheet 17, changed R/$\overline{W}_R$ and $\overline{CE}_R$ from L to X for function Reset Left $\overline{INT}_L$ Flag. Added device types 09-12. - glg	99-04-19	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Jeff Bowling

CHECKED BY
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APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-04-13

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 4K X 16 DUAL PORT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-91662**

SHEET **1** OF **31**

DSCC FORM 2233
APR 97

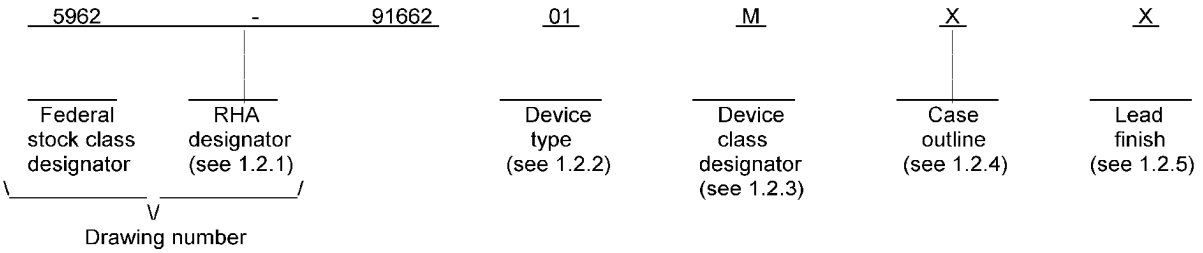
5962-E138-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 (RHA) designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Data retention	Access time
01	7024	4K X 16 Dual port SRAM	No	70 ns
02	7024	4K X 16 Dual port SRAM	Yes	70 ns
03	7024	4K X 16 Dual port SRAM	No	55 ns
04	7024	4K X 16 Dual port SRAM	Yes	55 ns
05	7024	4K X 16 Dual port SRAM	No	45 ns
06	7024	4K X 16 Dual port SRAM	Yes	45 ns
07	7024	4K X 16 Dual port SRAM	No	35 ns
08	7024	4K X 16 Dual port SRAM	Yes	35 ns
09	7024	4K X 16 Dual port SRAM	No	25 ns
10	7024	4K X 16 Dual port SRAM	Yes	25 ns
11	7024	4K X 16 Dual port SRAM	No	20 ns
12	7024	4K X 16 Dual port SRAM	Yes	20 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-PN	84	Pin grid array
Y	See figure 1	84	Flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
DC output current	50 mA
Maximum power dissipation (P_D)	2.2 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	20°C/W
Maximum junction temperature (T_J)	+150°C 3/
DC input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 4/
DC output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 4/
Output voltage applied in high Z state	-0.5 V dc to V_{CC} + 0.5 V dc

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH})	2.2 V dc to 6.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to GND unless otherwise specified.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.
5/ When a value is available, it shall be provided.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's)
MIL-HDBK-780 - Standard Microcircuit Drawings

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OL} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Input leakage current 1/	I_{LI}	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	1, 2, 3	01,03,05, 07,09,11		10	µA
				02,04,06, 08,10,12		5	
Output leakage current	I_{LO}	V_{CC} = 5.5 V, $\overline{CE} = V_{IH}$, V_{OUT} = 0 V to V_{CC}	1, 2, 3	01,03,05, 07,09,11		10	µA
				02,04,06, 08,10,12		5	
Dynamic operating current (both ports active)	I_{CC1}	V_{CC} = 5.5 V, $\overline{CE} \le V_{IL}$, Outputs Open, $\overline{SEM} \ge V_{IH}$, f = f_{MAX} 2/	1, 2, 3	01		390	mA
				02		330	
				03		395	
				04		335	
				05,07		400	
				06,08		340	
				09,11		410	
				10,12		350	
Standby current (both ports - TTL level inputs)	I_{CC2}	V_{CC} = 5.5 V, $\overline{CE}_R = \overline{CE}_L \ge V_{IH}$, $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$, f = f_{MAX} 2/	1, 2, 3	01,03,05, 07,09,11		90	mA
				02,04,06, 08,10,12		65	
Standby current (one port - TTL level inputs)	I_{CC3}	V_{CC} = 5.5 V, $\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, active port outputs open, f = f_{MAX} 2/ $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	1, 2, 3	01,03,05, 07,09,11		290	mA
				02,04,06, 08,10,12		250	
Full standby current (both ports - all CMOS level inputs)	I_{CC4}	V_{CC} = 5.5 V, Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2 V $V_{IN} \ge V_{CC}$ - 0.2 V or $V_{IN} \le 0.2$ V, f = 0 3/ $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2 V	1, 2, 3	01,03,05, 07,09,11		30	mA
				02,04,06, 08,10,12		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Full standby current (one port - all CMOS level inputs)	I_{CC5}	V_{CC} = 5.5 V, One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2 V $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2 V $V_{IN} \ge V_{CC}$ - 0.2 V or $V_{IN} \le 0.2$ V Active port outputs open, $f = f_{MAX}$ 2/	1, 2, 3	01,03,05, 07,09,11		260	mA
				02,04,06, 08,10,12		215	
Data retention voltage	V_{DR}	V_{CC} = 2.0 V, $\overline{CE} \ge V_{CC}$ - 0.2 V, $V_{IN} \ge V_{CC}$ - 0.2 V or $\le$ 0.2 V	1, 2, 3	02,04,06, 08,10,12	2.0		V
Data retention current	I_{CC6}		1, 2, 3	02,04,06, 08,10,12		4	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.0 V, f = 1MHz, T_A = 25°C, see 4.4.1e	4	All		11	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, V_{CC} = 5.0 V, f = 1MHz, T_A = 25°C, see 4.4.1e	4	All		11	pF
Functional testing		See 4.4.1c	7, 8A, 8B	All			
Chip deselect to data retention time 4/	t_{CDR}	V_{CC} = 2 V, $\overline{CE} \ge V_{CC}$ - 0.2 V, $V_{IN} \ge V_{CC}$ - 0.2 V or $\le$ 0.2 V, see figures 4 and 5 5/	9, 10, 11	02,04,06, 08,10,12	0		ns
Operation recovery time 4/	t_R		9, 10, 11	02,04,06, 08,10,12	t_{AVAV} 6/		ns
Read cycle time	t_{AVAV}	See figures 4 and 5 5/	9, 10, 11	01,02	70		ns
				03,04	55		
				05,06	45		
				07,08	35		
				09,10	25		
				11,12	20		
Address access time	t_{AVQV}		9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	
				09,10		25	
				11,12		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable access time 7/	t_{ELQV}	See figures 4 and 5 5/	9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	
				09,10		25	
				11,12		20	
Byte enable access time 7/	t_{ABE}		9, 10, 11	01,02		70	ns
				03,04		55	
				05,06		45	
				07,08		35	
				09,10		25	
				11,12		20	
Output enable access time	t_{OLQV}		9, 10, 11	01,02		35	ns
				03,04		30	
				05,06		25	
				07,08		20	
				09,10		13	
				11,12		12	
Output hold from address change	t_{AVQX}		9, 10, 11	All	3		ns
Output enable to output active 4/	t_{OLQX}	See figures 4 and 5 8/	9, 10, 11	01-06	5		ns
				07-12	3		
Output disable to output inactive 4/	t_{OHQZ}		9, 10, 11	01,02		30	ns
				03,04		25	
				05,06		20	
				07-10		15	
				11,12		12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to power up time 4/	t_{ELPU}	See figures 4 and 5 5/	9, 10, 11	All	0		ns
Chip disable to power down time 4/	t_{EHPD}		9, 10, 11	All		50	ns
Semaphore flag update pulse (OE or SEM)	t_{SOP}		9, 10, 11	All	15		ns
Write cycle time	t_{AVAV}		9, 10, 11	01,02	70		ns
				03,04	55		
				05,06	45		
				07,08	35		
				09,10	25		
				11,12	20		
Chip enable to end of write 9/	t_{ELWH}		9, 10, 11	01,02	50		ns
				03,04	45		
				05,06	40		
				07,08	30		
				09,10	20		
				11,12	15		
Address valid to end of write	t_{AVWH}		9, 10, 11	01,02	50		ns
				03,04	45		
				05,06	40		
				07,08	30		
				09,10	20		
				11,12	15		
Address set-up time 9/	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width	t_{WLWH}		9, 10, 11	01,02	50		ns
				03,04	40		
				05,06	35		
				07,08	30		
				09,10	20		
				11,12	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write recovery time	t_{WHAX}	See figures 4 and 5 5/	9, 10, 11	All	0		ns
Data valid to end of write	t_{DVWH}		9, 10, 11	01,02	40		ns
				03,04	30		
				05-08	25		
				09-12	15		
Data hold time 10/	t_{WHDX}		9, 10, 11	All	0		ns
Write enable to output inactive	t_{WLQZ}	See figures 4 and 5 4/ 8/	9, 10, 11	01,02		30	ns
				03,04		25	
				05,06		20	
				07-10		15	
				11,12		12	
Output active from end of write 10/	t_{WHQX}		9, 10, 11	All	0		ns
$\overline{SEM}$ flag write to read time	t_{SWRD}	See figures 4 and 5 5/	9, 10, 11	All	10		ns
$\overline{SEM}$ flag contention window	t_{SPS}		9, 10, 11	All	10		ns
$\overline{BUSY}$ access time from address match	t_{BAA}	$M/\overline{S}$ = H See figures 4 and 5 4/	9, 10, 11	01-04		45	ns
				05-08		35	
				09-12		20	
$\overline{BUSY}$ disable time from address not matched	t_{BDA}		9, 10, 11	01-04		40	ns
				05-08		30	
				09-12		20	
$\overline{BUSY}$ access time from chip enable low	t_{BAC}		9, 10, 11	01-04		40	ns
				05-08		30	
				09-12		20	
$\overline{BUSY}$ disable time from chip enable high	t_{BDC}		9, 10, 11	01-04		35	ns
				05-08		25	
				09-12		17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Arbitration priority set-up time 11/	t_{APS}		9, 10, 11	All	5		ns
$\overline{\text{BUSY}}$ disable to valid data 12/	t_{BDD}		9, 10, 11	All		12/	ns
$\overline{\text{BUSY}}$ input to write 13/	t_{WB}	$\overline{M/S}$ = L See figures 4 and 5 4/	9, 10, 11	All	0		ns
Write hold after $\overline{\text{BUSY}}$ 14/	t_{WH}		9, 10, 11	All	25		ns
Write pulse to data delay	t_{WDD}		9, 10, 11	01,02		95	ns
				03,04		80	
				05,06		70	
				07,08		60	
				09,10		50	
				11,12		45	
Write data valid to read data delay	t_{DDD}		9, 10, 11	01,02		80	ns
				03,04		65	
				05,06		55	
				07,08		45	
				09-12		35	
Interrupt set time	t_{INS}		9, 10, 11	01,02		50	ns
				03,04		40	
				05,06		35	
				07,08		30	
				09-12		20	
Interrupt reset time	t_{INR}		9, 10, 11	01,02		50	ns
				03,04		40	
				05,06		35	
				07,08		30	
				09-12		20	

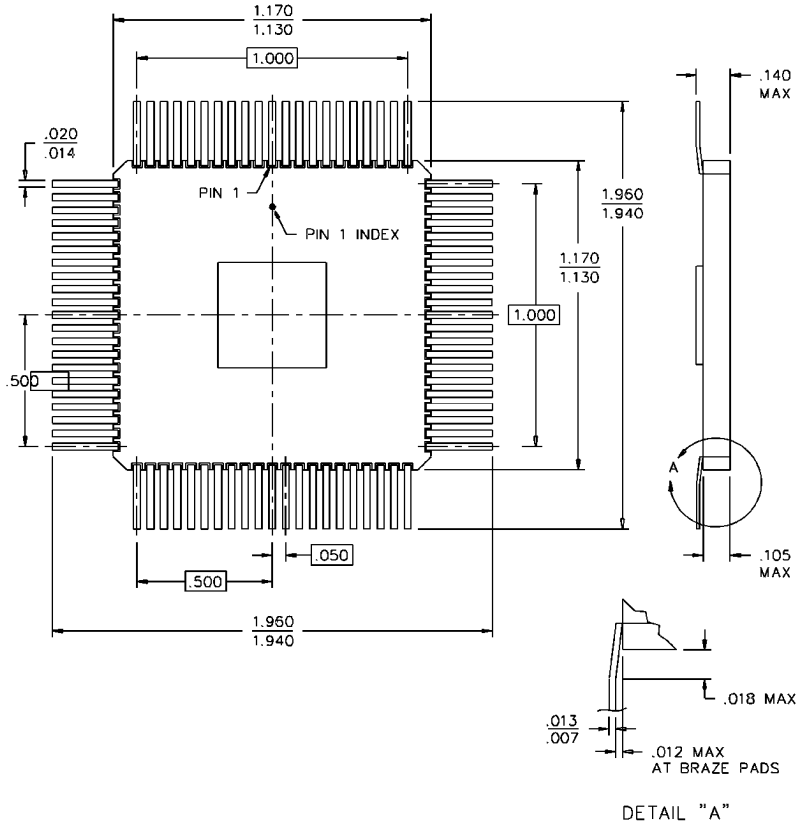
See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

1/ At $V_{CC} \leq 2.0$ V input leakages are undefined.
2/ At f_{MAX}, address and data inputs (except $\overline{OE}$) are cycling at the maximum frequency of read cycle of $1/t_{AVAV}$, and using AC test conditions of input levels of GND to 3 V.
3/ f = 0 Hz means no address or control lines change.
4/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ AC measurements assume transition times $\leq$ 5 ns, input levels from ground to 3.0 V, timing reference levels of 1.5 V, and the output load in figure 4, circuit A.
6/ t_R reference to t_{AVAV} refers to read cycle.

7/ To access RAM: $\overline{CE}$ = L, $\overline{SEM}$ = H, $\overline{UB}$ or $\overline{LB}$ = L.
8/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 4, circuit B.
9/ To access RAM: $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H. To access semaphore: $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{ELWH} time.
10/ The specification for t_{WHDX} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{WHDX} and t_{WHQX} values will vary over voltage and temperature, the actual t_{WHDX} will always be smaller than the actual t_{WHQX}.
11/ To ensure that the earlier of the two ports wins.
12/ t_{BDD} is a calculated parameter and is greater of 0, $t_{WDD} - t_{DVWH}$(actual) or $t_{WDD} - t_{WLWH}$(actual).
13/ To ensure that the write cycle is inhibited during contention.
14/ To ensure that a write cycle is completed after contention.

Case Y



Inches	Millimeters	Inches	Millimeters
.007	0.18	.140	3.56
.012	0.30	.500	12.70
.013	0.33	1.000	25.40
.014	0.36	1.130	28.70
.018	0.46	1.170	29.72
.020	0.51	1.940	49.28
.050	1.27	1.960	49.78
.105	2.67		

NOTES:
1. All dimensions are in inches.
2. BSC - Basic lead spacing between centers.

FIGURE 1. Case outline.

Device types	All		
Case outline	X		
Terminal number	Terminal 1/ 2/ symbol	Terminal number	Terminal 1/ 2/ symbol
A1	I/O_{8R}	F9	V_{CC}
A2	I/O_{6R}	F10	$\overline{UB}_L$
A3	I/O_{5R}	F11	$\overline{OE}_L$
A4	I/O_{3R}	G1	$\overline{CE}_R$
A5	I/O_{1R}	G2	$\overline{UB}_R$
A6	I/O_{0R}	G3	$\overline{SEM}_R$
A7	I/O_{15L}	G9	$R/\overline{W}_L$
A8	I/O_{13L}	G10	$\overline{CE}_L$
A9	I/O_{11L}	G11	$\overline{SEM}_L$
A10	I/O_{10L}	H1	NC
A11	I/O_{7L}	H2	A_{11R}
B1	I/O_{11R}	H10	NC
B2	I/O_{9R}	H11	$\overline{LB}_L$
B3	I/O_{7R}	J1	A_{10R}
B4	I/O_{4R}	J2	A_{8R}
B5	I/O_{2R}	J5	A_{0R}
B6	GND	J6	GND
B7	I/O_{14L}	J7	$\overline{BUSY}_L$
B8	I/O_{12L}	J10	A_{9L}
B9	I/O_{9L}	J11	A_{11L}
B10	I/O_{8L}	K1	A_{9R}
B11	I/O_{5L}	K2	A_{6R}
C1	I/O_{12R}	K3	A_{5R}
C2	I/O_{10R}	K4	A_{2R}
C5	V_{CC}	K5	$\overline{INT}_R$
C6	GND	K6	M/S
C7	V_{CC}	K7	A_{0L}
C10	I/O_{6L}	K8	A_{3L}
C11	I/O_{4L}	K9	A_{6L}
D1	I/O_{14R}	K10	A_{8L}
D2	I/O_{13R}	K11	A_{10L}
D10	I/O_{3L}	L1	A_{7R}
D11	I/O_{2L}	L2	A_{4R}
E1	$\overline{OE}_R$	L3	A_{3R}
E2	I/O_{15R}	L4	A_{1R}
E3	GND	L5	$\overline{BUSY}_R$
E9	GND	L6	A_{1L}
E10	I/O_{1L}	L7	$\overline{INT}_L$
E11	I/O_{0L}	L8	A_{2L}
F1	$\overline{LB}_R$	L9	A_{4L}
F2	$R/\overline{W}_R$	L10	A_{5L}
F3	GND	L11	A_{7L}

1/ All V_{CC} pins must be connected to power supply.
2/ All GND pins must be connected to ground supply.

FIGURE 2. Terminal connections.

Device types	All		
Case outline	Y		
Terminal number	Terminal 1/ 2/ symbol	Terminal number	Terminal 1/ 2/ symbol
1	V_{CC}	43	GND
2	$\overline{OE}_L$	44	$\overline{SEM}_R$
3	I/O_{0L}	45	$\overline{CE}_R$
4	I/O_{1L}	46	$\overline{UB}_R$
5	GND	47	$\overline{LB}_R$
6	I/O_{2L}	48	NC
7	I/O_{3L}	49	A_{11R}
8	I/O_{4L}	50	A_{10R}
9	I/O_{5L}	51	A_{9R}
10	I/O_{6L}	52	A_{8R}
11	I/O_{7L}	53	A_{7R}
12	I/O_{8L}	54	A_{6R}
13	I/O_{9L}	55	A_{5R}
14	I/O_{10L}	56	A_{4R}
15	I/O_{11L}	57	A_{3R}
16	I/O_{12L}	58	A_{2R}
17	I/O_{13L}	59	A_{1R}
18	GND	60	A_{0R}
19	I/O_{14L}	61	$\overline{INT}_R$
20	I/O_{15L}	62	$\overline{BUSY}_R$
21	V_{CC}	63	M/S
22	GND	64	GND
23	I/O_{0R}	65	$\overline{BUSY}_L$
24	I/O_{1R}	66	$\overline{INT}_L$
25	I/O_{2R}	67	A_{0L}
26	V_{CC}	68	A_{1L}
27	I/O_{3R}	69	A_{2L}
28	I/O_{4R}	70	A_{3L}
29	I/O_{5R}	71	A_{4L}
30	I/O_{6R}	72	A_{5L}
31	I/O_{7R}	73	A_{6L}
32	I/O_{8R}	74	A_{7L}
33	I/O_{9R}	75	A_{8L}
34	I/O_{10R}	76	A_{9L}
35	I/O_{11R}	77	A_{10L}
36	I/O_{12R}	78	A_{11L}
37	I/O_{13R}	79	NC
38	I/O_{14R}	80	$\overline{LB}_L$
39	GND	81	$\overline{UB}_L$
40	I/O_{15R}	82	$\overline{CE}_L$
41	$\overline{OE}_R$	83	$\overline{SEM}_L$
42	$R/\overline{W}_R$	84	$R/\overline{W}_L$

1/ All V_{CC} pins must be connected to power supply.
2/ All GND pins must be connected to ground supply.

FIGURE 2. Terminal connections - Continued.

Non-contention read/write control

Inputs 1/						Outputs		Mode
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected: Power Down
L	L	X	L	H	H	$DATA_{IN}$	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

1/ A_{0L}-$A_{11L} \neq A_{0R}$-A_{11R}

Semaphore read/write control

Inputs						Outputs		Mode
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
H	1/	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Semaphore Flag
X	1/	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L	-	-	Not Allowed
L	X	X	X	L	L	-	-	Not Allowed

1/ Rising Edge of Signal

FIGURE 3. Truth tables.

Interrupt flag 1/

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{11L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{11R}	$\overline{INT}_R$	
L	L	X	FFF	X	X	X	X	X	L 2/	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	FFF	H 3/	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L 3/	L	L	X	FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	FFE	H 2/	X	X	X	FFE	X	Reset Left $\overline{INT}_L$ Flag

1/ Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2/ If $\overline{BUSY}_L$ = L, then no change.
3/ If $\overline{BUSY}_R$ = L, then no change.

Address busy arbitration 1/

Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	A_{OL}-A_{11L} A_{OR}-A_{11R}	$\overline{BUSY}_L$ 1/	$\overline{BUSY}_R$ 1/	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	2/	2/	Write Inhibit 3/

1/ $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $BUSY_X$ outputs are push pull, not open drain outputs. On slaves the $BUSY_X$ input internally inhibits writes.
2/ L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $BUSY_L$ or $BUSY_R$ = Low will result. $BUSY_L$ and $BUSY_R$ outputs cannot be low simultaneously.
3/ Writes to the left port are internally ignored when $BUSY_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $BUSY_R$ outputs are driving low regardless of actual logic level on the pin.

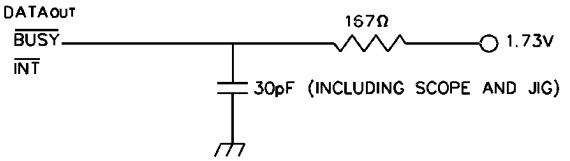
FIGURE 3. Truth tables - continued.

Example of Semaphore Procurement Sequence 1/

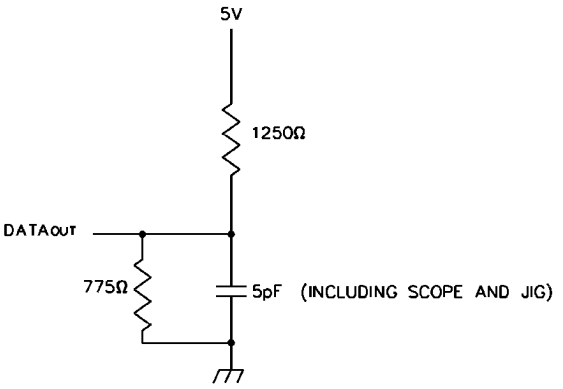
Functions	D_0-D_{15} Left	D_0-D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

1/ This table denotes a sequence of events for only one of the eight semaphores.

FIGURE 3. Truth tables - continued.



Circuit A

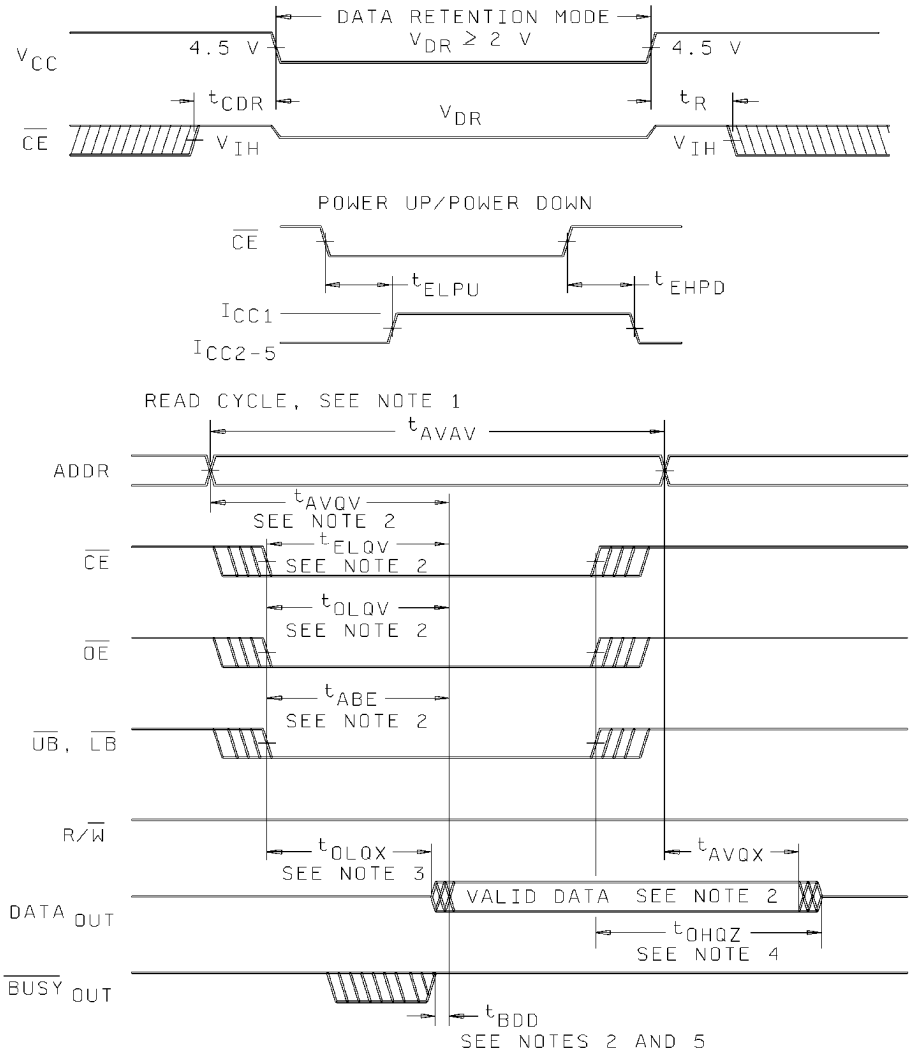


Circuit B (for t_{OLQX}, t_{OHQZ}, t_{WLQZ} and t_{WHQX})

AC test conditions

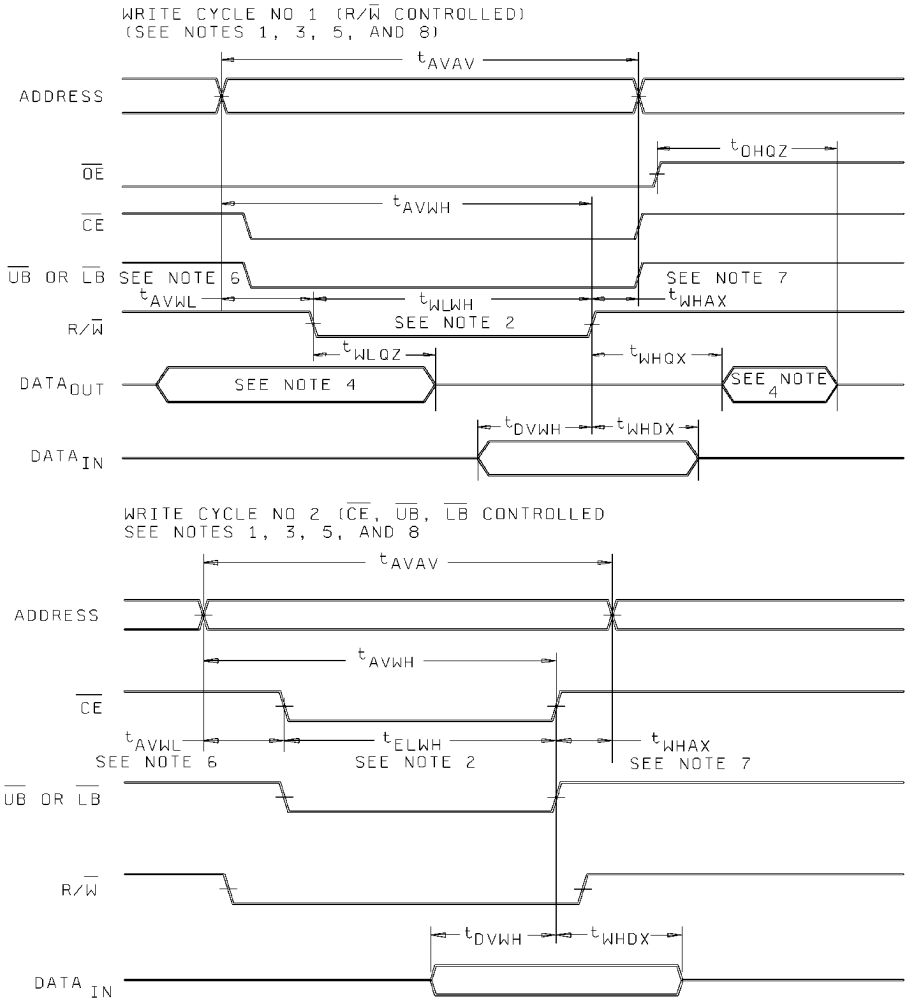
Input pulse levels	GND to 3.0 V
Input rise and fall times (t_r, t_f)	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuits.



Notes on read operation:
1. SEM = H.
2. Start of valid data depends on which timing becomes effective last, t_{ABE}, t_{OLQV}, t_{ELQV}, t_{AVQV}, t_{BDD}.
3. Timing depends on which signal is asserted last, OE, CE, LB, or UB.
4. Timing depends on which signal is de-asserted first, OE, CE, LB, or UB.
5. t_{BDD} delay is required only in case where opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.

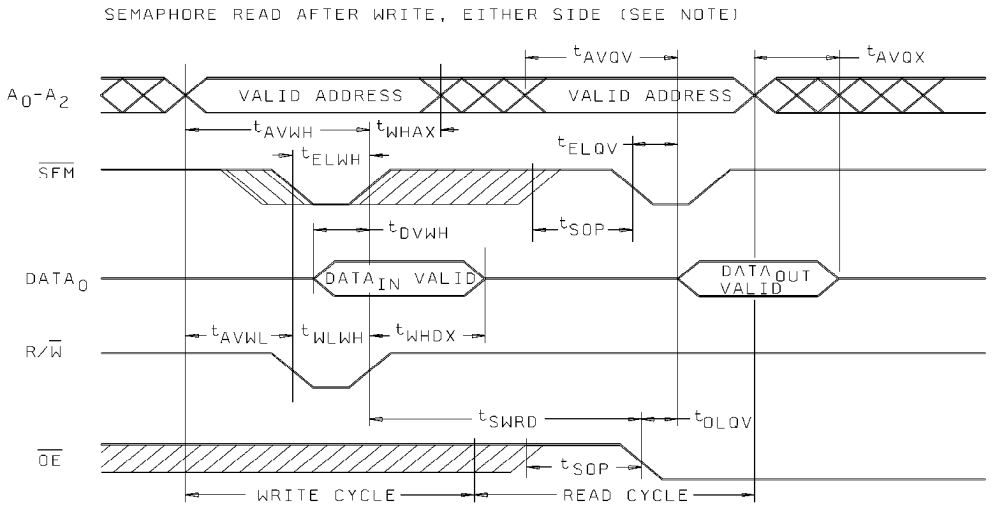
FIGURE 5. Timing waveforms.



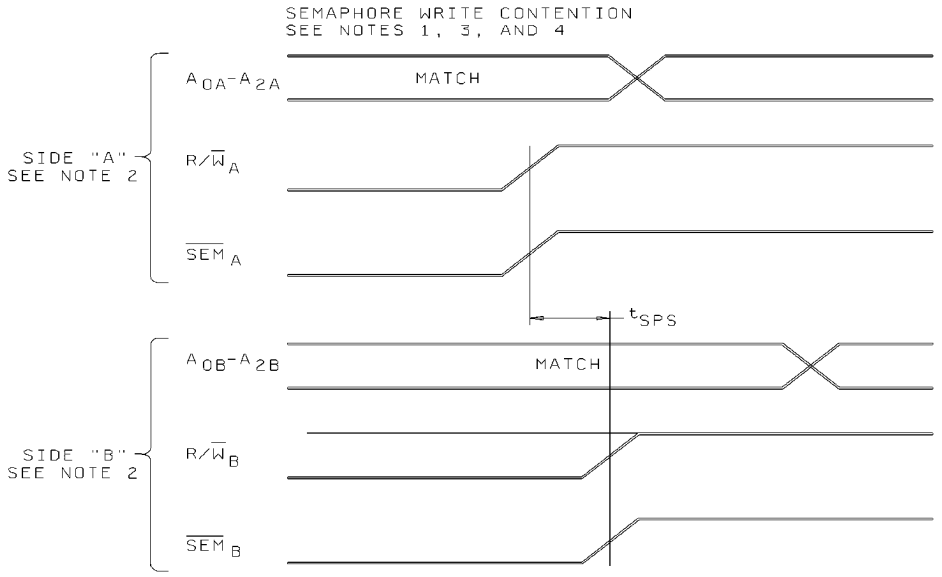
Notes on write cycle:

1. R/W must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/W for memory array writing cycle.
3. t_{WHAX} is measured from the earlier of $\overline{CE}$ or R/W (or $\overline{SEM}$ or R/W) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/W low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If OE is low during R/W controlled write cycle, the write pulse width must be the larger of t_{WLWH} or ($t_{WLQZ} + t_{DVWH}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DVWH}. If $\overline{OE}$ is high during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

FIGURE 5. Timing waveforms - continued.

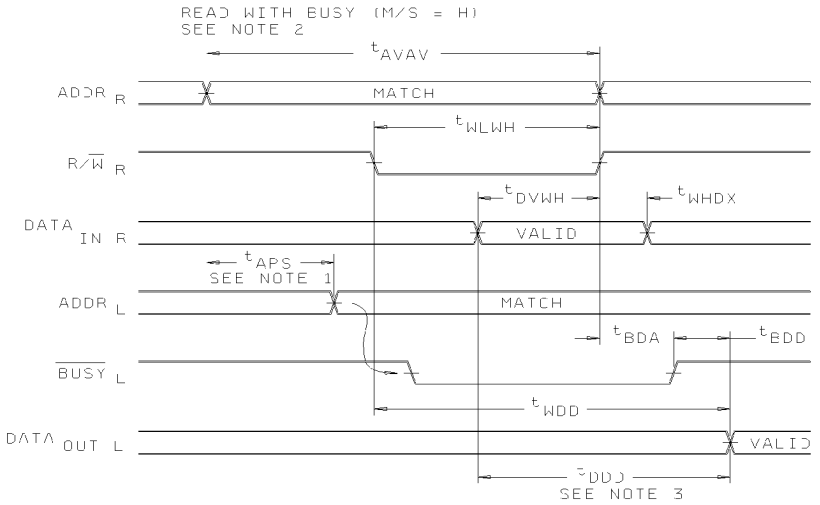


Note: $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

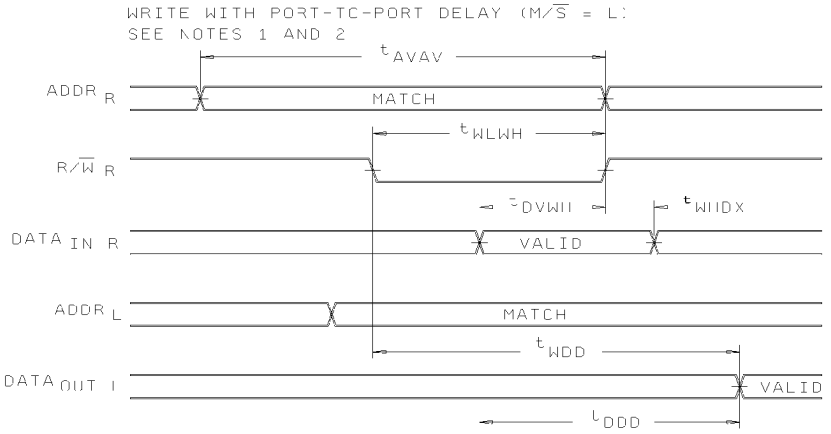


Notes:
1. $D_{OR} = D_{OL}$, $\overline{CE}_R = \overline{CE}_L$ = H, semaphore flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/W_A or SEM_A going high to R/W_B or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FIGURE 5. Timing waveforms - continued.



1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L = \overline{CE}_R = L$.
3. $\overline{OE}$ = L for the reading port.



1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L = \overline{CE}_R = L$.

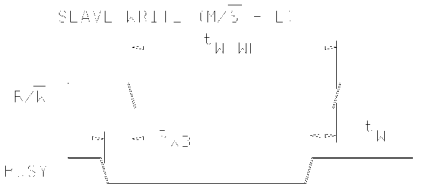
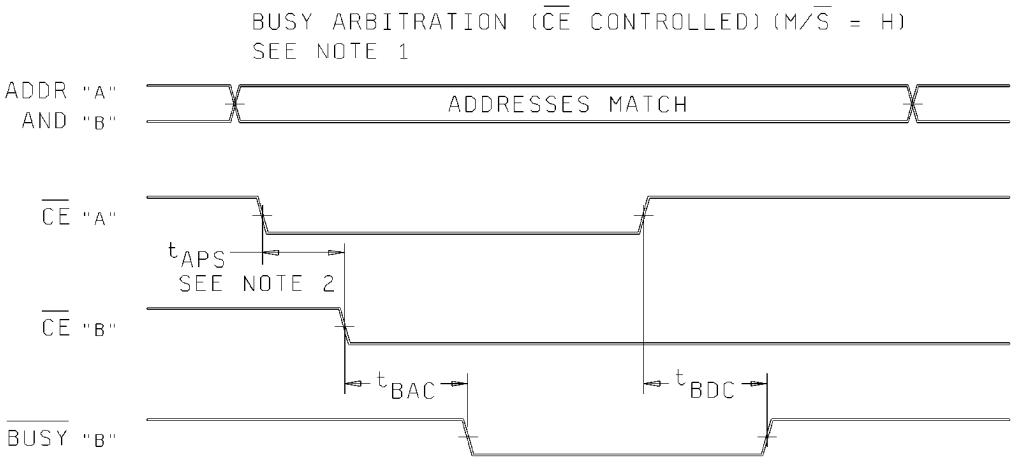
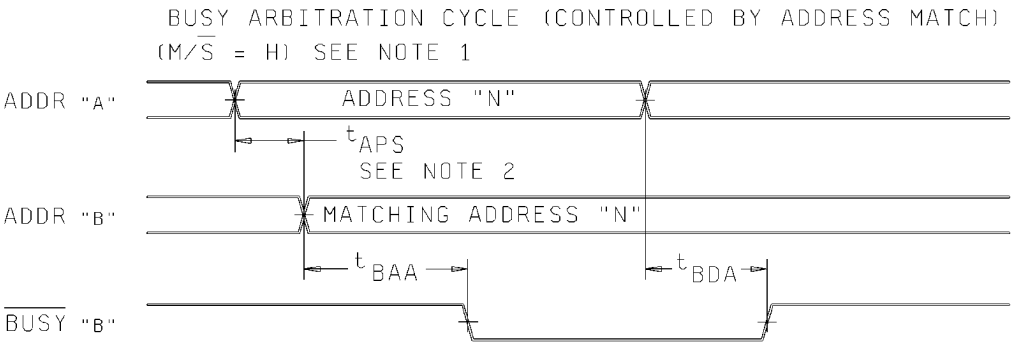


FIGURE 5. Timing waveforms - continued.

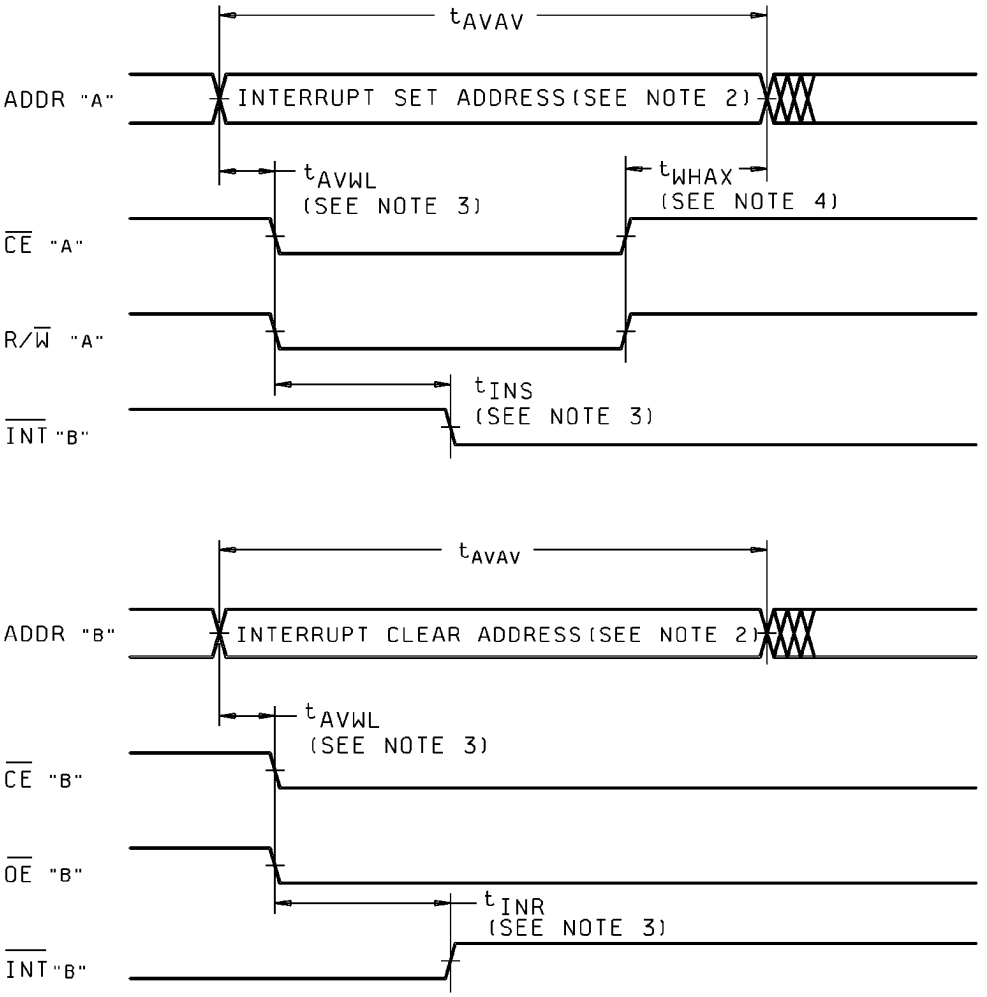




Notes on busy arbitration:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If t_{APS} is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

FIGURE 5. Timing waveforms - continued.

INTERRUPT TIMING (SEE NOTE 1)



Notes on interrupt timing:
1. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

FIGURE 5. Timing waveforms - continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC4}, I_{CC5}	±10% of specified value in table I.
I_{LI}, I_{LO}	±10% of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

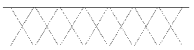
6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

C_{IN} . . . . . Input terminal capacitance.
C_{OUT} . . . . . Output and bidirectional output terminal capacitance.
GND . . . . . Ground zero voltage potential.
I_{CC} . . . . . Supply current.
I_{LI} . . . . . Input leakage current.
I_{LO} . . . . . Output leakage current.
T_C . . . . . Case temperature.
V_{CC} . . . . . Positive supply voltage.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that al manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-04-19

Approved sources of supply for SMD 5962-91662 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535 .

Standard 1/ microcircuit drawing PIN	Vendor CAGE number	Vendor similar 2/ PIN
5962-9166201MXA	61772	IDT7024S70GB
5962-9166201MYA	61772	IDT7024S70FB
5962-9166202MXA	61772	IDT7024L70GB
5962-9166202MYA	61772	IDT7024L70FB
5962-9166203MXA	61772	IDT7024S55GB
5962-9166203MYA	61772	IDT7024S55FB
5962-9166204MXA	61772	IDT7024L55GB
5962-9166204MYA	61772	IDT7024L55FB
5962-9166205MXA	61772	IDT7024S45GB
5962-9166205MYA	61772	IDT7024S45FB
5962-9166206MXA	61772	IDT7024L45GB
5962-9166206MYA	61772	IDT7024L45FB
5962-9166207MXA	61772	IDT7024S35GB
5962-9166207MYA	61772	IDT7024S35FB
5962-9166208MXA	61772	IDT7024L35GB
5962-9166208MYA	61772	IDT7024L35FB
5962-9166209MXA	61772	IDT7024S25GB
5962-9166209MYA	61772	IDT7024S25FB
5962-9166210MXA	61772	IDT7024L25GB
5962-9166210MYA	61772	IDT7024L25FB
5962-9166211MXA	61772	IDT7024S20GB
5962-9166211MYA	61772	IDT7024S20FB
5962-9166212MXA	61772	IDT7024L20GB
5962-9166212MYA	61772	IDT7024L20FB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology 2975 Stender Way P.O. Box 58015 Santa Clara, CA 95054-8015

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.