Preferred Device

NPN Silicon Power Transistor

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("T4" Suffix)
- High Gain 50 Min @ $I_C = 2.0$ Amps
- Low Saturation Voltage 0.5 V @ $I_C = 2.0 \text{ Amps}$
- High Current Gain–Bandwidth Product f_T = 3.0 MHz Min @ I_C = 250 mAdc

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	45	Vdc
Collector-Base Voltage	V _{CB}	45	Vdc
Emitter-Base Voltage	V _{EB}	5	Vdc
Collector Current — Continuous Peak	I _C	4 7	Adc
Base Current	Ι _Β	50	mAdc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	20 0.16	Watts W/°C
Total Power Dissipation (Note 1) @ T _A = 25°C Derate above 25°C	P _D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W

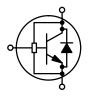
^{1.} These ratings are applicable when surface mounted on the minimum pad sizes recommended.



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2 AMPERES 1000 VOLTS 50 WATTS POWER TRANSISTOR



MARKING DIAGRAMS



DPAK CASE 369A STYLE 1



Y = Year WW = Work Week MJD18002 = Device Code

ORDERING INFORMATION

Device	Package	Shipping
MJD148-2	DPAK	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 2)	$I_C = 100 \text{ mAdc}, I_B = 0$	V _{CEO(sus)}	45	_	Vdc
Collector Cutoff Current	V _{CB} = 45 Vdc, I _E = 0	I _{CBO}	-	20	μAdc
Emitter Cutoff Current	V _{BE} = 5 Vdc, I _C = 0	I _{EBO}	-	1	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 2)	$\begin{split} I_{C} &= 10 \text{ mAdc, } V_{CE} = 5 \text{ Vdc} \\ I_{C} &= 0.5 \text{ Adc, } V_{CE} = 1 \text{ Vdc} \\ I_{C} &= 2 \text{ Adc, } V_{CE} = 1 \text{ Vdc} \\ I_{C} &= 3 \text{ Adc, } V_{CE} = 1 \text{ Vdc} \end{split}$	h _{FE}	40 85 50 30	- 375 - -	1
Collector–Emitter Saturation Voltage (Note 2)	I _C = 2 Adc, I _B = 0.2 Adc	V _{CE(sat)}	-	0.5	Vdc
Base–Emitter On Voltage (Note 2)	I _C = 2 Adc, V _{CE} = 1 Vdc	V _{BE(on)}	-	1.1	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product	I _C = 250 mAdc, V _{CE} = 1 Vdc, f = 1 MHz	f _T	3		MHz

^{2.} Pulse Test: Pulse Width $\leq 300 \,\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

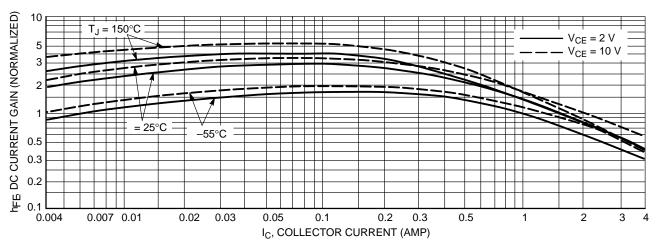


Figure 1. DC Current Gain

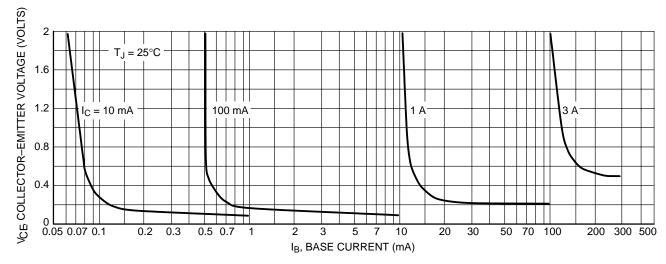


Figure 2. Collector Saturation Region

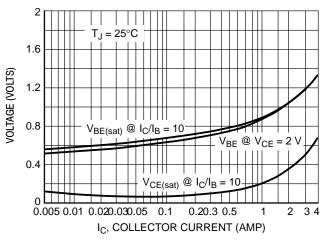


Figure 3. "On" Voltages

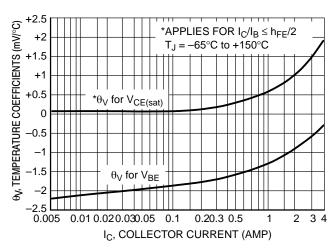


Figure 4. Temperature Coefficients

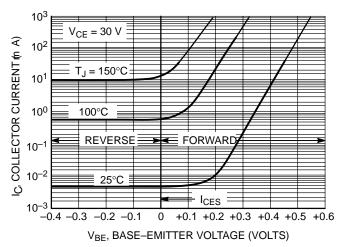


Figure 5. Collector Cut-Off Region

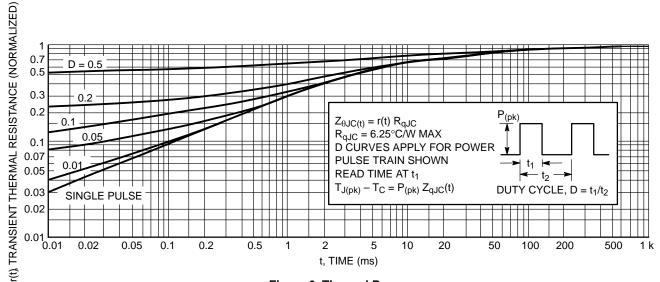


Figure 6. Thermal Response

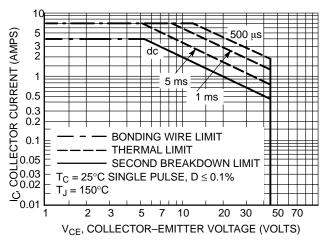


Figure 7. Maximum Rated Forward Bias

FORWARD BIAS SAFE OPERATING AREA INFORMATION

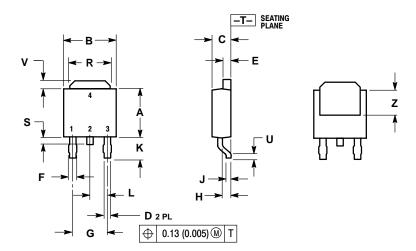
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_{C} is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

DPAK

CASE 369A-13 **ISSUE AB**

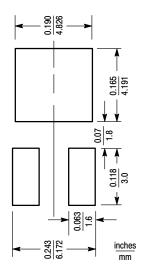


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.250	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180	BSC	4.58	BSC
Н	0.034	0.040	0.87	1.01
7	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29	BSC
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020		0.51	
٧	0.030	0.050	0.77	1.27
7	0.138		3 51	

- STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR

Minimum Pad Sizes Recommended for Surface Mounted Applications



Notes

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