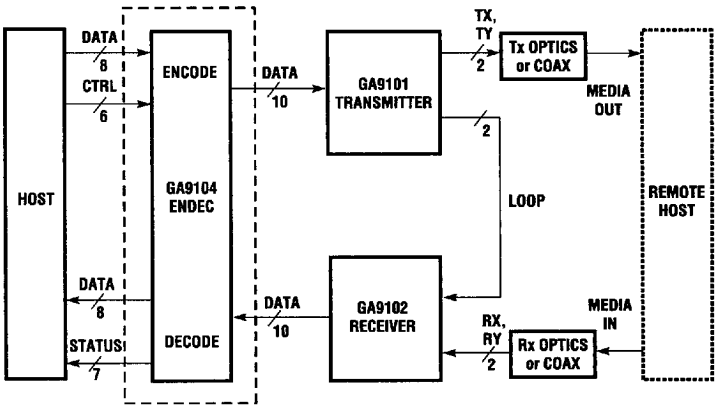
GA9104

200 MBaud ESCON™ ENDEC



The GA9104 is a part of TriQuint's FC-200 chip set, which provides a comprehensive electrical and physical interface in compliance with IBM's Enterprise Systems Connection Architecture (ESCON ™) Specification. This chip set consists of GA9104, the ENDEC; GA9101, the transmitter (Tx); and GA9102, the receiver (Rx). The Tx/Rx chips implement parallel-to-serial conversion, bit clock generation, receive clock/data recovery, and serial-to-parallel conversion. The ESCON I/O interface provides an optical-fiber communication link between I/O devices and main storage of IBM or IBM-compatible computers implementing Enterprise Systems Architecture/390 (ESA/390 ™). The communication link supports a point-to-point configuration or a switched-point-to-point configuration through a "director." This link can be as long as 10 km, operating at a serial rate of 200 Megabaud.

The state-of-the-art CMOS ENDEC chip, GA9104, implements the data and control encoding functions of the physical link of the ESCON standard. In addition, it performs 16-bit CRC and parity generate/check functions. It interfaces to TriQuint's GA9101 Transmitter and GA9102 Receiver chips via two 10-bit buses. This chip set can be used to interface with either the device link protocol controller or the fabric.

The GA9101 and GA9102 Transmitter/Receiver chips, designed with TriQuint's proprietary 0.7 micron One-Up™ GaAs process, interface either directly to the electrical medium or to the fiber-optic interface.

Along with a fiber-optic module, this chip set will provide complete ESCON I/O interface requirements.

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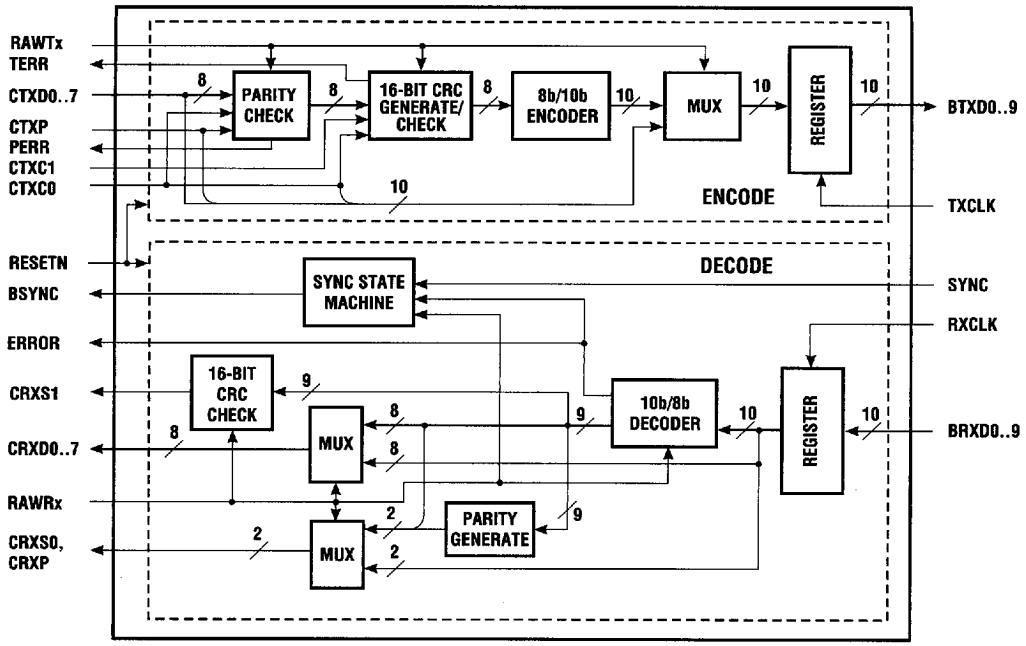
Features

- *For ESCON™, point-to-point and network applications*
- *With fiber optics and TriQuint's Transmitter and Receiver chips, provides a complete ESCON physical link solution*
- *8b/10b Encode/Decode of data and control*
- *Receive Synchronization indicate*
- *TTL-compatible 10-bit-wide Transmitter/Receiver interface with 20 MHz byte clock*
- *16-bit CRC and Parity Generate/Check*
- *Common chip for fabric and device adapters*
- *Multiplexed data/control 8-bit system interface*
- *68-pin PLCC*

GA9104 ENDEC Block Diagram



Functional Description – Encode

The PARITY CHECK block compares the input odd parity with that of the incoming data, CTXD0..7 and CTXC0. If the number of ones in the input is an even number, CTXP will be HIGH. If the number of ones in the input is odd, CTXP will be LOW. If there is a parity error, it is flagged through the PERR signal. This parity error flag is disabled (PERR=0) when the RAWTx signal is active.

The CRC GENERATE/CHECK function either generates or checks the CRC for the incoming 8-bit data word, CTXD0..7. For a 16-bit CRC, the methodology, polynomials, and equations are the same as in the ESCON specification. A CRC is computed for every frame. The computation begins after the receipt of the Start-of-Frame (SOF) ordered set and finishes one byte before the End-of-Frame (EOF). The CRC corresponds to the ones complement of the remainder, R(x),obtained by dividing the frame sequence polynomial H(x) by the following generator polynomial, P(x),* where

$$P(x) = X^{16} + X^{12} + X^5 + 1$$

The frame sequence polynomial is formed as follows: the bits of the frame are treated as a coefficient of a polynomial D(x) of order k, where k is one degree less than the total number of bits. A polynomial H(x) is formed by multiplying D(x) by X^{16} and inverting the 16 terms of the resulting polynomial, starting at the X(k+16) term. The order of computation within a byte starts with the least significant bit (CTXD0) and continues through to the most significant bit (CTXD7). CRC is appended to the data starting with the most significant coefficient (X^{15}) and continuing through to the least significant coefficient.

A 16-bit CRC check is performed by comparing the incoming CRC to the computed CRC. The CRC check is performed by checking the remainder, R(x), at the end of the incoming frame against the expected value of R(x) as shown below. If the incoming CRC is correct, the remainder should be 1D0F Hex, in the order of reception.

$$R(x) = X^{12} + X^{11} + X^{10} + X^{8} + X^{3} + X^{2} + X^{1} + 1$$

In the RAW mode, the CRC function is disabled. The CRC GENERATE functional block is enabled at the device by the CTXC1 signal input. (This same control signal is used to enable the Check CRC function at the fabric interface.) A logic HIGH on the CTXC1 pin indicates the Generate CRC function is selected. A logic LOW on CTXC1 indicates the Check CRC is selected.

When initiated, the CRC computation commences after the Start-of-Frame (SOF) signal, and ends prior to the End-of-Frame (EOF) signal.

The requirements for the Generate CRC mode for the ENCODE block are as follows: to enable the start of the 16-bit CRC computation, the CTXC1 pin is HIGH, the previous encoded byte is K28.7, and CTXC0 goes from HIGH to LOW. The CRC computation is completed when the CTXC0 signal goes back to HIGH. The CTXC0 signal must be HIGH for at least two byte clocks in order to append the CRC to the transmitted data. In the Generate CRC mode or when RAWTx = 1, the signal at the TERR pin (CRC Error) is LOW. The timing for the Generate CRC mode is shown in Figure 1. During the Append CRC cycle, while the two input bytes at CTXD0..7 are ignored, the logic still performs the parity error check on this data.

The requirements for the Check CRC mode for the ENCODE block are as follows: the CTXC1 pin is LOW, the previous encoded byte was K28.7, and the CTXC0 signal goes from HIGH to LOW. This sequence enables the start of the 16-bit CRC computation. The CRC computation is completed when the CTXC0 signals goes back to HIGH from a previous LOW. If there is a CRC error, it is flagged by the TERR pin going HIGH for one byte time. The timing for the Check CRC mode is shown in Figure 2.

The 8b/10b ENCODER encodes the data as per the ESCON rules for encoding. The encoding of valid data and valid special characters are as shown in Tables 1 and 2. The tables have two columns of encoded output based on the current Running Disparity (R_D). The current Running Disparity may be positive or negative on reset. A new Running Disparity is calculated from the transmitted character. The CTXC0 and CTXD7..0 inputs have the bit combination as shown in Table 2 for the encoding of K28.x control characters.

The MUX selects between the 8b/10b ENCODER output and the data inputs. When the RAWTx input signal is HIGH, the inputs CTXD0..7, CTXP, and CTXC0 are selected, that is, the data bypasses the CRC and ENCODER functional blocks and is latched into the register in its "raw" form. When the RAWTx input is LOW, the ENCODER output is selected. The output of the MUX is 10 bits wide and is clocked into the REGISTER using the transmit byte clock, TXCLK. The REGISTER output goes to the GA9101 transmitter.

The asynchronous RESETN input, when LOW, is used to clear all internal state machine registers. It can take up to four byte clocks to clear the internal state machines after RESETN goes back to HIGH.

The bit ordering for transmission in the RAW mode is CTXD0..7, CTXP1 and CTXC0. It corresponds to mapping these signals to BTXD9..0, respectively.

**See ESCON I/O Interface document for more details.*

Figure 1. Generate CRC Mode Timing

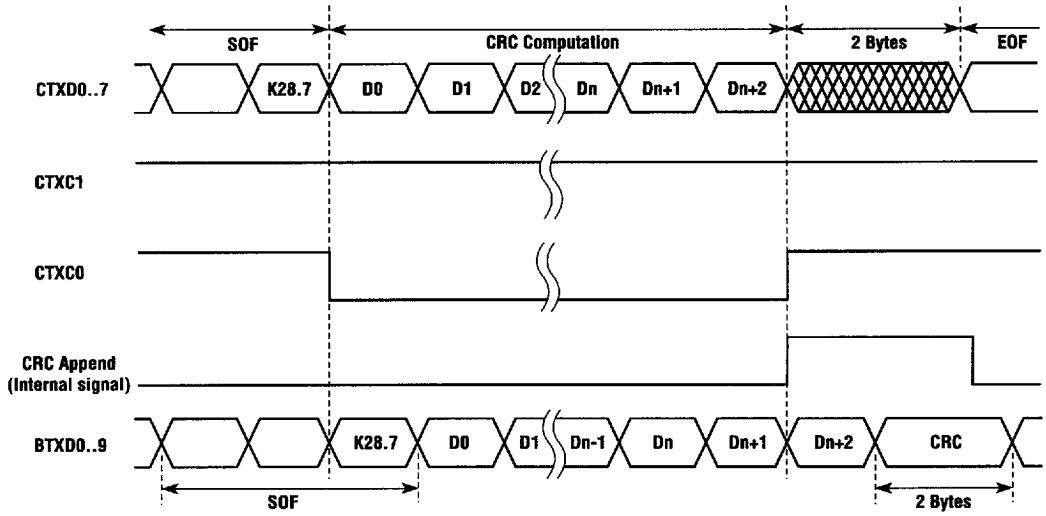


Figure 2. Check CRC Mode Timing

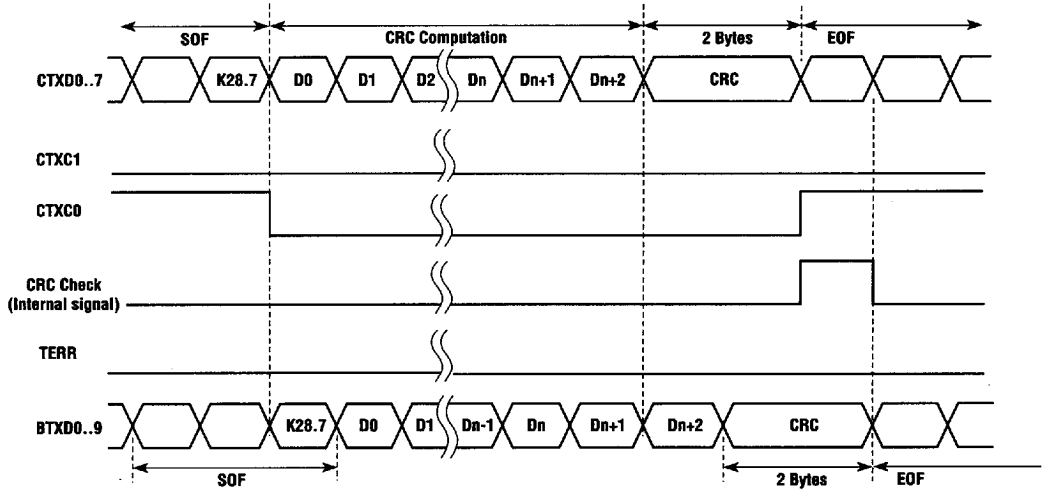


Table 1. Valid Data Characters – Encoding

Data Byte Name	Bits HGF	EDCBA [1]	Current RD – abcdei	fghj [2]	Current RD + abcdei	fghj [2]
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.2	010	11111	101011	0101	010100	0101
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.4	100	00110	011001	1101	011001	0010
D7.4	100	00111	111000	1101	000111	0010
D8.4	100	01000	111001	0010	000110	1101
D9.4	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010

Table 1. Valid Data Characters – Encoding (cont.)

Data Byte Name	HGF	Bits EDCBA [1]	Current RD – abcdei	fghj [2]	Current RD + abcdei	fghj [2]
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

Table 2. Valid Special Characters – Encoding

Special Code Name	CTXC0	CTXD7..0	Current RD – abcdei	fghj [2]	Current RD + abcdei	fhgj [2]	Notes
K28.0	1	00011100	001111	0100	110000	1011	Reserved
K28.1	1	00111100	001111	1001	110000	0110	
K28.2	1	01011100	001111	0101	110000	1010	
K28.3	1	01111100	001111	0011	110000	1100	Reserved
K28.4	1	10011100	001111	0010	110000	1101	
K28.5	1	10111100	001111	1010	110000	0101	
K28.6	1	11011100	001111	0110	110000	1001	
K28.7	1	11111100	001111	1000	110000	0111	
K23.7	1	11110111	111010	1000	000101	0111	Reserved
K27.7	1	11111011	110110	1000	001001	0111	Reserved
K29.7	1	11111101	101110	1000	010001	0111	Reserved
K30.7	1	11111110	011110	1000	100001	0111	Reserved

NOTES: 1. HGF EDCBA" correspond to Data Inputs CTXD7..0, in that order.

2. "a" is to be transmitted first, followed by "b", "c", ..., "j". "abcdeifghj", in that order, correspond to BTXD9 . . BTXD0.

Reserved – valid transmission characters which are not defined for use by ESCON.

Functional Description – Decode

The 10-bit-wide input from the ESCON/Fiber Channel Receiver is clocked into the REGISTER, using the Receiver byte clock, RXCLK.

The 10b/8b DECODER decodes the 10-bit data and special characters according to Tables 1 and 2. If RAWRx = 1 or RESETN = 1, the current Running Disparity is negative and each of the characters are decoded based on the received character. The DECODER also checks for the validity of received characters based on Tables 1 and 2. Any code violations or disparity are flagged through the ERROR pin. The special code characters are decoded as shown in Table 2, with outputs being CRXS0 and CRXD7..0, respectively.

The CRC CHECK block performs a 16-bit Cyclic Redundancy Check on the received data. (This block is enabled at all times.) The CRC computation begins after the Start-of-Frame (SOF) Detect and finishes prior to End-of-Frame (EOF). As in the case of the ENCODE block, the CRC check is performed by comparing the incoming frame to the expected value of the remainder R(x). If the remainder is not equal to 1D0F Hex, a CRC error is flagged at the CRXS1 pin. If RAWRx = 1, then CRXS1 = 0.

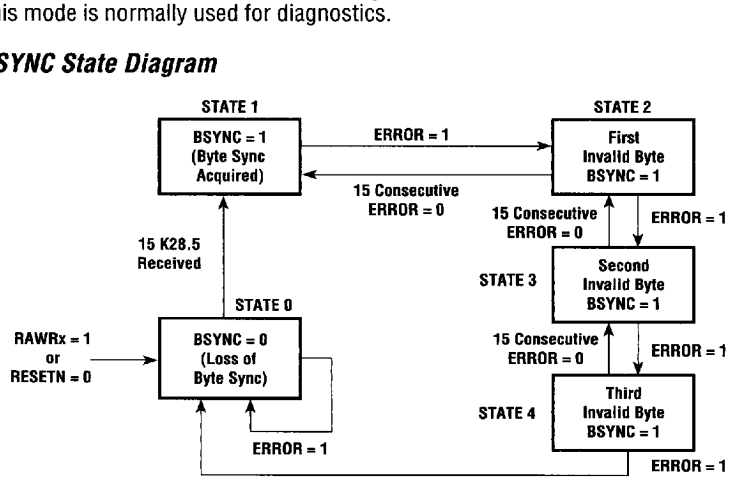
The DECODE functional block has a passthrough mode similar to the one in the ENCODE block. In this mode, when RAWRx = 1, the data bypasses the decoding logic and is made available to the host in its original form. This mode is normally used for diagnostics.

The MUX is used to choose between the decoded data/control and the REGISTER output. The REGISTER output is chosen when the RAWRx input signal is active HIGH. Otherwise, the decoded data/control is chosen.

The PARITY GENERATE block is used to generate an odd parity signal, CRXP, for every byte of data, CRXD0..7 and CRXS0. If the number of ones in the output CRXD0..7 and CRXS0 is an even number, CRXP will be HIGH. If the number of ones in the output CRXD0..7 and CRXS0 is odd, CRXP will be LOW.

The GA9104 has the ability to detect loss of synchronization in the link. The BSYNC signal is used to denote whether or not the link is synchronized. As shown in the state diagram below, BSYNC = 0 in State 0. That is, there is loss of byte synchronization if the link is in reset mode. The link achieves byte synchronization (State 1, BSYNC = 1) only after fifteen K28.5 bytes are received with no bytes in error during that time. Once synchronized, the link could lose synchronization if it receives an invalid byte as indicated by ERROR = 1. For a total loss of synchronization, the link must receive four invalid transmission characters within 60 bytes. During the sequence of transitioning from State 1 to State 4, the link can reacquire byte synchronization (return to State 1) if it receives 15 consecutive valid bytes (ERROR = 0) in each of the States as shown in the BSYNC State Diagram.
If RAWRx = 1, BSYNC = 0.

BSYNC State Diagram



Absolute Maximum Ratings

Exceeding the absolute maximum ratings may damage the device.

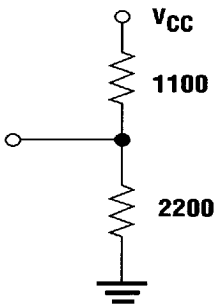
Storage temperature	-65°C to +150°C
Ambient temperature	-55°C to +125°C
Supply voltage to ground	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (VCC +0.5 V)
DC input current	-30 mA to +5 mA

Operating Conditions

Proper functionality is guaranteed under these conditions:

Supply voltage	5V ± 5%
Ambient temperature	0-70°C

TTL Test Load, TLL Outputs



DC Characteristics (Over operating range unless otherwise specified.)

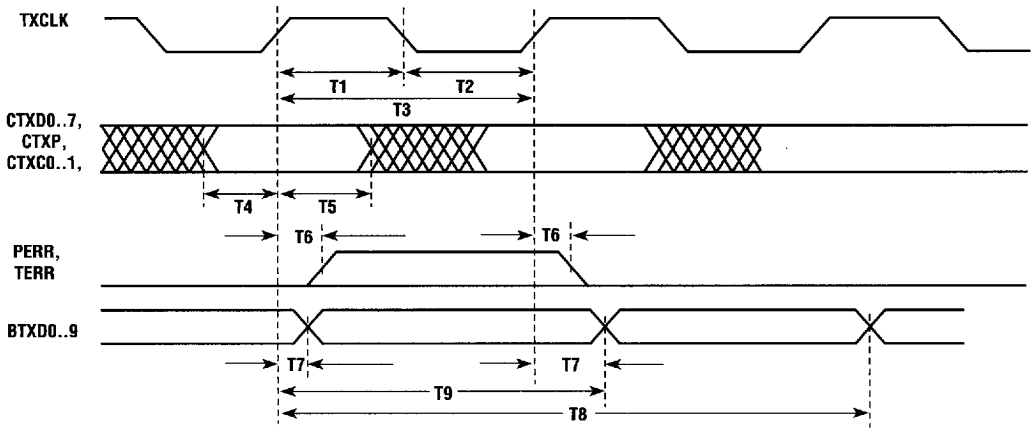
Symbol	Description	Test Conditions		Limits[1] Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min V_{IN}	I_{OH} = -4 mA = V_{IH} or V_{IL}	3.6			V
V_{OL}	Output LOW voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4 mA			0.37	V
V_{IH}[2]	Input HIGH level voltage for all inputs	Guaranteed input logical HIGH		2.0			V
V_{IL}[2]	Input LOW level voltage for all inputs	Guaranteed input logical LOW				0.8	V
I_{IL}	Input Leakage current	V_{CC} = Max	V_{IN} = 0.40 V		-150	-400	µA
I_{CC}	Power supply current	V_{CC} = Max			35	60	mA

Notes: 1. Typical limits are: V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

AC Characteristics – ENCODE

Parameter	Description	Min.	Typ.	Max.	Unit
T1	TXCLK Pulse Width HIGH	15			ns
T2	TXCLK Pulse Width LOW	15			ns
T3	TXCLK Period	48.00	50.00	52.00	ns
T4	CTXD0..7, CTXP, CTXC0..1 Setup Time	2			ns
T5	CTXD0..7, CTXP, CTXC0..1 Hold Time	7			ns
T6	TXCLK ↑ to PERR, TERR	3.50		17.00	ns
T7	TXCLK ↑ to BTXD0..9	5.00		19.00	ns
T8	ENCODE Latency (RAWTx = LOW)	2•T3 +5		2•T3 +19	ns
T9	ENCODE Latency (RAWTx = HIGH)	T3 +5		T3 +19	ns

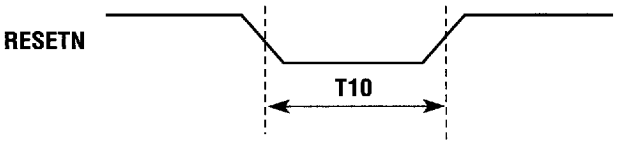
ENCODE Timing Diagram



AC Characteristics – Miscellaneous

Parameter	Description	Min.	Typ.	Max.	Unit
T10	RESETN Pulse Width LOW	10			ns

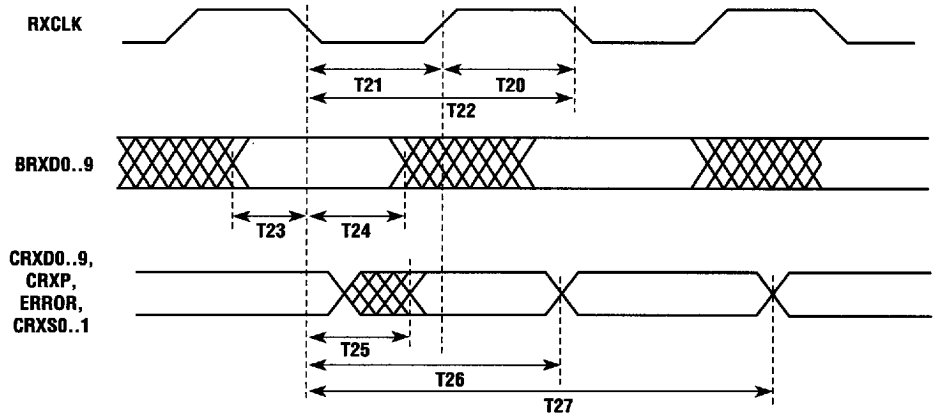
RESETN Timing Diagram



AC Characteristics – DECODE

Parameter	Description	Min.	Typ.	Max.	Unit
T20	RXCLK Pulse Width HIGH	(T22/2) - 3			ns
T21	RXCLK Pulse Width LOW	(T22/2) - 3			ns
T22	RXCLK Period	48.00	50.00	52.00	ns
T23	BRXD0..9, SYNC Setup Time	1			ns
T24	BRXD0..9, SYNC Hold Time	8			ns
T25	RXCLK ↓ to CRXD0..7, CRXP, ERROR, CRXS0..1 Outputs	4.00		11.00	ns
T26	DECODE Latency (RAWRx = HIGH)	T22 +4		T22 +11	ns
T27	DECODE Latency (RAWRx= LOW)	2•T22 +4		2•T22 + 11	ns

DECODE Timing Diagram



System Block Diagram

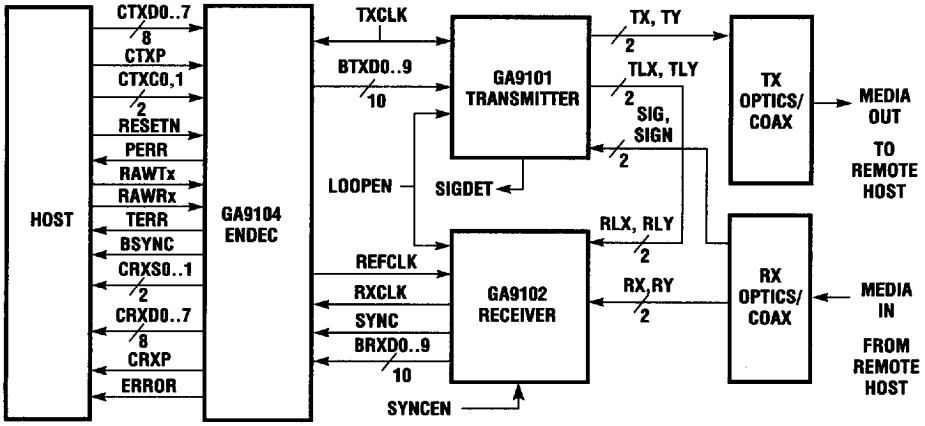
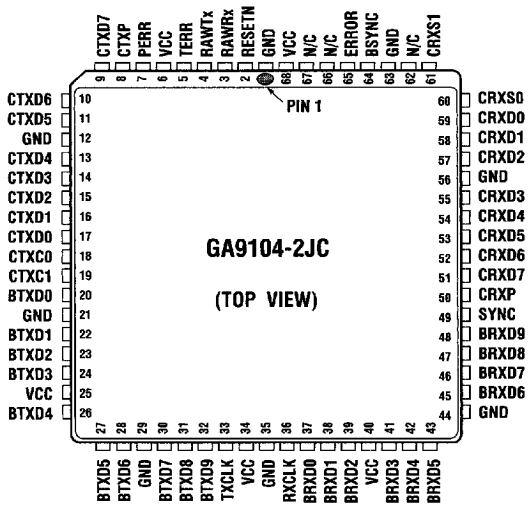


Table 5. Pin Definitions

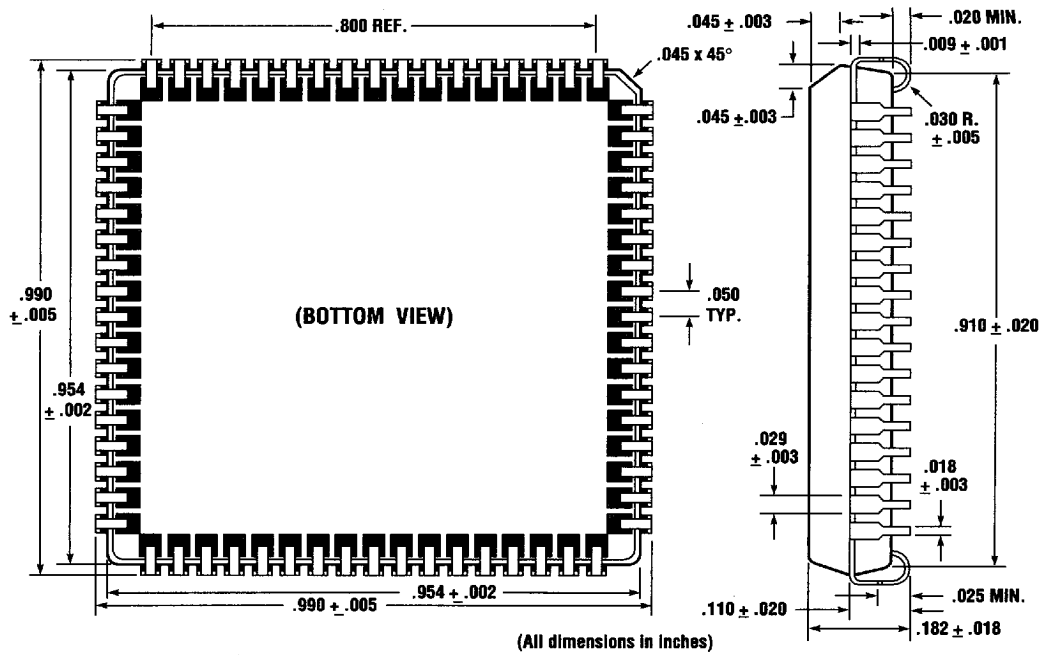
Symbol	I/O	Quantity	Logic Level	Active	Description	Pin #
CRXD0..7	Output	8	TTL	HIGH	Receive Data Output	59-57, 55-51
CRXS0	Output	1	TTL	HIGH	Receive Control	60
CRXS1	Output	1	TTL	HIGH	Receive CRC Error	61
BRXD0..9	Input	10	TTL	HIGH	Receive Data Input	37-39, 41-43, 45-48
RXCLK	Input	1	TTL	HIGH	Receive Byte Clock	36
SYNC	Input	1	TTL	HIGH	Receive Byte Sync	49
TXCLK	Input	1	TTL	HIGH	Transmit Byte Clock	33
BTXD0..9	Output	10	TTL	HIGH	Transmit Data Output	20, 22-24, 26-28, 30-32
CTXD0..7	Input	8	TTL	HIGH	Transmit Data Input	17-13, 11-9
CTXC0	Input	1	TTL	HIGH	Transmit Control	18
TERR	Output	1	TTL	HIGH	Transmit CRC Error	5
CTXC1	Input	1	TTL	HIGH	Generate CRC	19
BSYNC	Output	1	TTL	HIGH	Byte Sync Acquired	64
RAWTx	Input	1	TTL	HIGH	Raw Mode Transmit	4
RESETN	Input	1	TTL	LOW	System Reset	2
ERROR	Output	1	TTL	HIGH	Illegal Line Code or Disparity Received	65
PERR	Output	1	TTL	HIGH	Parity Error	7
CRXP	Output	1	TTL	HIGH	Odd Parity Output	50
CTXP	Input	1	TTL	HIGH	Odd Parity Input	8
RAWRx	Input	1	TTL	HIGH	Raw Mode Receive	3
VCC	Input	5	N/A	N/A	+5 Volt Supply	6, 25, 34, 40, 68
GND	Input	8	N/A	N/A	Ground	1, 12, 21, 29, 35, 44, 56, 63
RESERVED		3				62, 66, 67

Total Pins = 68

GA9104 Pinout



68-Pin Plastic Leaded Chip Carrier (PLCC)



Ordering Information

GA9104-2JC – ENDEC

Supporting Products

GA9101-2MC – Transmitter

GA9102-2MC – Receiver

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