REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to military drawing format. Add LCC package type. Add one device type. Change replacement military specification number. Add two vendors.	87-05-05	M.A.L.
B	Add vendor CAGE number 6Y440 as a supplier of device type 03. Changes to table I and table I footnotes. Changes to figure 1, figure 3, and figure 5. Editorial changes throughout.	88-10-04	M.A.L.
C	Delete vendor CAGE 01295 as a source of supply for X package. Add the Y package for vendor CAGE 01295. Editorial changes throughout.	90-11-06	M.A.L.
D	Changes to figure 1, case outline Y, dimensions for symbols L1 and L2. Editorial changes throughout.	92-07-27	M.A.L.

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV	D	C	C	C	C	C	C	C	C	C	C	C	C	C	C	D			
SHEET	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29			

REV STATUS OF SHEETS	REV	D	D	D	C	B	B	B	B	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
86-01-02

REVISION LEVEL
D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, NMOS, 256K X 1 RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	85152

SHEET 1

DESC FORM 193-1
JUL 91

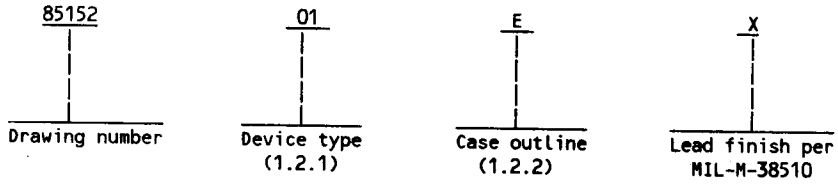
5962-E333

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit	Access time	Refresh
01		256K x 1 DRAM	150 ns	256 cycles (4 ms)
02		256K x 1 DRAM	200 ns	256 cycles (4 ms)
03		256K x 1 DRAM	120 ns	256 cycles (4 ms)

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
X	See figure 1 (18-terminal, .305" x .505"), rectangular chip carrier package
Y	See figure 1 (18-terminal, .305" x .505"), rectangular chip carrier package

1.3 Absolute maximum ratings. 2/

Voltage range for any pin, including V_{CC} supply 3/	-1.0 V dc to +7.0 V dc
Short circuit output current	50 mA
Power dissipation	1 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X and Y	50°C/W
Case E	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.75 V dc to 5.25 V dc
Supply voltage (V_{SS})	0 V dc
High level input voltage range (V_{IH})	2.4 V dc to 5.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.6 V dc
Case operating temperature range (T_C)	-55°C to +110°C
Refresh cycle time	4.0 ms

1/ Generic numbers are listed on the Standarized Military Source Approval Bulletin and will be listed in MIL-BUL-103.
2/ Voltage values are with respect to V_{SS}.
3/ Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$ 4.75 V dc $\le V_{CC} \le$ 5.25 V dc	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -5 mA, V_{CC} = 4.75 V V_{IL} = 0.6 V, V_{IH} = 2.4 V	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 4.2 mA, V_{CC} = 4.75 V	1,2,3	All		0.4	V
High level input leakage current	I_{IH}	V_{CC} = 5.25 V, V_I = 5.0 V	1,2,3	All		10	µA
Low level input leakage current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.0 V	1,2,3	All		-10	µA
High level output leakage current	I_{OH}	V_{CC} = 5.25 V V_O = 5.25 V	1,2,3	All		10	µA
Low level output leakage current	I_{OL}	V_{CC} = 5.25 V, V_O = 0.0 V	1,2,3	All		-10	µA
Average operating current during read or write cycle 3/	I_{CC1}	t_c = minimum cycle V_{CC} = 5.25 V	1,2,3	01		75	mA
				02		60	mA
				03		80	mA
Standby current 3/	I_{CC2}	After 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high V_{CC} = 5.25 V	1,2,3	All		5	mA
Average refresh current 3/	I_{CC3}	t_c = minimum cycle, $\overline{CAS}$ high, RAS cycling V_{CC} = 5.25 V	1,2,3	01		60	mA
				02		50	mA
				03		63	mA
Average page-mode current 3/	I_{CC4}	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling V_{CC} = 5.25 V	1,2,3	01,03		50	mA
				02		45	mA
Access time from $\overline{RAS}$	$t_{a(R)}$	See figures 5 and 6 V_{CC} = 4.75 V to 5.25 V	9,10,11	01		150	ns
				02		200	ns
				03		120	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$ 4.75 V dc $\le V_{CC} \le$ 5.5 V dc	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Access time from $\overline{CAS}$	$t_{a(C)}$	See figures 5 and 6 V_{CC} = 4.75 V to 5.25 V	9,10,11	01		80	ns
				02		100	ns
				03		65	ns
Output disable time after CAS high 4/	$t_{dis(CH)}$		9,10,11	01		30	ns
				02		35	ns
				03		30	ns
Page-mode cycle time 4/	$t_{c(P)}$		9,10,11	01	145		ns
				02	190		ns
				03	125		ns
Page-mode cycle time (read-modify-write cycle 4/	$t_{c(PM)}$		9,10,11	01	205		ns
				02	250		ns
				03	172		ns
Read cycle time 4/	$t_{c(rd)}$		9,10,11	01	260		ns
				02	330		ns
				03	230		ns
Write cycle time 4/	$t_{c(W)}$		9,10,11	01	260		ns
				02	330		ns
				03	230		ns
Read-write/read-modify-write cycle time 4/	$t_{c(rdW)}$		9,10,11	01	315		ns
				02	390		ns
				03	277		ns
Pulse duration, $\overline{CAS}$ high (page mode)	$t_{W(CH)P}$		9,10,11	01	60		ns
				02	80		ns
				03	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$ 4.75 V dc $\le V_{CC} \le$ 5.5 V dc	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Pulse duration, $\overline{CAS}$ high (non-page mode)	$t_{w(CH)}$	See figures 5 and 6 V_{CC} = 4.75 V to 5.25 V	9,10,11	01	60		ns
				02	80		ns
				03	25		ns
Pulse duration, $\overline{CAS}$ low 5/	$t_{w(CL)}$		9,10,11	01	80	10,000	ns
				02	100	10,000	ns
				03	65	10,000	ns
Pulse duration, $\overline{RAS}$ high (precharge time) (page mode)	$t_{w(RH)P}$		9,10,11	01,02	120		ns
				03	115		ns
Pulse duration, $\overline{RAS}$ high (precharge time) (non-page mode)	$t_{w(RH)}$		9,10,11	01,03	100		ns
				02	120		ns
Pulse duration, $\overline{RAS}$ low 6/	$t_{w(RL)}$		9,10,11	01	150	10,000	ns
				02	200	10,000	ns
				03	120	10,000	ns
Write pulse duration	$t_{w(W)}$		9,10,11	01	45		ns
				02	55		ns
				03	40		ns
Column address setup time	$t_{su(CA)}$		9,10,11	All	0		ns
Row address setup time	$t_{su(RA)}$		9,10,11	01,02	5		ns
				03	0		ns
Data setup time	$t_{su(D)}$		9,10,11	All	3		ns
Read command setup time	$t_{su(rd)}$		9,10,11	All	5		ns
Early write command setup time before $\overline{CAS}$ low	$t_{su(WCL)}$		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, $4.75\ V\ dc \le V_{CC} \le 5.5\ V\ dc$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write command setup time before CAS high	$t_{su(WCH)}$	See figures 5 and 6 V_{CC} = 4.75 V to 5.25 V	9,10,11	01	45		ns
				02	65		ns
				03	40		ns
Write command setup time before RAS high	$t_{su(WRH)}$		9,10,11	01	45		ns
				02	65		ns
				03	40		ns
Column address hold time after CAS low	$t_{h(CLCA)}$		9,10,11	01	30		ns
				02	45		ns
				03	20		ns
Row address hold time	$t_{h(RA)}$		9,10,11	01	20		ns
				02	25		ns
				03	15		ns
Column address hold time after RAS low	$t_{h(RLCA)}$		9,10,11	01	100		ns
				02	145		ns
				03	75		ns
Data hold time after $\overline{CAS}$ low	$t_{h(CLD)}$		9,10,11	01	50		ns
				02	55		ns
				03	40		ns
Data hold time after $\overline{RAS}$ low	$t_{h(RLD)}$		9,10,11	01	120		ns
				02	155		ns
				03	95		ns
Data hold time after $\overline{W}$ low	$t_{h(WLD)}$		9,10,11	01	45		ns
				02	55		ns
				03	40		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$ 4.75 V dc $\le V_{CC} \le$ 5.5 V dc	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read command hold time after CAS high	$t_{h(CHrd)}$	See figures 5 and 6 V_{CC} = 4.75 V to 5.25 V	9,10,11	All	0		ns
Read command hold time after RAS high	$t_{h(RHrd)}$		9,10,11	01,03	10		ns
				02	15		ns
Write command hold time after CAS low	$t_{h(CLW)}$		9,10,11	01	50		ns
				02	55		ns
				03	40		ns
Write command hold time	$t_{h(RLW)}$		9,10,11	01	120		ns
				02	155		ns
				03	95		ns
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{RLCH}		9,10,11	01	150		ns
				02	200		ns
				03	120		ns
Delay time, $\overline{CAS}$ high to RAS low	t_{CHRL}		9,10,11	All	5		ns
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{CLRH}		9,10,11	01	80		ns
				02	100		ns
				03	65		ns
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high 7/	t_{RLCH}		9,10,11	01	30		ns
				02	40		ns
				03	30		ns
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low 7/	t_{CLRL}		9,10,11	01	30		ns
				02	35		ns
				03	30		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +110°C$, 4.75 V dc $\le V_{CC} \le$ 5.5 V dc	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CLWL}	See figures 5 and 6, V_{CC} = 4.75 V to 5.25 V	9,10,11	01	85		ns
				02	90		ns
				03	67		ns
Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RHCL}		9,10,11	All	25		ns
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	t_{RLCL}		9,10,11	01	25	70	ns
				02	35	100	ns
				02	25	55	ns
Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RLWL}		9,10,11	01	155		ns
				02	190		ns
				03	122		ns
Refresh time interval	t_{rf}		9,10,11	All		4.0	ms

1/ Timing measurements are referenced to V_{IL} maximum and V_{IH} minimum.
2/ System transition times (rise and fall) for RAS and CAS are to be a minimum of 3 ns and a maximum of 50 ns.
3/ All I_{CC} measurements are taken with output (Q) open.
4/ All cycle times assume transition times t_t = 5 ns.
5/ In a read-modify-write cycle t_{LWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition time, this may require additional CAS low time $t_{W(EL)}$. Applies to page-mode read-modify-write also.
6/ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition time, this may require additional RAS low time $t_{W(RL)}$.
7/ CAS before RAS refresh only.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8a, 8b

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

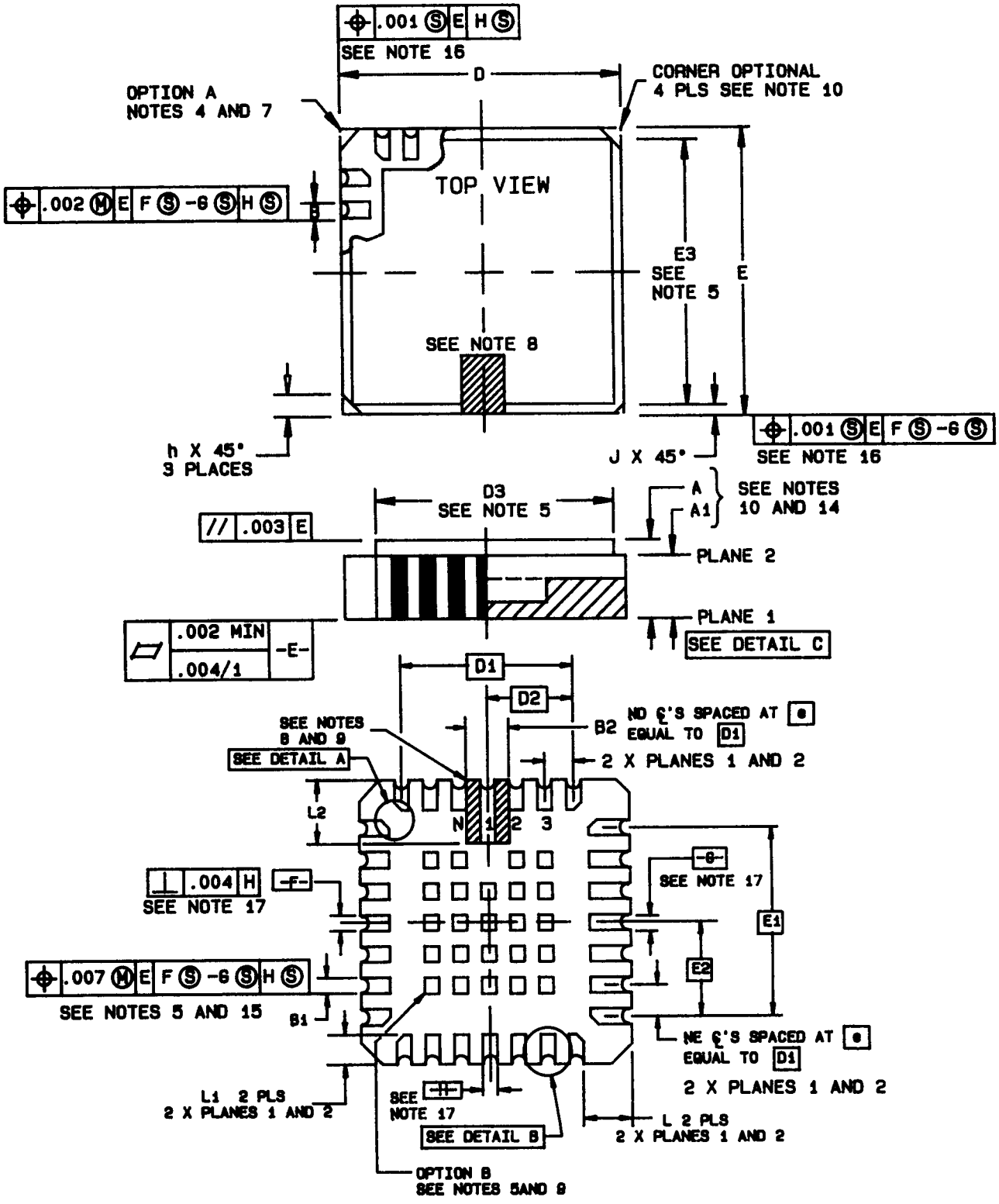


FIGURE 1. Case outlines X and Y (18-terminal, .305" x .505"), rectangular chip carrier package.

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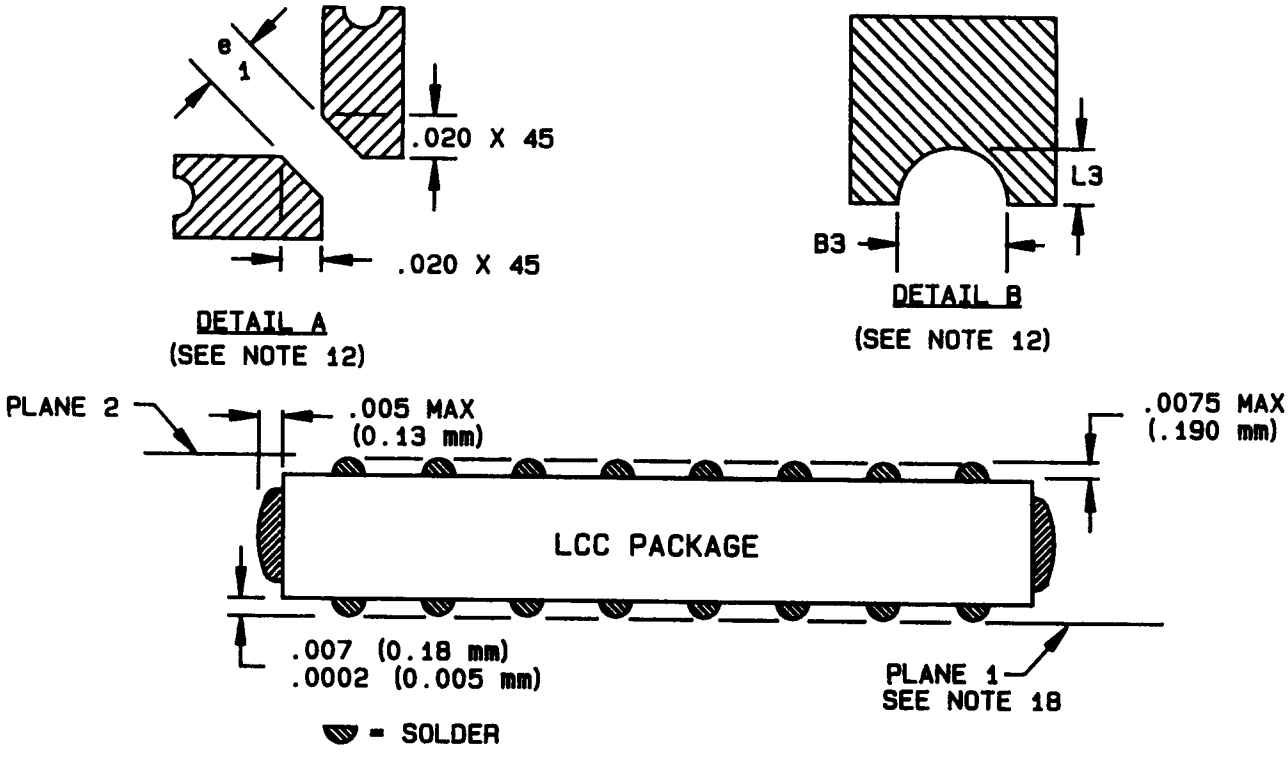


FIGURE 1. Case outlines X and Y (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

Dimensions					
	Inches		Millimeters		
Symbol	Min	Max	Min	Max	Notes
A	.060	.120	1.52	3.04	10, 14
A1	.050	.088	1.27	2.24	
B	---	---	---	---	
B1	.022	.028	0.56	0.71	5, 7
B2	.072 REF		1.83 REF		8, 9
B3	.006	.022	0.15	0.56	12
D	.280	.305	7.11	7.74	
D1	.150 BSC		3.81 BSC		
D2	.075 BSC		1.90 BSC		17
D3	---	.305	---	7.74	5
E	.480	.505	12.19	12.83	
E1	.200 BSC		5.08 BSC		
E2	.100 BSC		2.54 BSC		17
E3	---	.365	---	9.27	5
e	.050 BSC		0.38 BSC		
e1	.015	---	5, 13		5, 13
h	.040 REF		1.02 REF		11
j	.020 REF		0.51 REF		11
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	8, 9
L3	.003	.015	0.08	0.38	12
ND	4				6
NE	5				6
N	18				6

FIGURE 1. Case outline X (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

Dimensions					
	Inches		Millimeters		
Symbol	Min	Max	Min	Max	Notes
A	.060	.120	1.52	3.04	10, 14
A1	.050	.088	1.27	2.24	
B	---	---	---	---	
B1	.020	.030	0.50	0.76	5, 7
B2	.072 REF		1.83 REF		8, 9
B3	.006	.022	0.15	0.56	12
D	.280	.305	7.11	7.74	
D1	.150 BSC		3.81 BSC		
D2	.075 BSC		1.90 BSC		17
D3	---	.305	---	7.74	5
E	.480	.505	12.19	12.83	
E1	.200 BSC		5.08 BSC		
E2	.100 BSC		2.54 BSC		17
E3	---	.480	---	12.19	5
e	.050 BSC		0.38 BSC		
e1	.015	---	0.38	---	5, 13
h	.010 REF		0.25 REF		11
j	.010 REF		0.25 REF		11
L	.040	.055	1.14	1.40	
L1	.110	.120	2.79	3.05	19
L2	.120	.130	3.05	3.30	8, 9
L3	.003	.015	0.08	0.38	12
ND	4				6
NE	5				6
N	18				6

FIGURE 1. Case outline Y (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

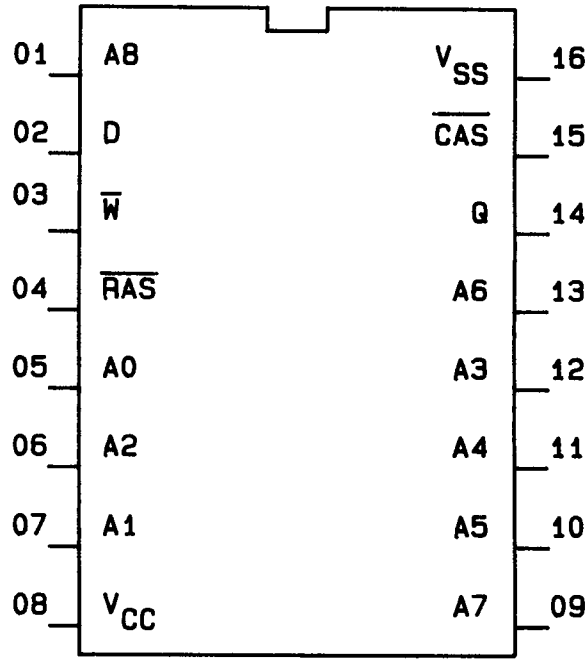
NOTES:

1. Dimensions are in inches.
2. Metric equivalents are for general information only.
3. To specify options in detail specification, see figure C-7 of MIL-M-38510.
4. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals (see 50.6 of MIL-M-38510).
5. Unless otherwise specified, a minimum clearance of .015 inch (0.38 mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
6. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E" respectively.
7. The required plane 1 terminals and optional plane 2 terminals shall be electrically connected.
8. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2 (see 40.6.3 of MIL-M-38510). Plane 1 terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension. See note 9 for more details.
9. Plane 1 is the heat radiating surface. This surface may optionally be metallized with a checkerboard pattern of thermal conduction pads. The pad centerlines shall be aligned with the terminal centerlines. The number of pads in the pattern is determined by the following algorithm: (ND - 2) x (NE - 2) see note 6. When this option exists, the terminal 1 index feature may be additionally or alternately defined by deleting the thermal pad which is adjacent to terminal 1.
10. Dimension "A" controls the overall package thickness. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.25 mm) and a maximum of .040 inch (1.02 mm).
11. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
12. See 50.6 and figure C-6 of MIL-M-38510. Dimensions "B3" minimum, "L3" minimum, and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimensions "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
13. Corner metallization for terminals may have a .020 inch (0.51 mm) by 45° maximum chamfer to obtain the e1 dimension.
14. Chip carriers shall be constructed of a minimum of two ceramic layers.
15. The pad metallization, including annular ring, at the pad-to-package edge shall be within the virtual pad width established by true position dimensioning.
16. The tolerance is intended to limit package edge anomalies caused by material protrusions, such as rough ceramic, and misaligned ceramic layers.
17. When the number of terminals per side is even, datums F-G and -H- are located at the terminal array centers. When the number of terminals per side is odd, datums F-G and -H- are located at the centers of the center terminals.
18. See 40.2.3 of MIL-M-38510 for coplanarity measurement requirements.
19. Must be a dimensional difference of .020 inch (0.51 mm) between L1 and L2.

FIGURE 1. Case outline Y (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

Device types 01, 02, and 03

Case E



Device types 01, 02, and 03

Cases X and Y

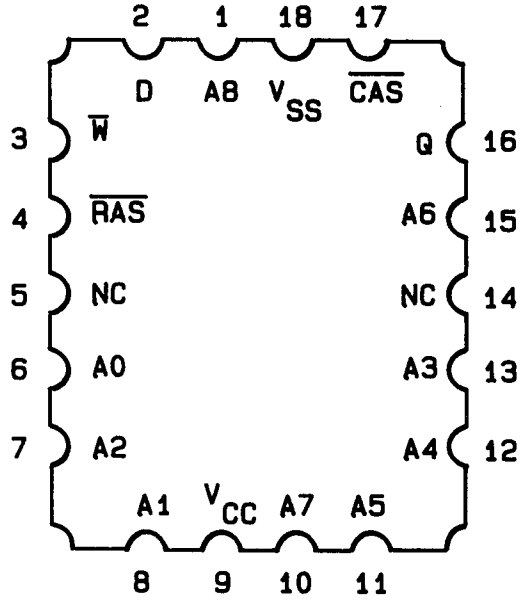


FIGURE 2. Terminal connections.

Device types 01, 02, and 03

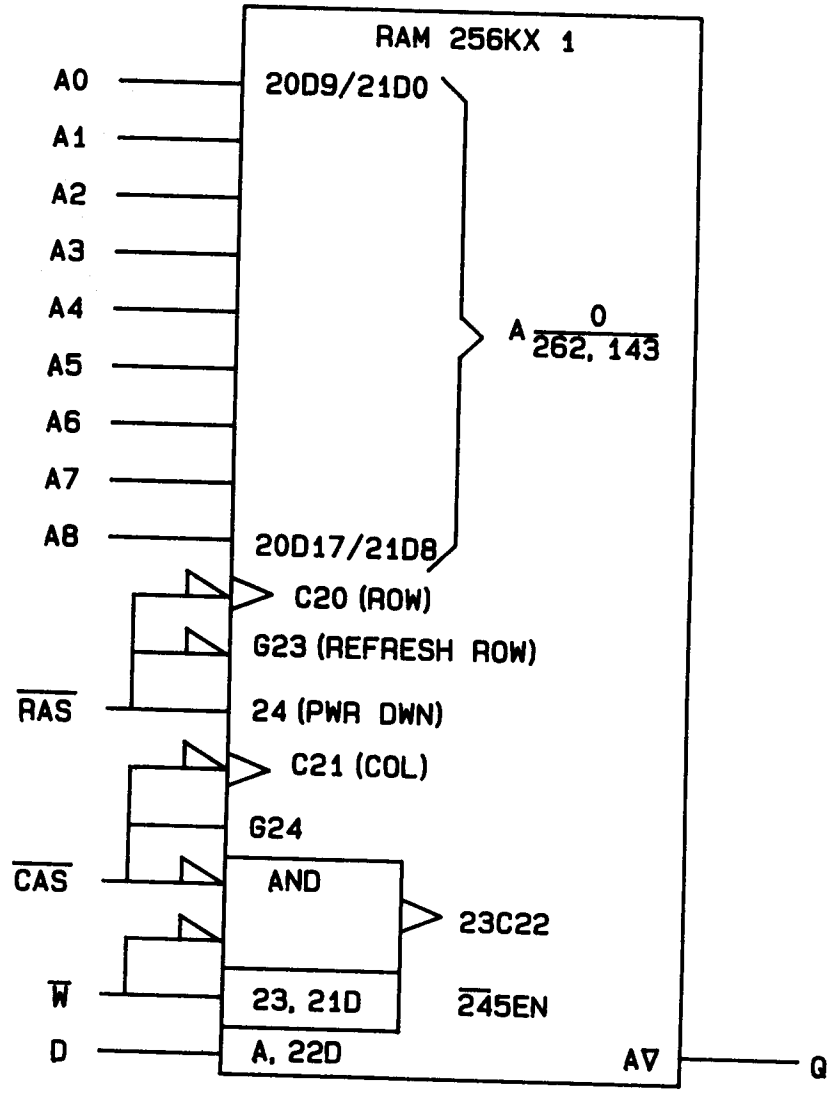


FIGURE 3. Logic diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		85152
		REVISION LEVEL C	SHEET 17

Device types 01, 02, and 03

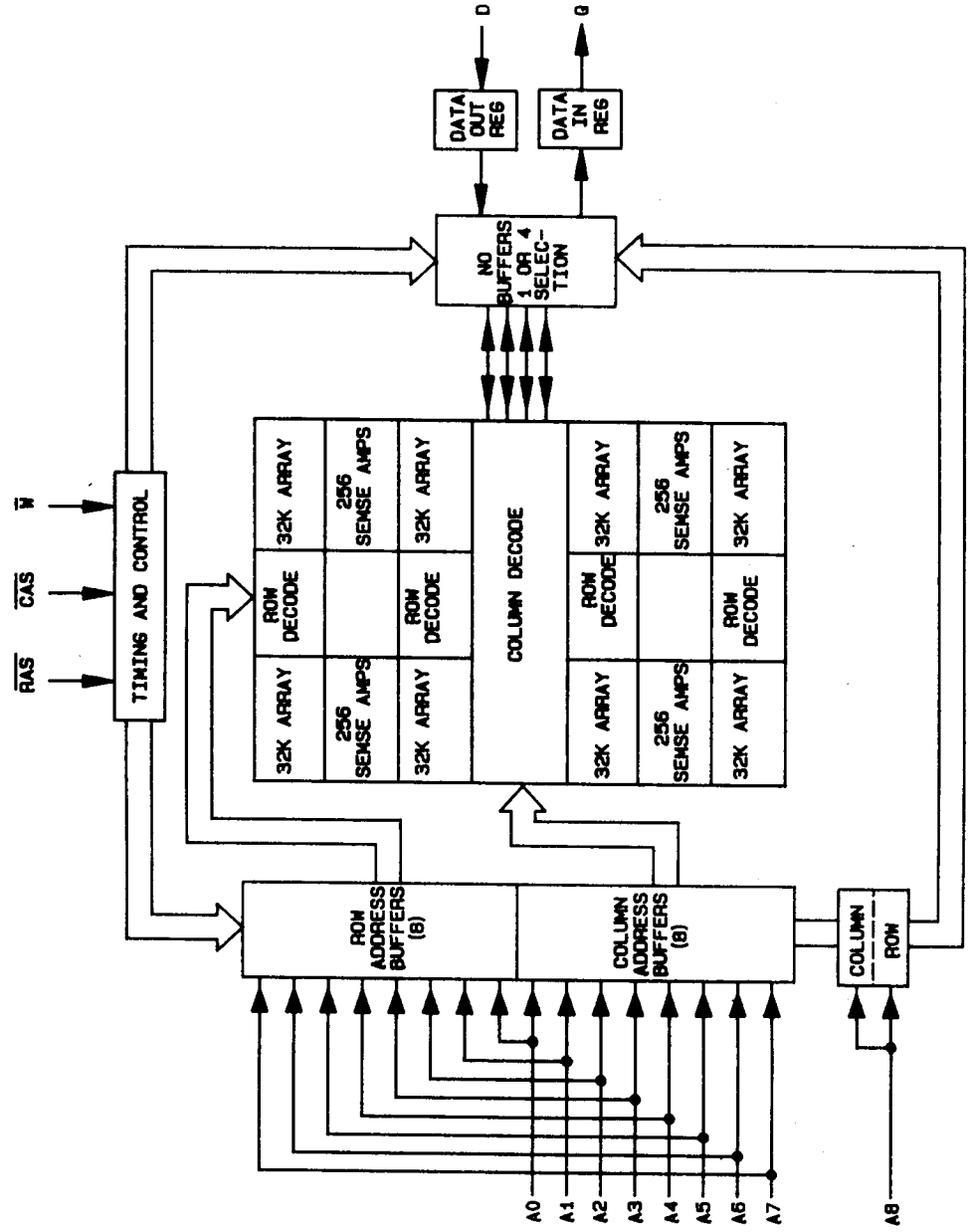
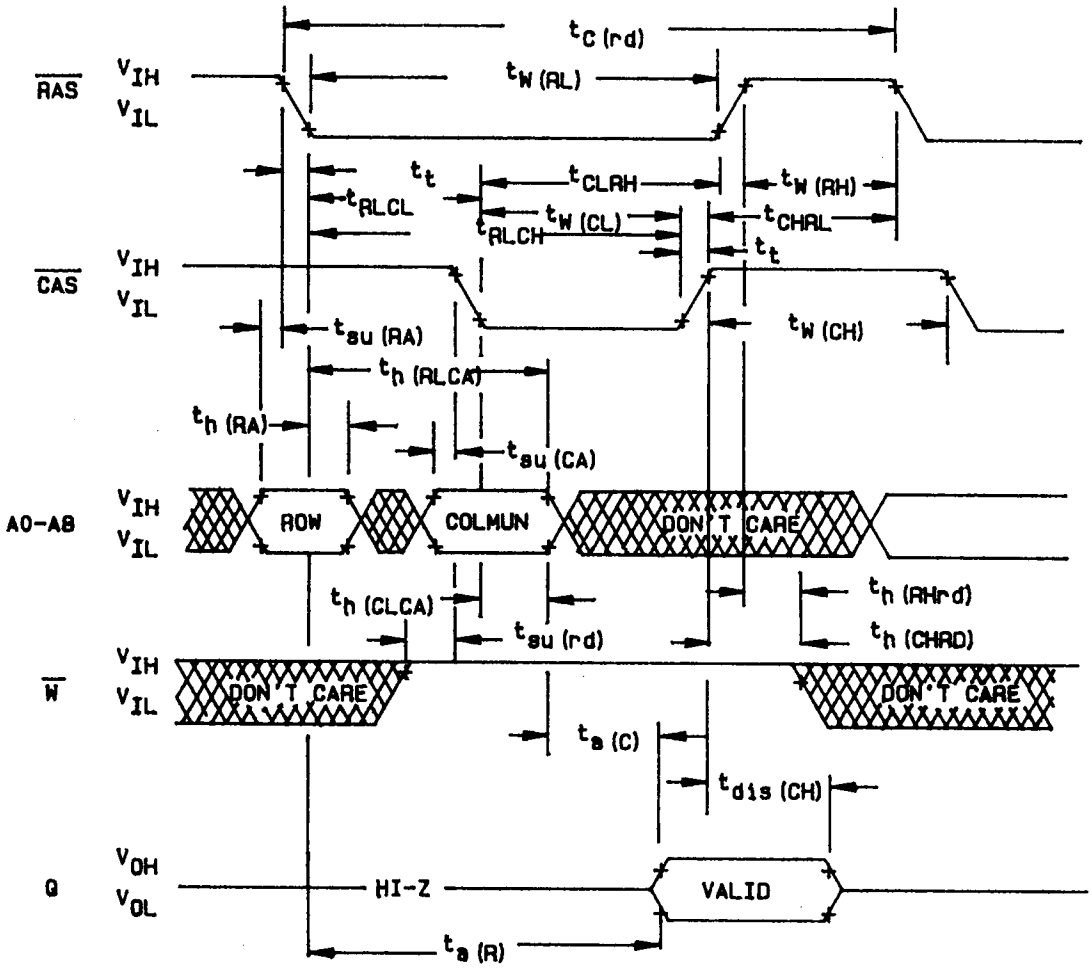


FIGURE 4. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		85152
		REVISION LEVEL C	SHEET 18

Read cycle timing

Device types 01, 02, and 03



NOTE: Outputs are referenced to: Hi-Z to active state, V_{OH} minimum or V_{OL} maximum; active state to Hi-Z, V_{OH} -.5 V or V_{OL} +.5 V.

FIGURE 5. Switching waveforms.

Early cycle timing

Device types 01, 02, and 03

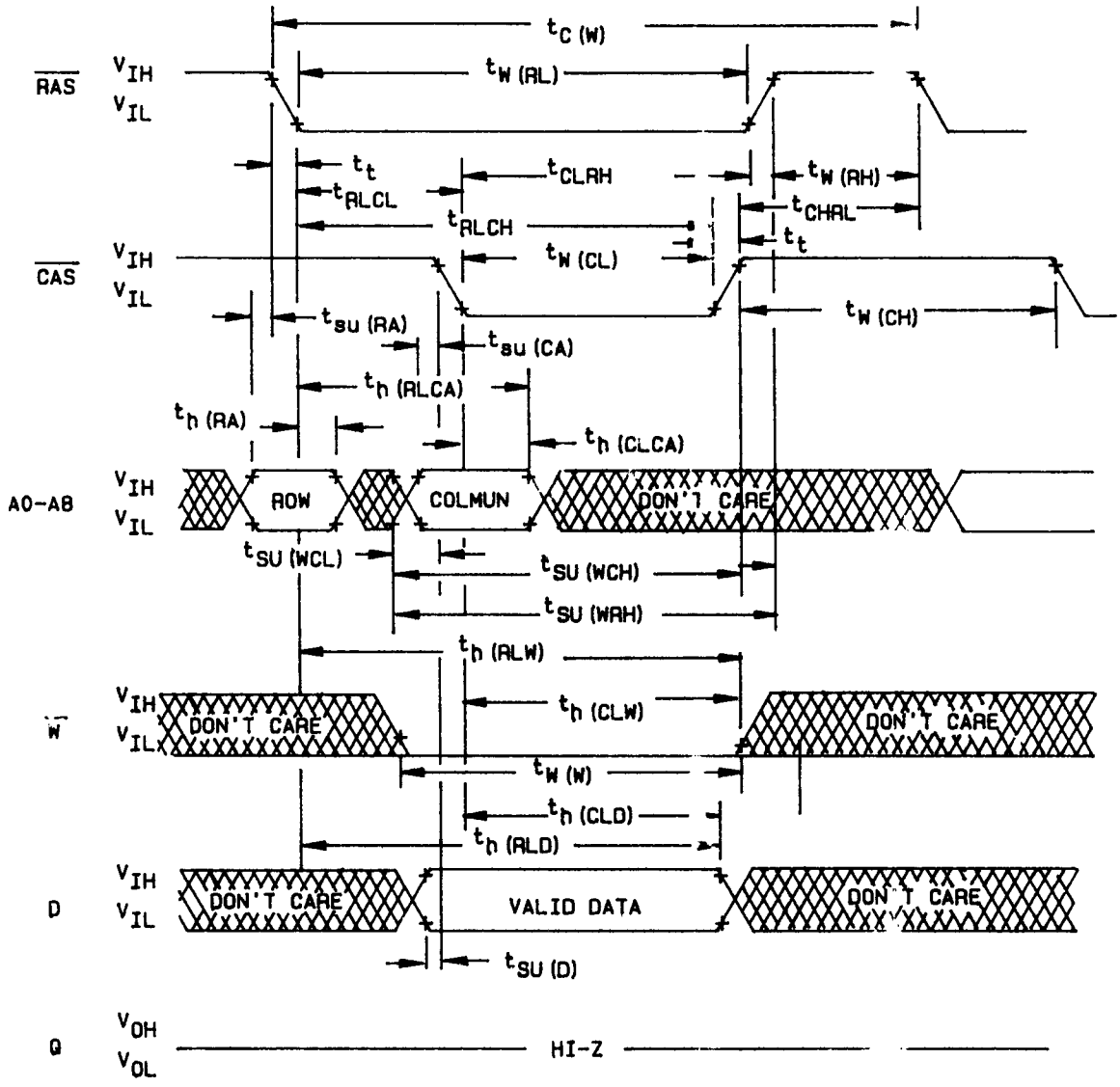
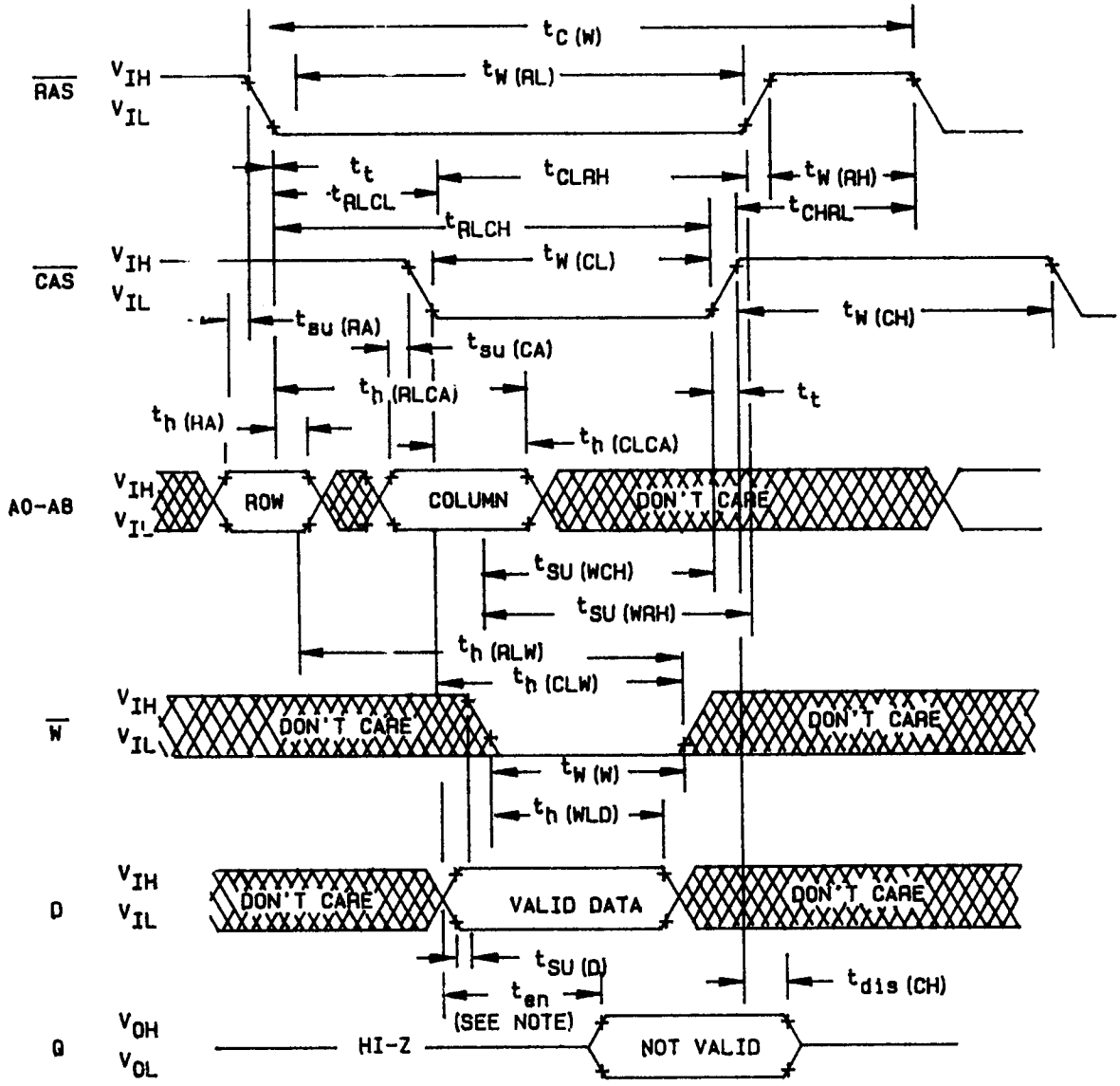


FIGURE 5. Switching waveforms - Continued.

Write cycle timing

Device types 01, 02, and 03



NOTE: The enable time (t_{en}) for a write cycle is equal in duration to the access time from CAS ($t_{a(c)}$) in a read cycle; but the active levels at the output are invalid.

FIGURE 5. Switching waveforms - Continued.

Read-write/read-modify-write cycle timing

Device types 01, 02, and 03

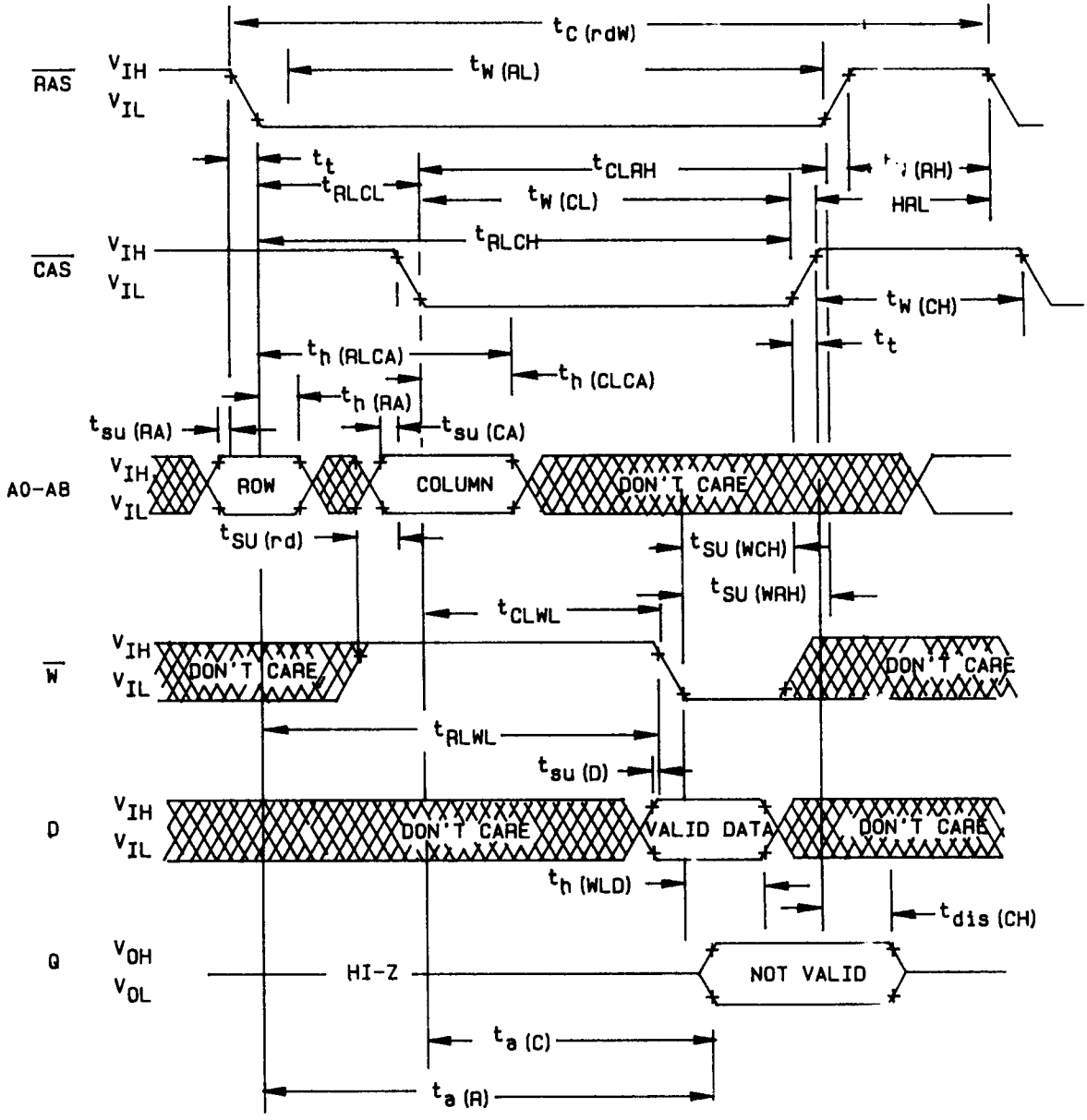


FIGURE 5. Switching waveforms - Continued.

Page-mode read cycle timing

Device types 01, 02, and 03

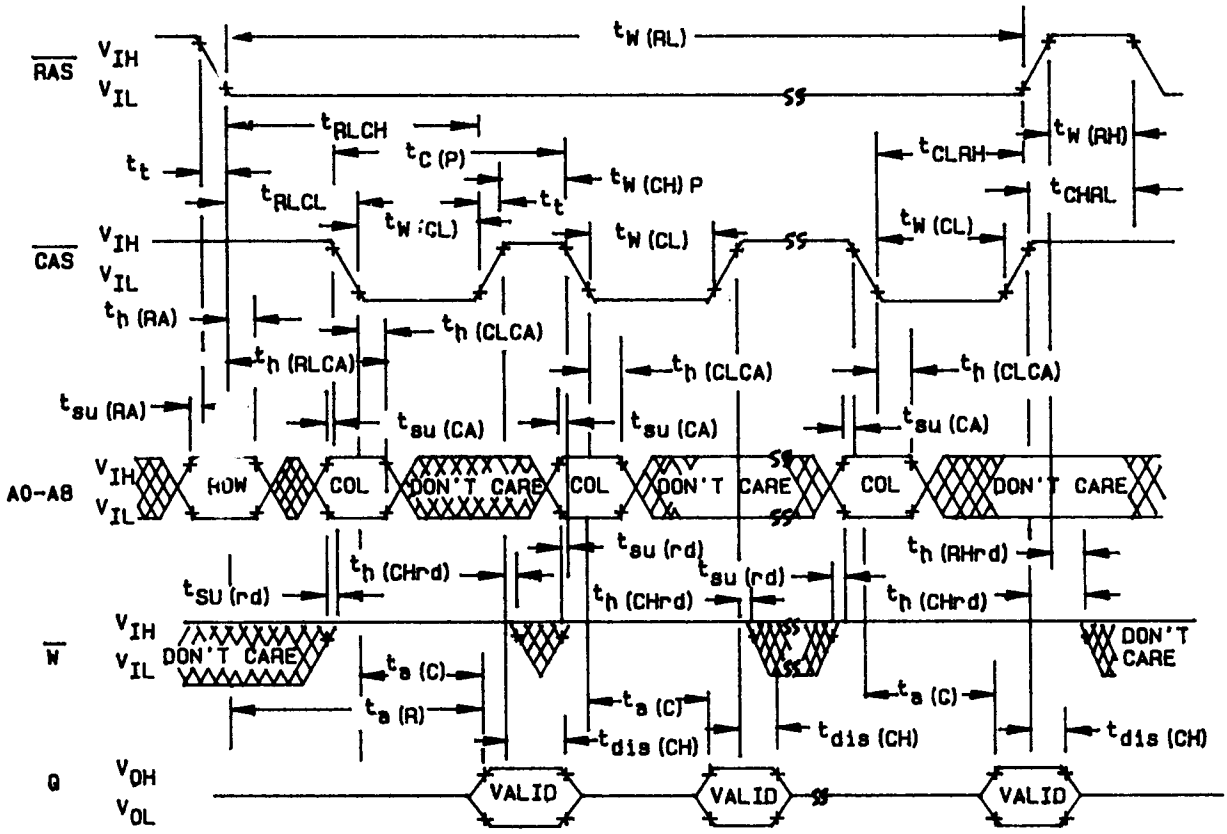


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		85152
		REVISION LEVEL C	SHEET 23

Page-mode write cycle timing

Device types 01, 02, and 03

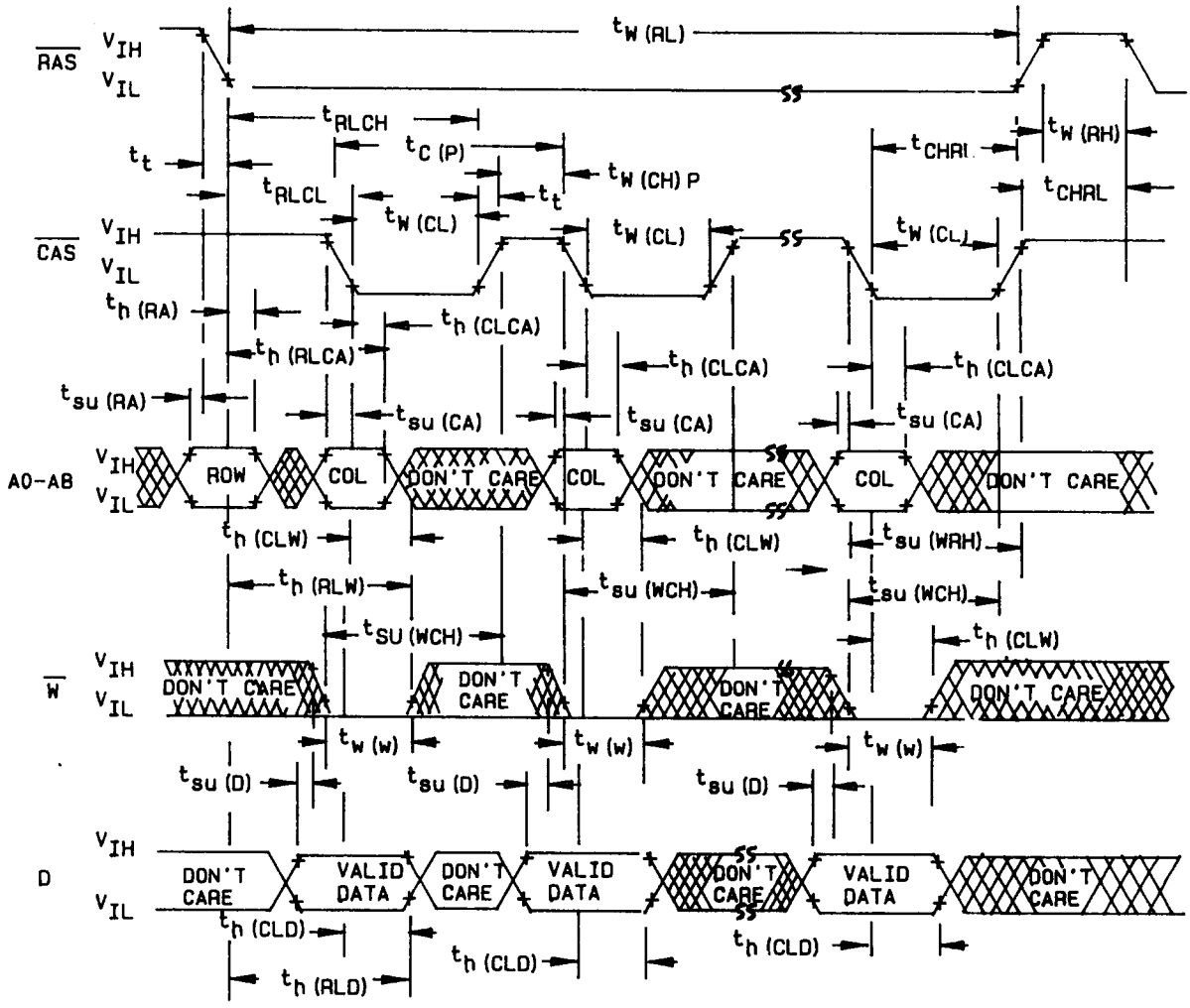


FIGURE 5. Switching waveforms - Continued.

Page-mode read-modify-write cycle timing

Device types 01, 02, and 03

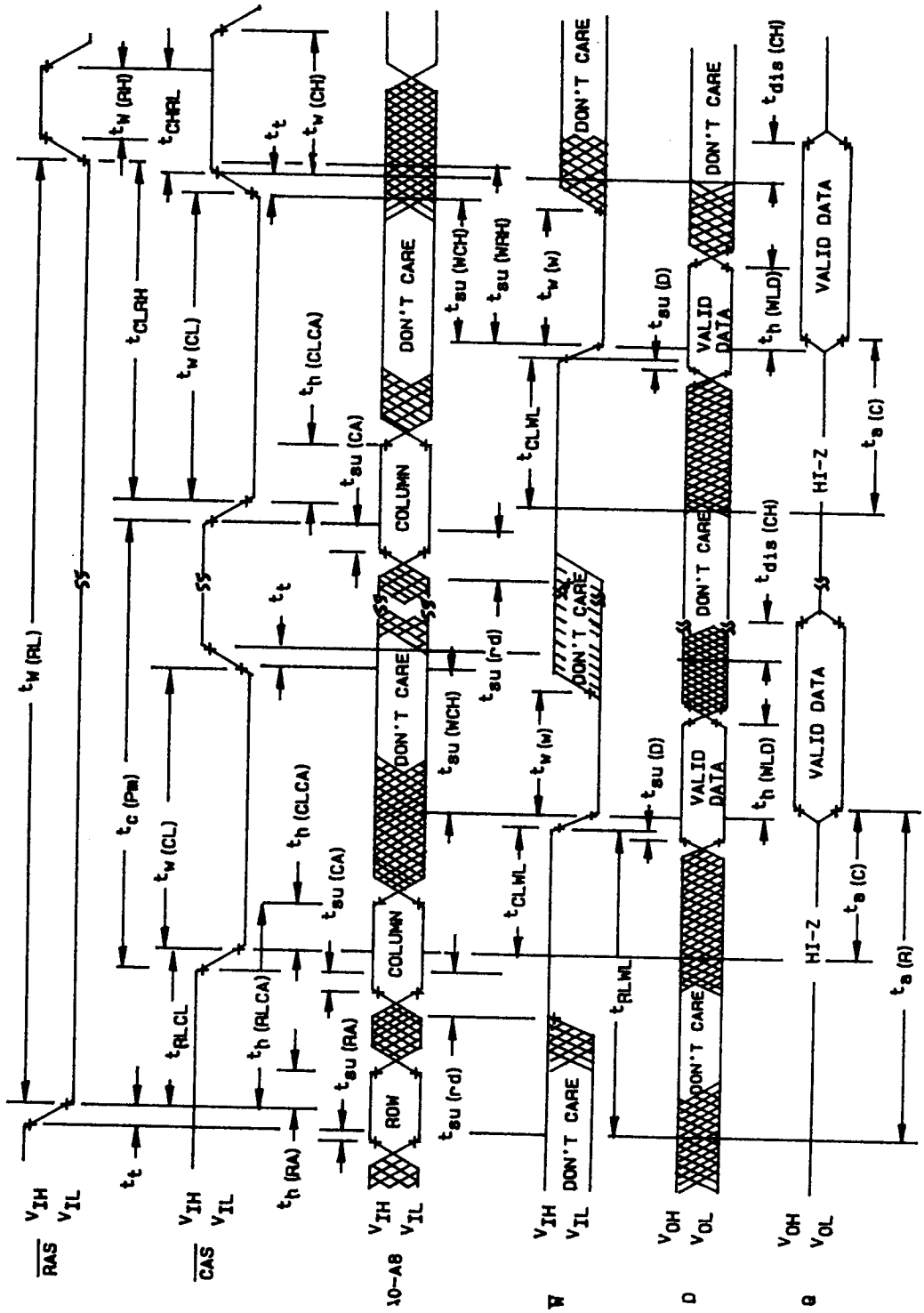


FIGURE 5. Switching waveforms - Continued.

$\overline{\text{RAS}}$-only refresh cycle timing

Device types 01, 02, and 03

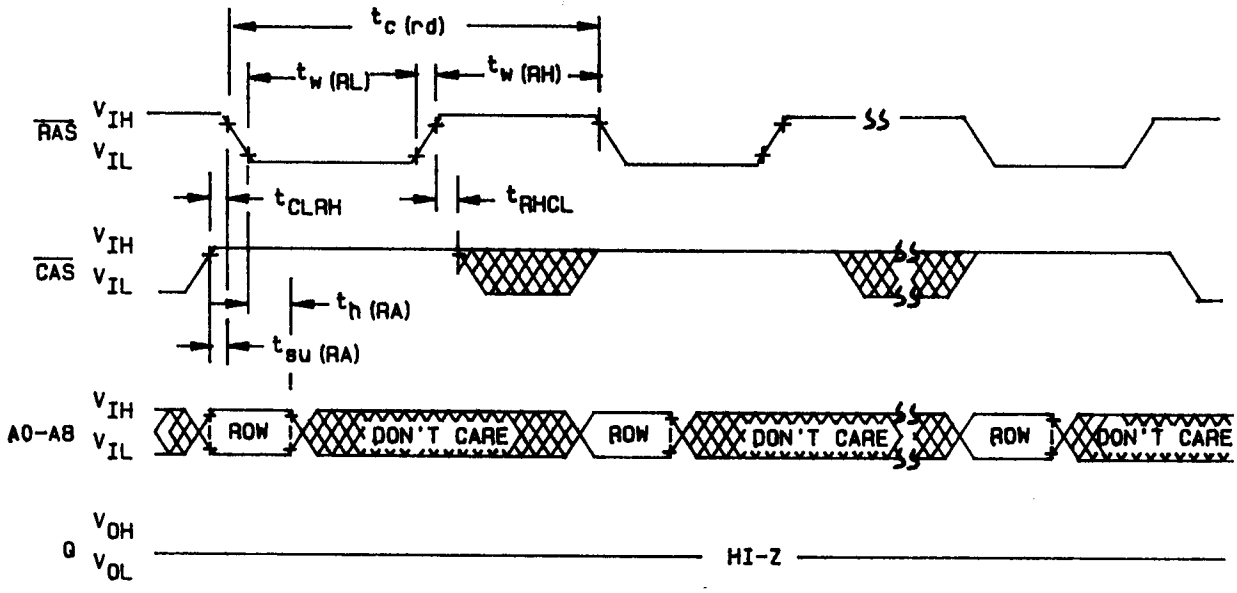


FIGURE 5. Switching waveforms - Continued.

Hidden refresh cycle timing

Device types 01, 02, and 03

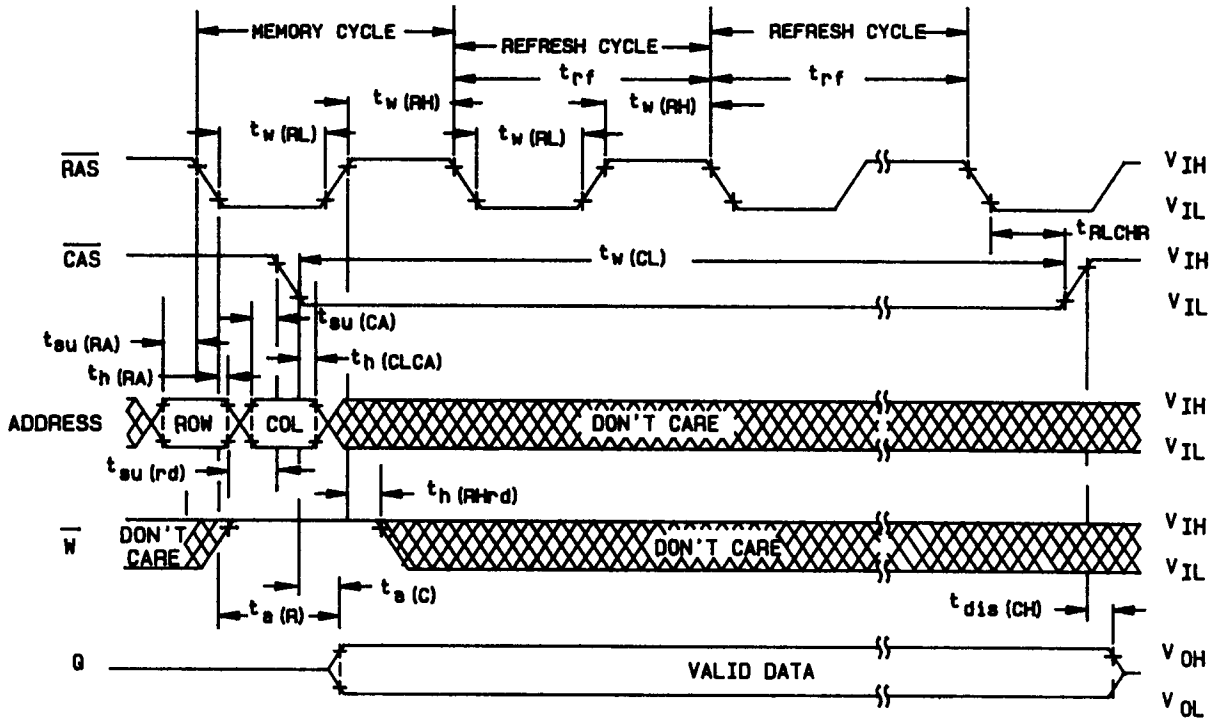


FIGURE 5. Switching waveforms - Continued.

Automatic $\overline{CAS}$ - before $\overline{RAS}$ refresh cycle timing

Device types 01, 02, and 03

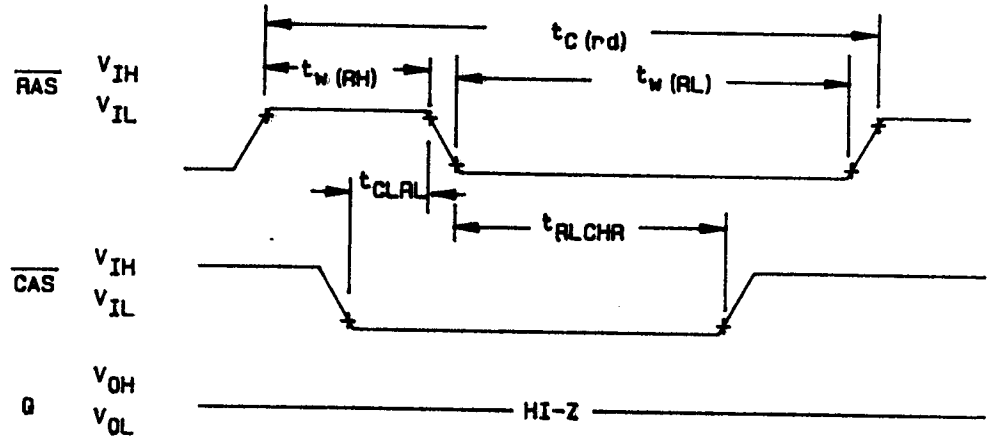


FIGURE 5. Switching waveforms - Continued.

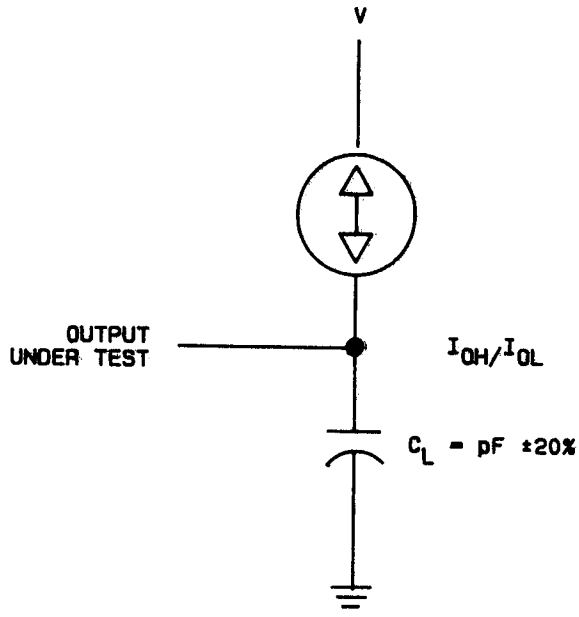


FIGURE 6. Load circuit.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the device specified in this drawing will be replaced by the microcircuit identified as PIN M38510/2460XB*X.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform the Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.