STANDARD MICROSYSTEMS CORPORATION

COM82C501
PRELIMINARY

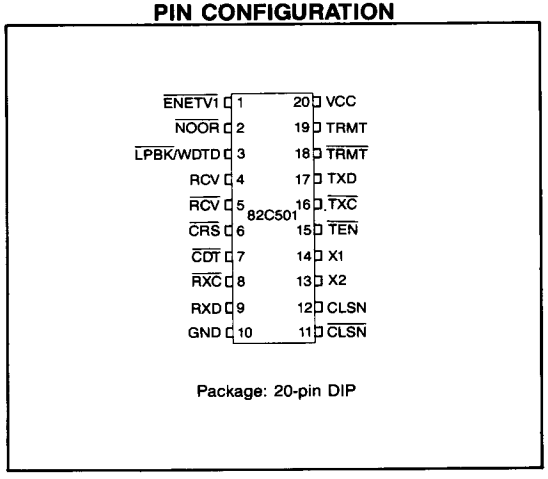
SECTION III

Ethernet™ Serial Interface

FEATURES

- ☐ Direct Replacement for Intel 82501 and 82C501, or SEEQ 8023A
- ☐ Compatible with IEEE 802.3 10BASE5 (Ethernet™) and 10BASE2 (Cheapernet) Specifications
- ☐ 10 Mbps Operation
- ☐ Replaces 8 to 12 MSI Components
- ☐ Manchester Encoding/Decoding and Receive Clock Recovery
- ☐ 10 MHz Transmit Clock Generator
- ☐ Drives/Receives IEEE 802.3 Transceiver Cable (AUI)
- ☐ Defeatable Watchdog Timer Circuit to Prevent Continuous Transmissions
- ☐ Diagnostic Loopback for Network Node Fault Detection and Isolation
- ☐ Direct Interface to the COM82586 LAN Coprocessor and COM82C502 Transceiver
- ☐ Low Power CMOS
- ☐ +5 Volt Only Operation

PIN CONFIGURATION

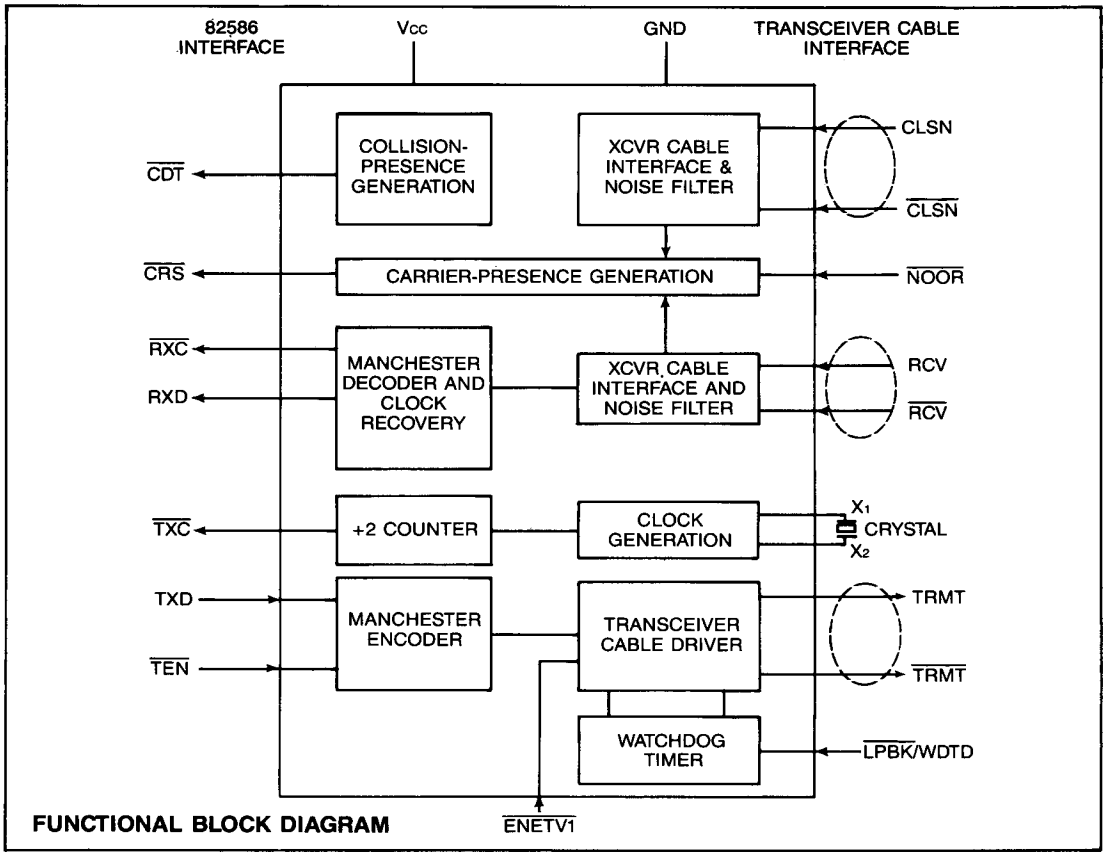


Package: 20-pin DIP

GENERAL DESCRIPTION

The COM82C501 Ethernet™ Serial Interface (ESI) chip is designed to work directly with the COM82586 LAN Coprocessor in IEEE 802.3 (10BASE5 and 10BASE2), 10 Mbps, Local Area Network applications. The major functions of the COM82C501 are to generate the 10 MHz transmit clock for the COM82586, perform Manchester encoding/decoding of the transmitted/received frames, and provide the electrical interface to the Ethernet™ transceiver cable (AUI). Diagnostic loopback control enables the COM82C501 to route the signal to be transmitted from the COM82586 through its Manchester encoding and decoding circuitry and back to the COM82586. The combined loopback capabilities of the COM82586 and COM82C501 result in efficient fault detection and isolation by providing sequential testing of the communications interface. An on-chip watchdog timer circuit (defeatable) prevents the station from locking up in a continuous transmit mode. The COM82C501 is socket compatible with the bipolar Intel 82501, the Seeq 8023A, and the CMOS Intel 82C501.

Ethernet™ is a trademark of the Xerox Corporation.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Ethernet Version 1.0	$\overline{\text{ENETV1}}$	An active low, MOS-level input. When $\overline{\text{ENETV1}}$ is asserted, the TRMT/$\overline{\text{TRMT}}$ pair remains at high differential voltage at the end of transmission. This operation is compatible with the Ethernet Version 1.0 specification. If the $\overline{\text{ENETV1}}$ pin is left floating, an internal pull-up resistor biases the input inactive high.
2	Carrier Sense Option	$\overline{\text{NOOR}}$	An active low, MOS-level input. When $\overline{\text{NOOR}}$ is asserted a valid signal on the collision-presence pair (CLSN/$\overline{\text{CLSN}}$) will not force $\overline{\text{CRS}}$ active low. With $\overline{\text{NOOR}}$ active $\overline{\text{CRS}}$ can only be asserted by the presence of valid data bits on the RCV/$\overline{\text{RCV}}$ pair. If the $\overline{\text{NOOR}}$ pin is floating, an internal pull-up resistor biases the input inactive high.
3	Loopback/Watchdog Timer Disable	$\overline{\text{LPBK}}$/ WDTD	An active low, TTL-level control signal enables the loopback mode. In loopback mode serial data on the TXD input is routed through the 82C501 internal circuits and back to the RXD output without driving the TRMT/$\overline{\text{TRMT}}$ output pair to the transceiver cable. During loopback $\overline{\text{CDT}}$ is asserted at the end of each transmission to simulate the SQE test. An input voltage of 12V $\pm$ 10% through a 4 KΩ resistor will disable the on-chip watchdog timer.
4 5	Receiver Pair	RCV $\overline{\text{RCV}}$	A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV will be negative-going to indicate the beginning of a frame. The last transition should be positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.

PIN NO.	NAME	SYMBOL	FUNCTION
6	Carrier Sense	$\overline{CRS}$	An active low, MOS-level output to notify the COM82586 that there is activity on the coaxial cable. The signal is asserted when valid data or a collision-presence signal from the transceiver is present. It is deasserted at the end of a frame; or when the end of the collision-presence signal is detected, synchronous with $\overline{RXC}$. After transmission, once deasserted, CRS will not be reasserted again for a period of 5 μs minimum or 7 μs maximum, regardless of any activity on the collision-presence signal (CLSN/$\overline{CLSN}$) and RCV/$\overline{RCV}$ inputs.
7	Collision Detect	$\overline{CDT}$	An active-low, MOS-level signal which drives the $\overline{CDT}$ input of the COM82586 controller. It is asserted as long as there is activity on the collision pair (CLSN/$\overline{CLSN}$), and during SQE (heartbeat) test in loopback.
8	Receive Clock	$\overline{RXC}$	A 10 MHz MOS level clock output with 5 ns rise and fall times. This output is connected to the COM82586 receive clock input $\overline{RXC}$. There is a maximum 1.2 μs delay at the beginning of a frame reception before the clock recovery circuit gains lock. During idle (no incoming frames) $\overline{RXC}$ is forced low.
9	Receive Data	RXD	A MOS-level output tied directly to the RXD input of the COM82586 controller and sampled by the COM82586 at the negative edge of $\overline{RXC}$. The bit stream received from the transceiver cable is Manchester decoded prior to being transferred to the controller. This output remains high during idle.
10	Ground	GND	Reference.
12 11	Collision Pair	CLSN $\overline{CLSN}$	A differentially driven input pair tied to the collision-presence pair of the Ethernet transceiver cable. The collision-presence signal is a 10 MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going to indicate the end of the signal.
14 13	Clock Crystal	X_1 X_2	20 MHz crystal inputs. When X_2 is floated, X_1 can be used as an external MOS level input clock.
15	Transmit Enable	$\overline{TEN}$	An active low, TTL level signal synchronous to TXC that enables data transmission to the transceiver cable and starts the watchdog timer. $\overline{TEN}$ can be driven by the $\overline{RTS}$ from the COM82586.
16	Transmit Clock	$\overline{TXC}$	A 10 MHz MOS level clock output with 5 ns rise and fall times. This clock is connected directly to the $\overline{TXC}$ input of the COM82586.
17	Transmit Data	TXD	A TTL-level input signal that is directly connected to the serial data output, TXD, of the COM82586.
19 18	Transmit Pair	TRMT $\overline{TRMT}$	A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transmission, which is always positive at TRMT, the differential voltage is slowly reduced to zero volts in a series of steps. If $\overline{ENETV1}$ is asserted this voltage stepping is disabled.
20	Power Supply	V_{CC}	+5V ± 10%.