# QUAD SERIAL BACKPLANE DEVICE S2004

## FEATURES

- Broad operating rate range (.98 - 1.3 GHz)
  - 1062 MHz (Fibre Channel)
  - 1250 MHz (Gigabit Ethernet) line rates
  - 1/2 Rate Operation
- Quad Transmitter with phase-locked loop (PLL) clock synthesis from low speed reference
- Quad Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- On-chip 8B/10B line encoding and decoding for four separate parallel 8-bit channels
- 32-bit parallel TTL interface with internal series terminated outputs
- Low-jitter serial PECL interface
- Individual local loopback control
- JTAG 1149.1 Boundary scan on low speed I/O signals
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 2.5 W power dissipation
- Compact 23mm x 23mm 208 TBGA package

## APPLICATIONS

- Ethernet Backbones
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

## GENERAL DESCRIPTION

The S2004 facilitates high-speed serial transmission of data in a variety of applications including Gigabit Ethernet, Fibre Channel, serial backplanes, and proprietary point to point links. The chip provides four separate transceivers which can be operated individually or locked together for an aggregate data capacity of >4 Gbps.

Each bi-directional channel provides 8B/10B coding/decoding, parallel to serial and serial to parallel conversion, clock generation/recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip quad receive PLL is used for clock recovery and data retiming on the four independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates 2.5 watts.

Figure 1 shows the S2004 and S2204 in a Gigabit Ethernet application. Figure 2 combines the S2004 with a crosspoint switch to demonstrate a serial backplane application. Figure 3 is the input/output diagram. Figures 4 and 5 show the transmit and receive block diagrams, respectively.

***Figure 1. Typical Quad Gigabit Ethernet Application***

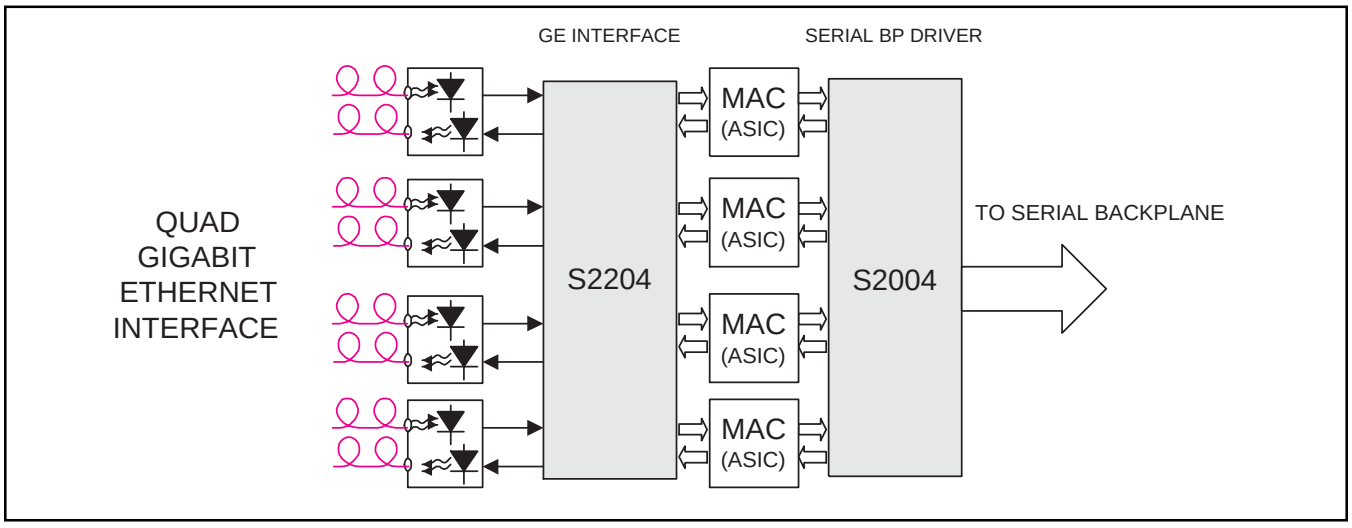


***Figure 2. Typical Backplane Application***

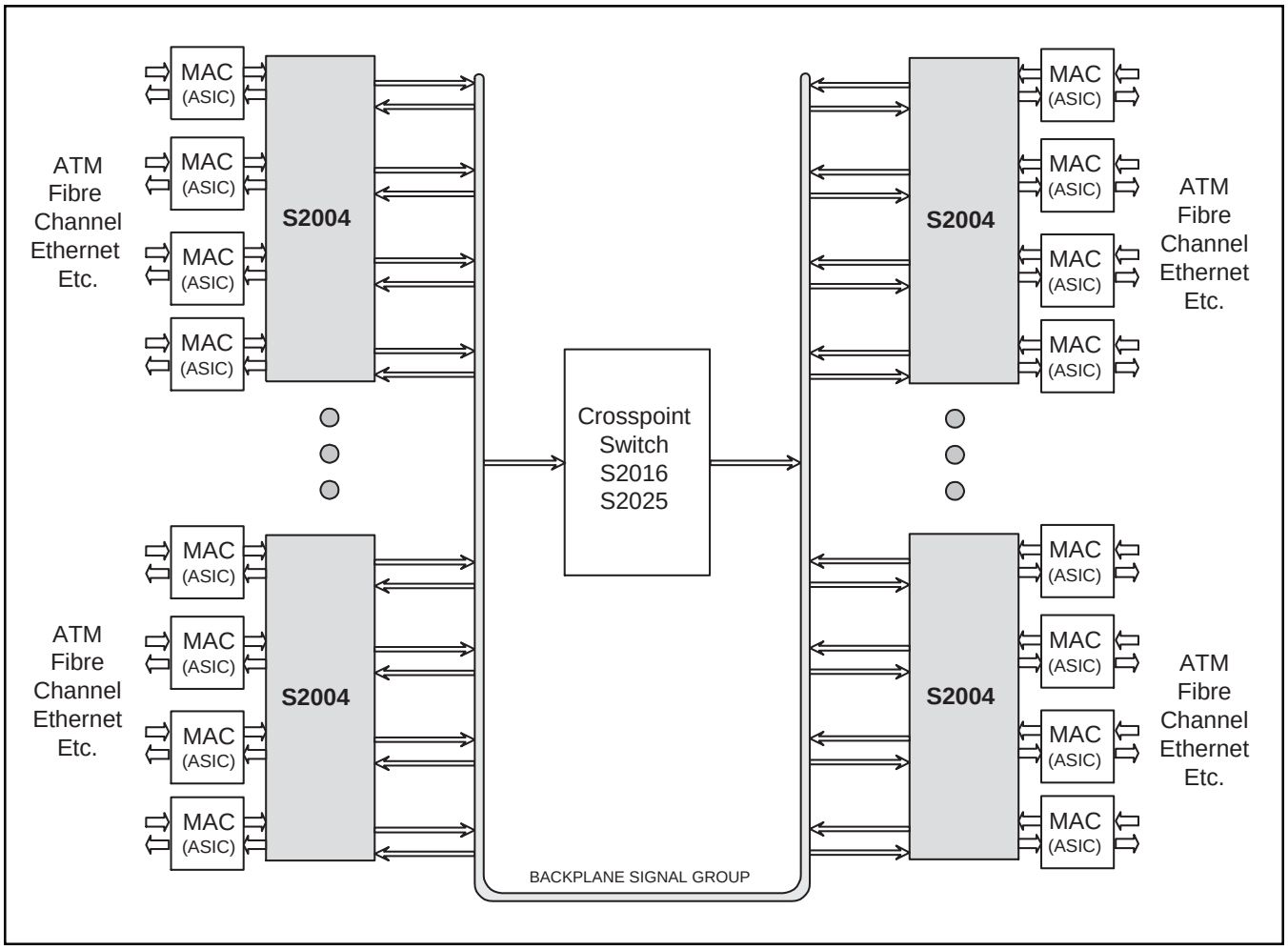


***Figure 3. S2004 Input/Output Diagram***

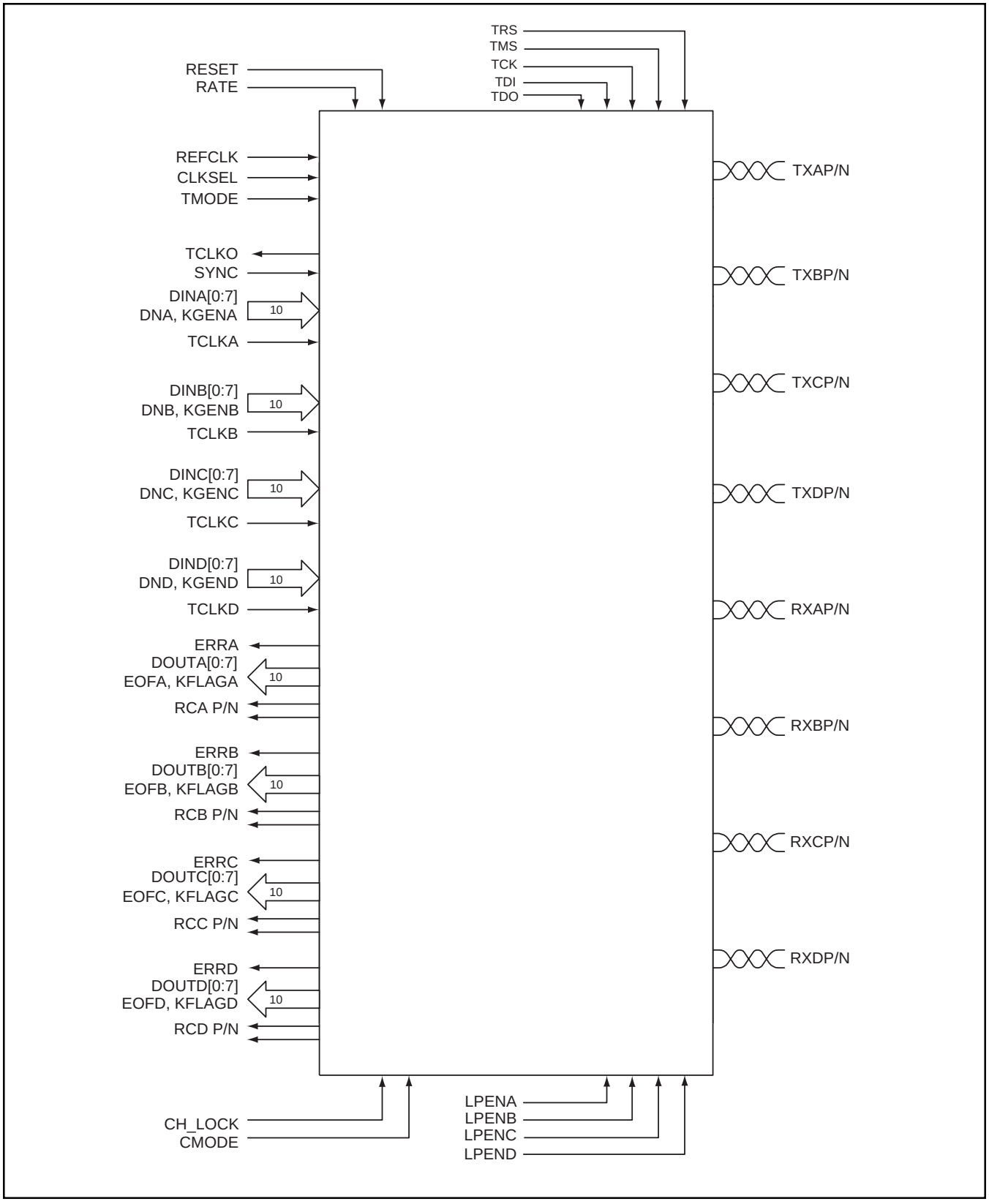


***Figure 4. Transmitter Block Diagram***

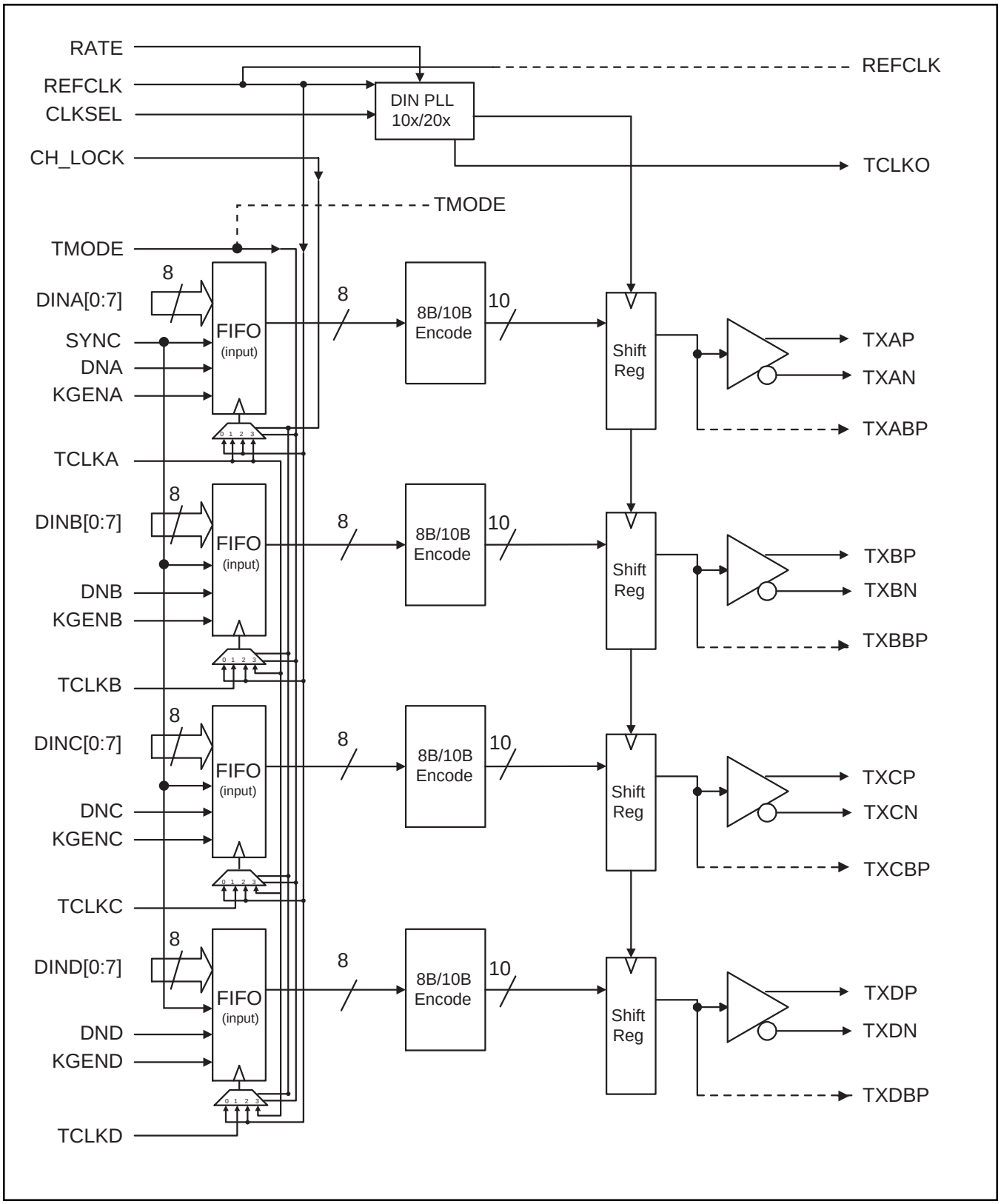
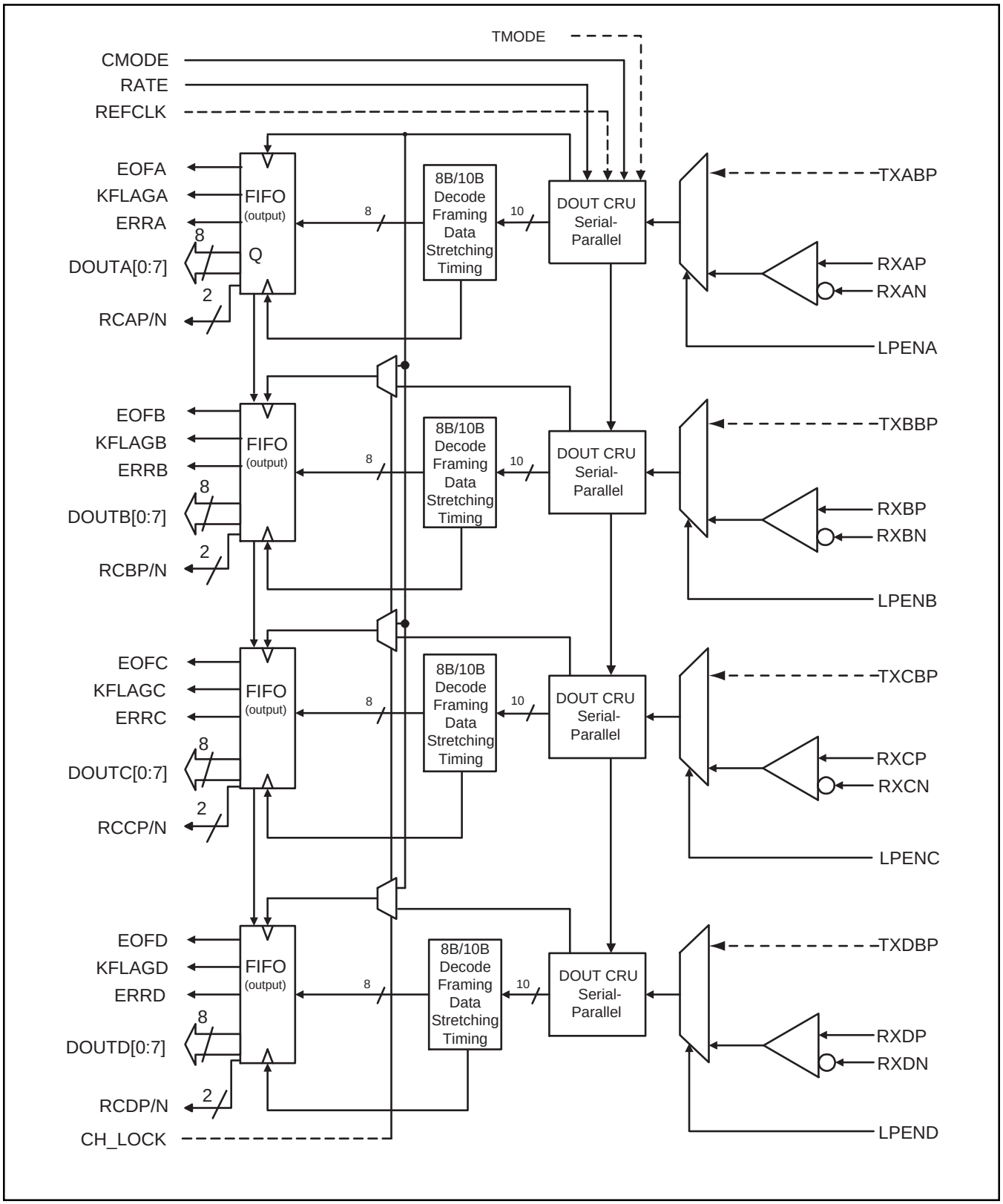


***Figure 5. Receiver Block Diagram***



## TRANSMITTER DESCRIPTION

The transmitter section of the S2004 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Four channels are provided with a variety of options regarding input clocking and loopback. The transmitters can operate in the range of .98 GHz to 1.3 GHz, 10 or 20 times the reference clock frequency.

### Data Input

The S2004 has been designed to simplify the parallel interface data transfer and provides the utmost in flexibility regarding clocking of parallel data. The S2004 incorporates a unique FIFO structure on both the parallel inputs and the parallel outputs which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device. Data can also be clocked in using the REFCLK.

Data is input to each channel of the S2004 nominally as a 10 bit wide word. This consists of eight data bits of user data, KGEN, and DN. An input FIFO and a clock input, TCLKx, are provided for each channel of the S2004. The device can operate in two different modes. In CHANNEL-LOCKED mode all four bytes of input data are clocked into their respective FIFOs using a common clock. The S2004 can be configured to use either the TCLKA (TCLK MODE) input or the REFCLK input (REFCLK MODE). In NORMAL mode, each byte of data is clocked into its FIFO with the TCLKx provided with each byte. Table 1 provides a summary of the input modes for the S2004.

Operation in the TCLK MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the parallel 10-bit interface. The TCLK signal is used to clock the data into an internal holding register and the S2004 synchronizes its internal data flow to insure stable operation. However, regardless of the clock mode, REFCLK is always the VCO reference clock. This facilitates the provision of a clean reference clock resulting in minimum jitter on the serial output. The TCLK must be frequency locked to REFCLK, but may have an arbitrary phase relationship. Adjustment of internal timing of the S2004 is performed during reset. Once synchronized, the user must insure that the timing of the TCLK signal does not change by more than ± 3 ns relative to the REFCLK.

Figure 6 demonstrates the flexibility afforded by the S2004. A low jitter reference is provided directly to the S2004 at either 1/10 or 1/20 the serial data rate. This insures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. The frequency of this output is constant at the parallel word rate, 1/10 the serial data rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be buffered as required without concern about added delay. There is no phase requirement between TCLKO and TCLKx, which is provided back to the S2004, other than that they remain within ± 3ns of the phase relationship established at reset.

***Table 1. Input Modes***

| CHANLOCK | TMODE | Operation |
|---|---|---|
| 0 | 0 | NORMAL REFCLK MODE. REFCLK used to clock data into FIFOs for all channels. (No receiver byte de-skew.) |
| 0 | 1 | NORMAL TCLK MODE. TCLKx used to clock data into FIFOs for all channels. (No receiver byte de-skew.) |
| 1 | 0 | CHANNEL LOCK MODE. REFCLK MODE. REFCLK used to clock data into FIFOs for all channels. (Receiver byte de-skew active.) |
| 1 | 1 | CHANNEL LOCK MODE. TCLKA MODE. TCLKA used to clock data into FIFOs for all channels. (Receiver byte de-skew active.) |

1. Note that internal synchronization of FIFOs is performed upon de-assertion of RESET or when the synchronization pattern is generated (SYNC = 1 DNx = 1).

***Figure 6. DINx Data Clocking with TCLK***

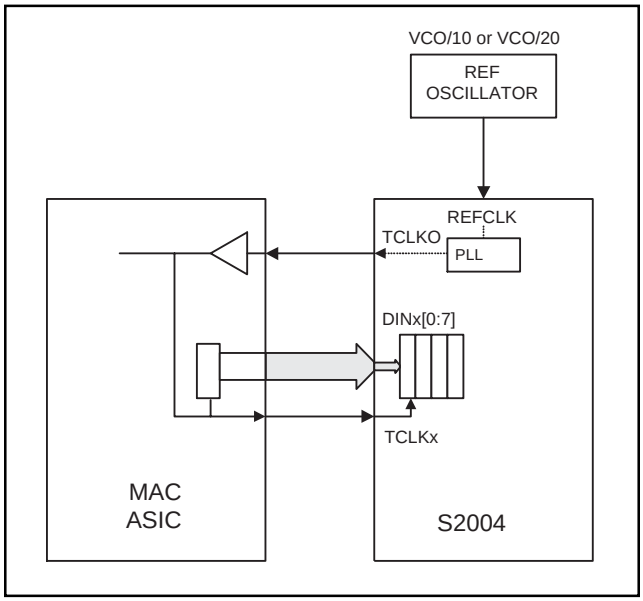
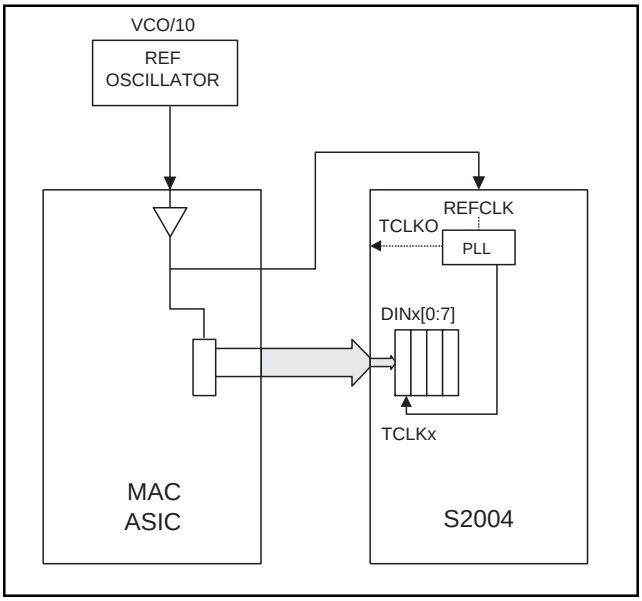



***Figure 7. DIN Clocking with REFCLK***




The S2004 also supports the traditional REFCLK (TBC) clocking found in many Fibre Channel and Gigabit Ethernet applications and is illustrated in Figure 7.

## Half Rate Operation

The S2004 supports full and 1/2 rate operation for all modes of operation. When RATE is LOW, the S2004 serial data rate equals the VCO frequency. When RATE is HIGH, the VCO is divided-by-2 before being provided to the chip. Thus the S2004 can support Fibre Channel and serial backplane functions at both full and 1/2 the VCO rate. (See Table 5.)

## 8B/10B Coding

The S2004 provides 8B/10B line coding for each channel. The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

The 8B/10B transmission code includes D-characters, used for data transmission, and K-characters, used for control or protocol functions. Each D-character and K-character has a positive and a negative parity version. The parity of each codeword is selected by the encoder to control the running disparity of the data stream. K-character generation is controlled individually for each channel using the KGENx input. When KGEN is asserted the data on the parallel input is mapped into the corresponding control character. The parity of the K-character is selected to minimize running disparity in the serial data stream. Table 3 lists the K characters supported by the S2004 and identifies the mapping of the DIN[7:0] bits to each character.

[1] 1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

In order to provide interface compatibility to non-AMCC serial backplane transceivers, the S2004 can also generate a unique sync character consisting of 16 consecutive K28.5 characters. This event is initiated by the simultaneous assertion of SYNC and DN. The SYNC character may start with either a positive or negative parity K28.5. (Depending on the current running disparity.) The parity of the second and third K28.5 are inverse with respect to a valid 8B/10B sequence. Parity of the remaining K28.5 are 8B/10B compliant. Thus the parity of the K28.5 pattern consists of + + - - + - + - + - + - + - or - - + + - + - + - + - + - +.

When operating in the channel locked mode, the KGENx and DNx inputs must be driven for each channel. The SYNC input is common to all four channels. Table 2 identifies the S2004 transmit control signals.

The special SYNC generation commences on the first cycle in which SYNC and DN=1 and continues for 16 cycles. During this period, the SYNC, KGEN, and DN inputs are ignored (assertion of DN and SYNC during this period will not prolong or re-initialize the special sync character generation).

## Frequency Synthesizer (PLL)

The S2004 synthesizes a serial transmit clock from the reference signal. Upon startup, the S2004 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

***Table 2. Transmitter Control Signals***

| SYNC | KGENx | DNx | S2004 Output |
|---|---|---|---|
| 0 | 0 | 0 | Encoded Parallel Data. |
| 0 | 0 | 1 | K28.5 Character. |
| 0 | 1 | 1 | K Character as defined by Table 3 and DIN[7:0]. |
| 1 | X | 1 | Special 16 word SYNC character generated and resets the transmit FIFO. |

***Table 3. K Character Generation (DNx = 1 KGENx =1 SYNC = 0)***

| K Character | DIN[7:0] | KGEN | Current RD+ | Current RD- | Comments |
|---|---|---|---|---|---|
| | | | abcdei fghj | abcdei fghj | |
| K28.0 | 000 11100 | 1 | 110000 1011 | 001111 0100 | |
| K28.1 | 001 11100 | 1 | 110000 0110 | 001111 1001 | |
| K28.2 | 010 11100 | 1 | 110000 1010 | 001111 0101 | |
| K28.3 | 011 11100 | 1 | 110000 1100 | 001111 0011 | |
| K28.4 | 100 11100 | 1 | 110000 1101 | 001111 0010 | |
| K28.5 | 101 11100 | 1 | 110000 0101 | 001111 1010 | Sync Character |
| K28.6 | 110 11100 | 1 | 110000 1001 | 001111 0110 | |
| K28.7 | 111 11100 | 1 | 110000 0111 | 001111 1000 | |
| K23.7 | 111 10111 | 1 | 000101 0111 | 111010 1000 | |
| K27.7 | 111 11011 | 1 | 001001 0111 | 110110 1000 | |
| K29.7 | 111 11101 | 1 | 010001 0111 | 101110 1000 | |
| K30.7 | 111 11110 | 1 | 100001 0111 | 011110 1000 | |

***Table 4. Data to 8B/10B Alphabetic Representation***

| | Data Byte | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| DIN[0:9] or DOUT[0:9] | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 8B/10B Alphanumeric Representation | a | b | c | d | e | i | f | g | h | j |

## Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to insure that the clock recovery units can lock to the serial data.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL = 1. In both cases the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate. See Table 5.

***Table 5. Operating Rates***

| RATE | CLKSEL | REFCLK Frequency | Serial Output Rate | TCLKO Frequency |
|---|---|---|---|---|
| 0 | 0 | SDR/10 | 0.98-1.3 GHz | SDR/10 |
| 0 | 1 | SDR/20 | 0.98-1.3 GHz | SDR/10 |
| 1 | 0 | SDR/10 | 0.49-0.65 GHz | SDR/10 |
| 1 | 1 | SDR/20 | 0.49-0.65 GHz | SDR/10 |

Note: SDR = Serial Data Rate.

## Serial Data Outputs

The S2004 provides LVPECL level serial outputs. The serial ouputs do not require output pulldown resistors. Outputs are designed to perform optimally when AC-coupled.

When operating in the CHAN-LOCK MODE, the user must insure that the path length of the four high speed serial data signals are matched to within 50 serial bit times of delay. Failure to meet this requirement may result in bit errors in the received data or in byte misalignment.

In addition to path length induced timing skew, the S2004 can tolerate up to ±3 ns of phase drift between channels after deskewing the outputs.

## Test Functions

The S2004 can be configured for factory test to aid in functional testing of the device. When in the test mode, the internal transmit and receive voltage-controlled oscillator (VCO) is bypassed and the reference clock substituted. This allows full functional testing of the digital portion of the chip or bypassing the internal synthesized clock with an external clock source. (See Other Operating Modes section.)

## Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TCLK to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET signal. The transmit FIFO is also reset when the special synchronization pattern (SYNC=1, DN=1) is generated. TCLKO will operate normally regardless of the state of RESET.

## RECEIVER DESCRIPTION

Each receiver channel is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 5.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2004 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

The S2004 provides the capability to operate with all four channels locked together (CHANNEL LOCK mode). Channel lock process and status reporting is described below.

### Data Input

A differential input receiver is provided for each channel of the S2004. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for each channel is enabled by its respective LPEN input.

The high speed serial inputs to the S2004 are internally biased to VDD-1.3V. All that is required externally is AC-coupling and line-to-line differential termination.

### Clock Recovery Function

Clock recovery is performed on the input data stream for each channel of the S2004. The receiver PLL has been optimized for the anticipated needs of Serial Backplane systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs. If at any time the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This allows the VCO to maintain the correct frequency in the absence of data.

The 'lock to reference' frequency criteria insure that the S2004 will respond to variations in the serial data input frequency (compared to the reference frequency). The new Lock State is dependent upon the current lock state, as shown in Table 6.

*Table 6. Lock to Reference Frequency Criteria*

| Current Lock State | PLL Frequency (vs. REFCLK) | New Lock State |
|---|---|---|
| Locked | < 488 ppm | Locked |
| | 488 to 732 ppm | Undetermined |
| | > 732 ppm | Unlocked |
| Unlocked | < 244 ppm | Locked |
| | 244 to 366 ppm | Undetermined |
| | > 366 ppm | Unlocked |

The run-length criteria insure that the S2004 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 - 128 may or may not, depending on how the data aligns across byte boundaries.

If both the off-frequency detect circuitry test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. When lock is achieved, LOCK-DET is asserted on the ERR, EOF, and KFLAG status lines. It is possible for the run length test to be satisfied due to noise on the inputs, even if no signal is present. In this case the lock detect status may periodically assert as the VCO frequency approaches that of the REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RCxP/N outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

When operating in independent mode, PLL lock status for each channel is indicated by a 1-0-1 on its respective ERR, EOF, and KFLAG outputs, respectively. When operating in the CHANNEL LOCK mode, PLL locking of all four channels must be accomplished before byte-skewing is achieved and "in sync" status is indicated on the ERR, EOF, and KFLAG outputs.

### Reference Clock Input

A single reference clock, which serves both transmitter and receiver, must be provided from a low jitter clock source. The frequency of the received data stream (divided-by -10 or -20) must be within 200 ppm of the reference clock to insure reliable locking of the receiver PLL.

## Serial to Parallel Conversion

Once bit synchronization has been attained by the S2004 CRU, the S2004 must synchronize to the 10 bit word boundary. Word synchronization in the S2004 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2004 will detect and byte-align to either polarity of the K28.5. Each channel of the S2004 will detect and align to a K28.5 anywhere in the data stream. Two modes of operation are supported. For NORMAL mode operation, the presence of a K28.5 is indicated for each channel by the assertion of the EOFx signal.

For CHANNEL-LOCK operation, the S2004 must provide an additional level of synchronization to insure that differences in delay encountered by the four channels do not result in parallel output data from each channel leading or lagging by one parallel clock cycle. In CHANNEL LOCK, assertion of DNA results in the K28.5 being transmitted simultaneously on all four channels. Each receiver provides a FIFO buffer and adjusts the delay through this buffer to insure that the first data following the K28.5 is output simultaneously from the receiver on the parallel interface. The reception of a K28.5 character is indicated on the EOFA signal. Table 7 details the function of the EOF, KFLAG, and ERR pins in status reporting. For CHANNEL-LOCK operation, a single output clock, RCA P/N, is provided synchronous with the data. The other RCx P/N clocks will be frequency locked, but will have an arbitrary phase relationship with the data.

### Channel Lock Mode Synchronization

Incidental errors occurring in the received data can transform a normal data character into a K28.5 character. To prevent this occurrence from making the channel locking process unnecessarily vulnerable to bit errors, the S2004 implements a channel lock state machine for each channel with linkage between channels to move to the final de-skewed state.

The Channel Lock state diagram is shown in Figure 8. The S2004 powers up in the “No Sync” state. When in the “No Sync” state, each channel of the S2004 is actively searching the received data stream for the occurrence of a K28.5 and will align its demultiplexor to the character when detected, and will enter the “Acquiring Sync” state. K28.5 will be reported on each channel as 0-1-1 (err-eof-kflag). When four or more consecutive K28.5 characters are received on a given channel, the channel will enter the “Re-sync” state as shown in Figure 8. “Re-sync” state status will not be reported as 1-1-1 until the first valid data character has been received. If all four channels are in the “Re-sync” state and each has received a valid data character within the deskew time of 5 bytes, then the S2004 will channel lock by aligning the data output from each channel such that the first valid data character for each channel is output simultaneously. The device will move to the “In Sync” state and indicate channel lock status by each channel as a 0-1-0. Note that “Re-sync” is reported independently by each channel regardless of the state of the other channels. However, “In Sync” can only be reported when all four channels are in the “In Sync” state and detect a valid data character within the deskew window. The “In Sync” state is reported for each as 0-1-0.

Once the S2004 has entered the “In Sync” state, it will report status but will not alter the relative skew of the output FIFOs. The S2004 will exit the “In Sync” state and move to the “No Sync” state if one of the four CRUs reports a loss of lock, if the 8B/10B decoder observes four consecutive decoding errors, or if the decoder error rate >50% in a block of 16 codewords. The device can also be put in the “No Sync” state by setting TCLKD=Low, asserting RESET, or by momentarily de-asserting CH_LOCK signal.

TCLKD is used to reset the Channel Lock state machine and provides minimum disruption of the data path.

When not in Channel Lock Mode, the linkage between the four state machines is broken and each channel operates independently.

Loss of Channel Lock will be reported as indicated in Figure 9 and Table 7 by a 1-0-1 on the ERR, EOF, and KFLAG signals, respectively. This is during the “No Sync” state. The status lines will reflect the status of the individual channels and the device will respond to appropriate channel locking sequences and deskew as necessary. Persistence of 1-0-1 status on any channel is indicative of CRU lock failure, most likely resulting from loss of receiver input signal. The device will then respond to the channel locking sequence.

When operating in the Channel Lock Mode, the TCLKB input must be tied low.

***Figure 8. Channel Lock State Machine***

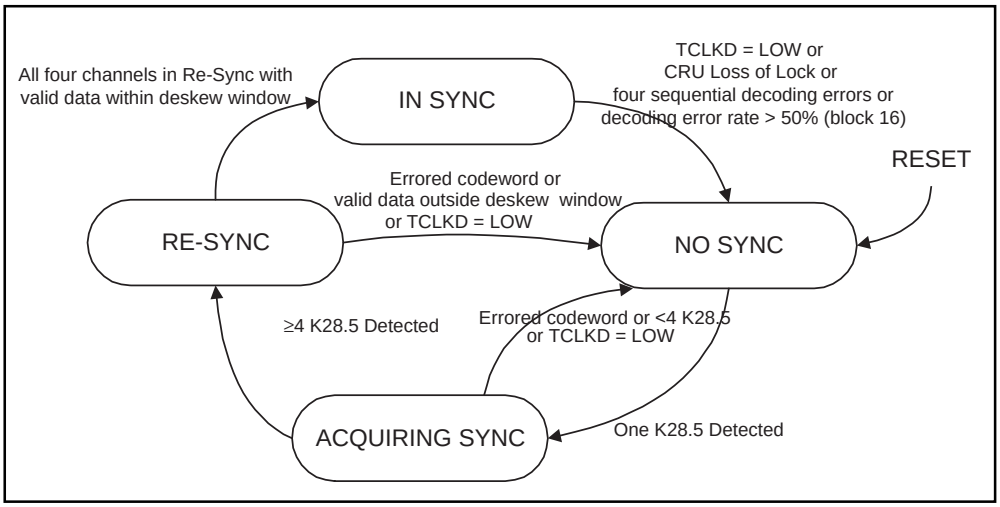
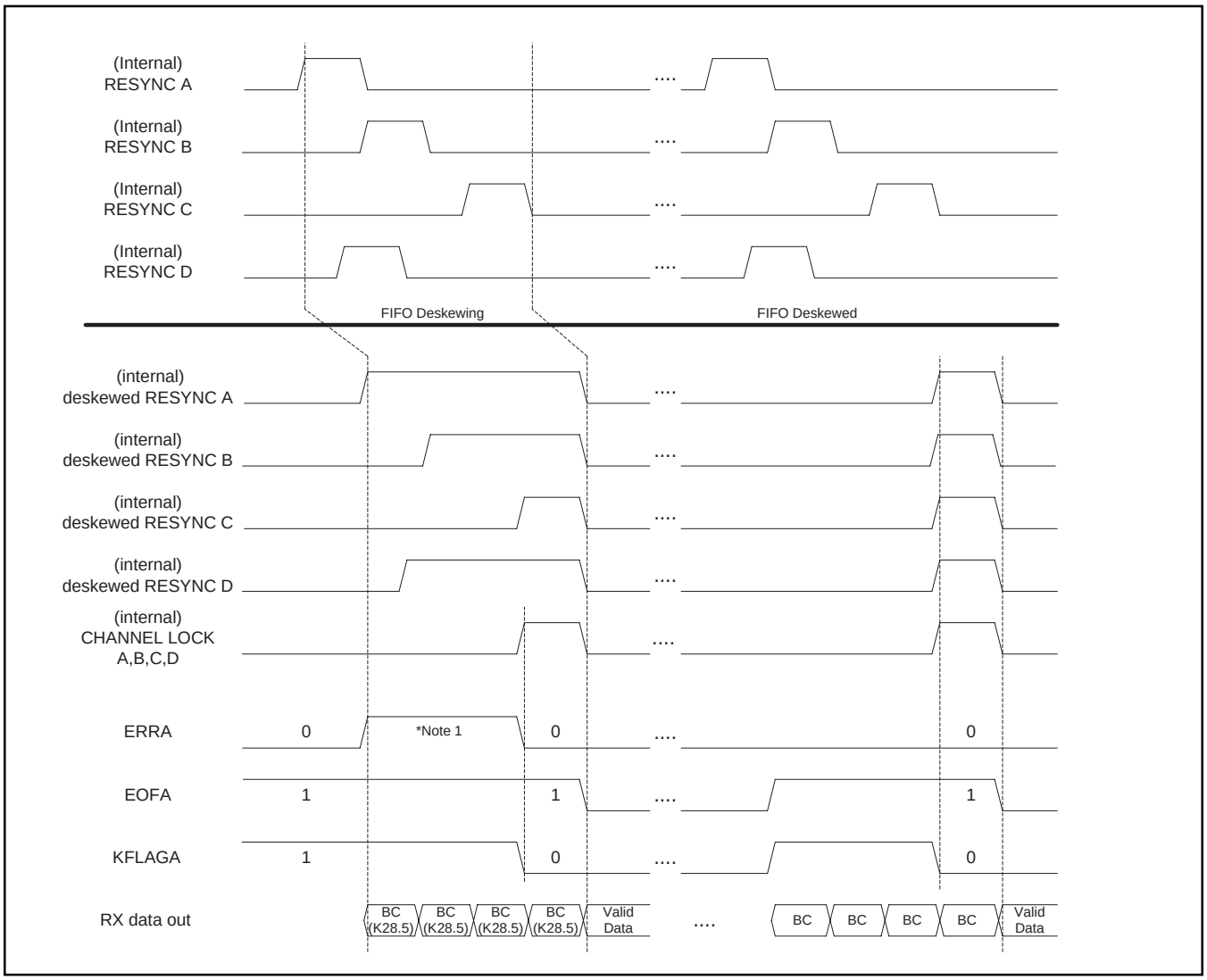



***Figure 9. Channel Lock Synchronization Timing***




1. The first three K28.5's will be reported as "K28.5" (011), subsequent K28.5 will be reported as "Resync" or "channel lock detected." See Table 7.

***Table 7. Error and Status Reporting***

| ERR | EOF | KFLAG | Description | Rank |
|---|---|---|---|---|
| 0 | 0 | 0 | Normal Character. Indicates that a valid data character has been detected. | 7 |
| 0 | 0 | 1 | K Character (not K28.5). Indicates that a K Character other than K28.5 has been detected. | 7 |
| 0 | 1 | 0 | Channel Lock Detected. Asserts for one parallel word on the ERRA, EOFA, and KFLAGA signals that all four channels have identified the re-sync sequence within the byte de-skew window. | 2 |
| 0 | 1 | 1 | K28.5+ or K28.5-. Indicates that a K28.5 character of arbitrary parity has been detected. | 5 |
| 1 | 0 | 0 | Codeword Violation. Indicates that a word not corresponding to any valid Dx.x or Kx.x mapping has been received. | 4 |
| 1 | 0 | 1 | Loss of Sync. Asserts for one parallel word to indicate that a condition has occured which results in loss of channel lock. When operating in the independent mode, indicates loss of CRU bit lock. | 1 |
| 1 | 1 | 0 | Parity Error. Indicates that a running disparity error has been observed. | 6 |
| 1 | 1 | 1 | Re-Sync (K28.5 x 4 + Dx.x). Asserts for one parallel word indicating that four consecutive K28.5 characters followed by a valid Dx.x character has been received. Each channel reports this condition independently and all four channels must identify the re-sync within the allowed byte de-skew time before channel lock can be achieved and be indicated with CHANNEL LOCK DETECTED (see above). | 3 |

## CHANNEL LOCKING/RE-LOCKING PROCEDURE

The Channel locking/relocking procedures are summarized below. Following these procedures will insure proper CHANNEL LOCK operation of the device. When powered up, the S2004 will lock to the received data within approximately 2500 bit times. The CRU must report lock for approximately 32,000 REFCLK periods (320 μs) before channel locking is enabled.

1. Insure that the S2004 is in the "No Sync" state. This can be accomplished by resetting the device by toggling TCLKD low, or by de-asserting the channel lock for several clock periods and then re-asserting.
2. Transmit the appropriate synchronization sequence. Four K28.5 characters or the 16 word SYNC sequence can be used to de-skew the DOUT FIFOs. The 16 word SYNC character can be generated by asserting SYNC=1 and DN=1.
3. Wait for "channel lock detected" as defined by Table 7.

The S2004 will enter the "No Sync" state if: any CRU loses lock, if the CH_LOCK signal is de-asserted, if four or more consecutive decoder errors are observed, or if the decoder error rate exceeds 50% in a block of 16 bytes, or if TCLKD is low. If desired, the CRU lock status of each channel can be checked by de-asserting CH_LOCK and confirming that "Loss of Sync" status (Table 7) is not reported by any channel. To reacquire Sync after moving to the "No Sync" state, repeat steps 2 and 3 above.

### 8B/10B Decoding

After serial to parallel conversion, the S2004 provides 8B/10B decoding of the data. The received 10-bit code word is decoded to recover the original 8-bit data. The decoder also checks for errors and flags, either invalid code word errors or running disparity errors by assertion of the ERRx signal. Error type is determined by examining the EOF output in accordance with Table 7. When more than one reportable condition occurs simultaneously, reporting is in accordance with the rank assigned by Table 7.

### Data Output

Data is output on the DOUT[0:7] outputs. K-characters are flagged using the KFLAG signal. The EOF (with KFLAG) is used to indicate the reception of a valid K28.5 character. Invalid codewords and decoding errors are indicated on the ERR output. KFLAG, EOF, and ERR are buffered with the data in the FIFO to insure that all outputs are synchronized at the S2004 outputs. Errors are reported independently for each channel in both CHANNEL-LOCK mode and NORMAL mode operation.

The S2004 TTL outputs are optimized to drive 65Ω line impedances. Internal source matching provides good performance on unterminated lines of reasonable length.

### Parallel Output Clock Rate

Two output clock modes are supported, as shown in Table 8. When CMODE is High, a complementary TTL clock at the data rate is provided on the RCxP/N outputs. Data should be clocked on the rising edge of RCxP. When CMODE is Low, a complementary TTL clock at 1/2 the data rate is provided. Data should be latched on the rising edge of RCxP and the rising edge of RCxN.

In Fibre Channel and Gigabit Ethernet applications, multiple consecutive K28.5 characters cannot be generated. However, for serial backplane applications this can occur. The S2004 must be able to operate properly when multiple K28.5 characters are received. After the first K28.5 is detected and aligned, the RCxP/N clock will operate without glitches or loss of cycles.

### Receiver Output Clocking

The S2004 parallel output clock source is determined by the TMODE selection. When REFCLK clocking is selected (TMODE = Low), the parallel output clocks (RCxP/N) are sourced from the TCLKA input. When TCLK clocking is selected (External Clocking Mode), the parallel output clocks are derived from the recovered clock from each channel. Table 8A describes the receiver output clocking options available.

When TCLKA is the output clock source, REFCLK and TCLKA must equal the parallel word rate (CLKSEL = Low). Additionally, the recovered clocks and the clock input on TCLKA must be frequency locked in order to avoid overflow/underflow of the internal FIFOs. The propagation delay between TCLKA and DOUTx, listed in Table 21, shows that the phase delay between TCLKA and the RCxP/N outputs may vary more than a bit time based on process variation.

The recommended clocking configuration for external clocking mode (REFCLK input clocking) is shown in Figure 10. TCLKA is sourced from TCLKO, which is frequency locked to the Reference clock input.

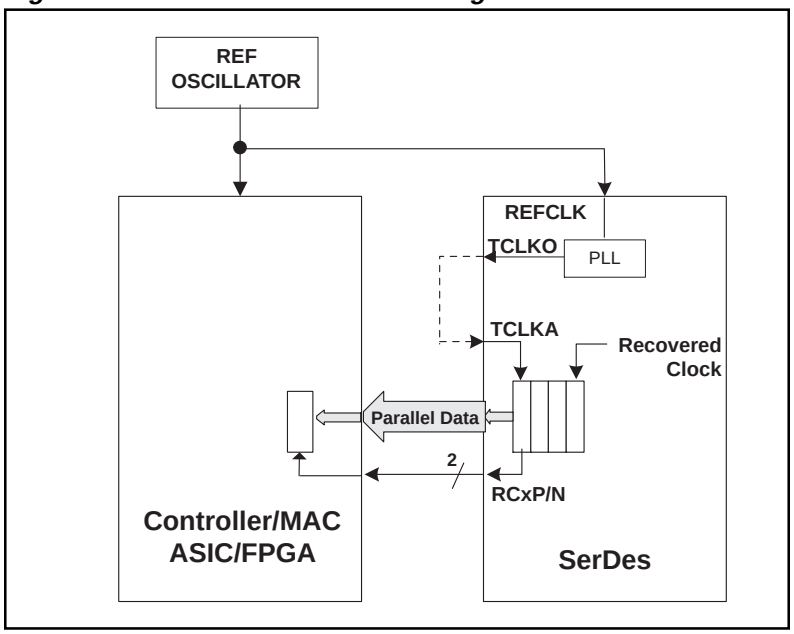
***Table 8. Output Clock Mode (TMODE = 1)***

| Mode | CMODE | RCx P/N Freq |
|---|---|---|
| Half Clock Mode | 0 | VCO/20 |
| Full Clock Mode | 1 | VCO/10 |

***Table 8A. S2004 Data Clocking***

| CH_LOCK | TMODE | Input Clock Source | Output Clock Source |
|---|---|---|---|
| 0 | 0 | REFCLK | TCLKA |
| 0 | 1 | TCLKx | RCx |
| 1 | 0 | REFCLK | TCLKA |
| 1 | 1 | TCLKA | RCA |

***Figure 10. External Receiver Clocking***



## OTHER OPERATING MODES

### Operating Frequency Range

The S2004 is designed to operate at serial baud rates of .98 GHz to 1.3 GHz (800 Mbps to 1040 Mbps user data rate). The part is specified at Fibre Channel (1062 MHz) and Gigabit Ethernet (1.25 GHz) serial baud rates, but will operate satisfactorily at any rate in this range.

### Loopback Mode

When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver, as shown in Figure 11. This provides the ability to perform system diagnostics and off-line testing of the interface to verify the integrity of the serial channel. Loopback mode is enabled independently for each channel using its respective loopback-enable input, LPEN.

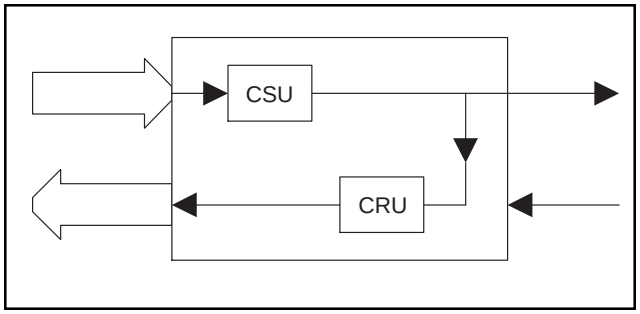
## TEST MODES

The S2004 has a testability input to aid in functional testing of the device. The test mode is entered when CH_LOCK is HIGH and TCLKB is HIGH. Thus users must take care to insure that TCLKB is held LOW when operating in the channel locked mode. The following conditions are asserted when in test mode:

- REFCLK replaces the VCO CLK (it also still goes to the transmit clock mux).
- TCLKA clocks all 4 transmit channels
- TCLKC is muxed in as the lock detect REFCLK for test purposes.
- TCLKD High becomes the channel lock signal to the whole of the chip except the transmit clock.

The RESET pin is used to initialize the Transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization). Note that Reset does not disable the TCLKO output unless the TCLKB input is HIGH.

***Figure 11. S2004 Diagnostic Loopback Operation***




Note: Serial output data remains active during loopback operation to enable other system tests to be performed.

## JTAG TESTING

The JTAG implementation for the S2004 is compliant with the IEEE1149.1 requirements. JTAG is used to test the connectivity of the pins on the chip. The TAP, (Test Access Port), provides access to the test logic of the chip. When TRST is asserted the TAP is initialized. TAP is a state machine that is controlled by TMS. The test instruction and data are loaded through TDI on the rising edge of TCK. When TMS is high the test instruction is loaded into the instruction register. When TMS is low the test data is loaded into the data register. TDO changes on the falling edge of TCK. All input pins, including clocks, that have boundary scan are observe only. They can be sampled in either normal operational or test mode. All output pins that have boundary scan, are observe and control. They can be sampled as they are driven out of the chip in normal operational mode, and they can be driven out of the chip in test mode using the Extest instruction. Since JTAG testing operates only on digital signals there are some pins with analog signals that JTAG does not cover. The JTAG implementation has the three required instruction, Bypass, Extest, and Sample/Preload.

| Instruction | Code |
|---|---|
| BYPASS | 11 |
| EXTEST | 00 |
| SAMPLE/PRELOAD | 01 |
| ID CODE | 10 |

### JTAG Instruction Description:

The BYPASS register contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and TDO pins of a component when no test operation of that component is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

The SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instructions.

The following table provides a list of the pins that are JTAG tested. Each port has a boundary scan register (BSR), unless otherwise noted. The following features are described: the JTAG mode of each register (input, output2, or internal (refers to an internal package pin)), the direction of the port if it has a boundary scan register (in or out), and the position of this register on the scan chain.

***Table 9. JTAG Pin Assignments,***

| S2004 Pin Name | Core_Scan Port Name | JTAG Mode | Routing In | Routing Out |
|---|---|---|---|---|
| SYNC | sync | Input | 0 | - |
| CMODE | cmode | Input | 1 | - |
| CH_LOCK | chan_lock | Input | 2 | - |
| LPEND | lpend | Input | 3 | - |
| LPENC | lpenc | Input | 4 | - |
| LPENB | lpenb | Input | 5 | - |
| LPENA | lpena | Input | 6 | - |
| CLKSEL | clksel | Input | 7 | - |
| TMODE | tmode | Input | 8 | - |
| | | Internal | 9 | - |
| RESET | reset | Input | 10 | - |
| REFCLK | refclk | Input | 11 | - |
| TCLKO | transmit_clk_ buf_out | Output2 | - | 12 |
| DND | dnd | Input | 13 | - |
| KGEND | kgend | Input | 14 | - |
| DIND7 | tdatain_d (7) | Input | 15 | - |
| DIND6 | tdatain_d (6) | Input | 16 | - |
| DIND5 | tdatain_d (5) | Input | 17 | - |
| DIND4 | tdatain_d (4) | Input | 18 | - |
| DIND3 | tdatain_d (3) | Input | 19 | - |
| DIND2 | tdatain_d (2) | Input | 20 | - |
| DIND1 | tdatain_d (1) | Input | 21 | - |
| DIND0 | tdatain_d (0) | Input | 22 | - |
| TCLKD | tclkd | Input | 23 | - |
| DNC | dnc | Input | 24 | - |
| KGENC | kgenc | Input | 25 | - |
| DINC7 | tdatain_c (7) | Input | 26 | - |
| DINC6 | tdatain_c (6) | Input | 27 | - |
| DINC5 | tdatain_c (5) | Input | 28 | - |
| DINC4 | tdatain_c (4) | Input | 29 | - |
| DINC3 | tdatain_c (3) | Input | 30 | - |
| DINC2 | tdatain_c (2) | Input | 31 | - |
| DINC1 | tdatain_c (1) | Input | 32 | - |
| DINC0 | tdatain_c (0) | Input | 33 | - |
| TCLKC | tclkc | Input | 34 | - |
| KGENB | kgenb | Input | 35 | - |
| DNB | dnb | Input | 36 | - |
| DINB7 | tdatain_b (7) | Input | 37 | - |
| DINB6 | tdatain_b (6) | Input | 38 | - |
| DINB5 | tdatain_b (5) | Input | 39 | - |
| DINB4 | tdatain_b (4) | Input | 40 | - |
| DINB3 | tdatain_b (3) | Input | 41 | - |
| DINB2 | tdatain_b (2) | Input | 42 | - |
| DINB1 | tdatain_b (1) | Input | 43 | - |
| DINB0 | tdatain_b (0) | Input | 44 | - |
| TCLKB | tclkb | Input | 45 | - |
| DNA | dna | Input | 46 | - |
| KGENA | kgena | Input | 47 | - |
| DINA7 | tdatain_a (7) | Input | 48 | - |
| DINA6 | tdatain_a (6) | Input | 49 | - |
| DINA5 | tdatain_a (5) | Input | 50 | - |
| DINA4 | tdatain_a (4) | Input | 51 | - |
| DINA3 | tdatain_a (3) | Input | 52 | - |
| DINA2 | tdatain_a (2) | Input | 53 | - |
| DINA1 | tdatain_a (1) | Input | 54 | - |
| DINA0 | tdatain_a (0) | Input | 55 | - |
| TCLKA | tclka | Input | 56 | - |
| RCDP | rcdp | Output2 | - | 57 |
| RCDN | rcdn | Output2 | - | 58 |
| DOUTD7 | rdataout_d (7) | Output2 | - | 59 |
| DOUTD6 | rdataout_d (6) | Output2 | - | 60 |
| DOUTD5 | rdataout_d (5) | Output2 | - | 61 |
| DOUTD4 | rdataout_d (4) | Output2 | - | 62 |
| DOUTD3 | rdataout_d (3) | Output2 | - | 63 |
| DOUTD2 | rdataout_d (2) | Output2 | - | 64 |
| DOUTD1 | rdataout_d (1) | Output2 | - | 65 |
| DOUTD0 | rdataout_d (0) | Output2 | - | 66 |
| EOFD | eofd_d | Output2 | - | 67 |
| KFLAGD | kflagd_d | Output2 | - | 68 |
| ERRD | errd_d | Output2 | - | 69 |
| RCCP | rccp | Output2 | - | 70 |
| RCCN | rccn | Output2 | - | 71 |
| DOUTC7 | rdataout_c (7) | Output2 | - | 72 |
| DOUTC6 | rdataout_c (6) | Output2 | - | 73 |
| DOUTC5 | rdataout_c (5) | Output2 | - | 74 |
| DOUTC4 | rdataout_c (4) | Output2 | - | 75 |
| DOUTC3 | rdataout_c (3) | Output2 | - | 76 |
| DOUTC2 | rdataout_c (2) | Output2 | - | 77 |
| DOUTC1 | rdataout_c (1) | Output2 | - | 78 |
| DOUTC0 | rdataout_c (0) | Output2 | - | 79 |

***Table 9. JTAG Pin Assignments (Continued)***

| S2004 Pin Name | Core_Scan Port Name | JTAG Mode | Routing In | Routing Out |
|---|---|---|---|---|
| ERRC | errd_c | Output2 | - | 80 |
| EOFC | eofd_c | Output2 | - | 81 |
| KFLAGC | kflag_c | Output2 | - | 82 |
| RCBP | rcbp | Output2 | - | 83 |
| RCBN | rcbn | Output2 | - | 84 |
| KFLAGB | kflagd_b | Output2 | - | 85 |
| DOUTB7 | rdataout_b (7) | Output2 | - | 86 |
| DOUTB6 | rdataout_b (6) | Output2 | - | 87 |
| DOUTB5 | rdataout_b (5) | Output2 | - | 88 |
| DOUTB4 | rdataout_b (4) | Output2 | - | 89 |
| DOUTB3 | rdataout_b (3) | Output2 | - | 90 |
| DOUTB2 | rdataout_b (2) | Output2 | - | 91 |
| DOUTB1 | rdataout_b (1) | Output2 | - | 92 |
| DOUTB0 | rdataout_b (0) | Output2 | - | 93 |
| EOFB | eofd_b | Output2 | - | 94 |
| ERRB | errd_b | Output2 | - | 95 |
| RCAP | rcap | Output2 | - | 96 |
| RCAN | rcan | Output2 | - | 97 |
| ERRA | errd_a | Output2 | - | 98 |
| DOUTA7 | rdataout_a (7) | Output2 | - | 99 |
| DOUTA6 | rdataout_a (6) | Output2 | - | 100 |
| DOUTA5 | rdataout_a (5) | Output2 | - | 101 |
| DOUTA4 | rdataout_a (4) | Output2 | - | 102 |
| DOUTA3 | rdataout_a (3) | Output2 | - | 103 |
| DOUTA2 | rdataout_a (2) | Output2 | - | 104 |
| DOUTA1 | rdataout_a (1) | Output2 | - | 105 |
| DOUTA0 | rdataout_a (0) | Output2 | - | 106 |
| EOFA | eofd_a | Output2 | - | 107 |
| KFLAGA | kflagd_a | Output2 | - | 108 |
| | | Internal | - | 109 |

| S2004 Pin Name | Core_Scan Port Name | JTAG Mode | Routing In | Routing Out |
|---|---|---|---|---|
| **JTAG Control Pins** (Ports that do not have a Boundary Scan Register) | | | | |
| TCK | jtag_tck | - | - | - |
| TDI | jtag_tdi | - | - | - |
| TDO | jtag_tdo | - | - | - |
| TMS | jtag_tms | - | - | - |
| TRS | jtag_trs | - | - | - |
| **Pins not JTAG Tested** | | | | |
| TXAP | - | - | - | - |
| TXAN | - | - | - | - |
| TXBP | - | - | - | - |
| TXBN | - | - | - | - |
| TXCP | - | - | - | - |
| TXCN | - | - | - | - |
| TXDP | - | - | - | - |
| TXDN | - | - | - | - |
| RATE | - | - | - | - |
| RXAP | - | - | - | - |
| RXAN | - | - | - | - |
| RXBP | - | - | - | - |
| RXBN | - | - | - | - |
| RXCP | - | - | - | - |
| RXCN | - | - | - | - |
| RXDP | - | - | - | - |
| RXDN | - | - | - | - |

***Table 10. Transmitter Input Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| DINA7<br>DINA6<br>DINA5<br>DINA4<br>DINA3<br>DINA2<br>DINA1<br>DINA0 | TTL | I | P12<br>R12<br>T13<br>T12<br>U13<br>P11<br>R11<br>T11 | Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TCLKA or REFCLK. (See Table 1.) |
| DNA | TTL | I | U15 | DATA_NOT. When Low, data present on DINA[0:7] is 8B/10B encoded and transmitted serially. When High, special character/sequences are generated as indicated in Table 2. |
| KGENA | TTL | I | U14 | K-Character Generation. KGENA High causes the data on DINA[0:7] to be encoded into a K-Character. (See Table 2.) |
| TCLKA | TTL | I | U12 | Transmit Data Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:7], KGENA, and DNA into the S2004. When TMODE is Low, TCLKA is ignored. |
| DINB7<br>DINB6<br>DINB5<br>DINB4<br>DINB3<br>DINB2<br>DINB1<br>DINB0 | TTL | I | R15<br>P14<br>T15<br>R14<br>U17<br>U16<br>P13<br>T14 | Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TCLKA, TCLKB or REFCLK. (See Table 1.) |
| DNB | TTL | I | R16 | DATA_NOT. When Low, data present on DINB[0:7] is 8B/10B encoded and transmitted serially. When High, special character/sequences are generated as indicated in Table 2. |
| KGENB | TTL | I | T16 | K-Character Generation. KGENB High causes the data on DINB[0:7] to be encoded into a K-Character. (See Table 2.) |
| TCLKB | TTL | I | R13 | Transmit Data Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:7], KGENB, and DNB into the S2004. When TMODE is Low, TCLKB is ignored. When CH_LOCK = HIGH, TCLKB must be tied Low. |
| DINC7<br>DINC6<br>DINC5<br>DINC4<br>DINC3<br>DINC2<br>DINC1<br>DINC0 | TTL | I | M15<br>N16<br>M14<br>R17<br>P16<br>N15<br>T17<br>N14 | Transmit Data for Channel C. Parallel data on this bus is clocked in on the rising edge of TCLKA, TCLKC, or REFCLK. (See Table 1.) |

***Table 10. Transmitter Signal Descriptions (Continued)***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| DNC | TTL | I | N17 | DATA_NOT. When Low, data present on DINC[0:7] is 8B/10B encoded and transmitted serially. When High, special character/sequences are generated as indicated in Table 2. |
| KGENC | TTL | I | P17 | K-Character Generation. KGENC High causes the data on DINC[0:7] to be encoded into a K-Character. (See Table 2.) |
| TCLKC | TTL | I | P15 | Transmit Data Clock C. When TMODE is High, this signal is used to clock Data on DINC[0:7], KGENC, and DNC into the S2004. When TMODE is Low, TCLKC is ignored. |
| DIND7<br>DIND6<br>DIND5<br>DIND4<br>DIND3<br>DIND2<br>DIND1<br>DIND0 | TTL | I | L17<br>K16<br>K15<br>K14<br>M17<br>L16<br>M16<br>L15 | Transmit Data for Channel D. Parallel data on this bus is clocked in on the rising edge of TCLKA, TCLKD or REFCLK. (See Table 1.) |
| DND | TTL | I | J16 | DATA_NOT, When Low, data present on DIND[0:7] is 8B/10B encoded and transmitted serially. When High, special character/sequences are generated as indicated in Table 2. |
| KGEND | TTL | I | K17 | K-Character Generation. KGEND High causes the data on DIND[0:7] to be encoded into a K-Character. (See Table 2.) |
| TCLKD | TTL | I | L14 | Transmit Data Clock D. When TMODE is High, this signal is used to clock Data on DIND[0:7], KGEND, and DND into the S2004. When TMODE is Low, TCLKD is ignored. In Channel Lock Mode, CH_LOCK = HIGH, TCLKD (Low) is used to reset the Channel Lock state machine. |
| SYNC | TTL | I | D4 | When High, (See Table 2) used to generate a special sequence of K28.5 charaters. See earlier text. |

***Table 11. Transmitter Output Signals***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| TXAP<br>TXAN | Diff.<br>LVPECL | O | A17<br>B17 | High speed serial outputs for Channel A. |
| TXBP<br>TXBN | Diff.<br>LVPECL | O | C17<br>D17 | High speed serial outputs for Channel B. |
| TXCP<br>TXCN | Diff.<br>LVPECL | O | E17<br>F16 | High speed serial outputs for Channel C. |
| TXDP<br>TXDN | Diff.<br>LVPECL | O | F17<br>G17 | High speed serial outputs for Channel D. |
| TCLKO | TTL | O | J14 | TTL Output Clock at the Parallel data rate. This clock is provided for use by up-stream circuitry. |

***Table 12. Mode Control Signals***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| CH_LOCK | TTL | I | E4 | Parallel Input Mode Control. Channel Lock High locks all four channels together. (See Table 1.) |
| TMODE | TTL | I | B13 | Transmit Mode Control. Controls the source of the clock used to input and output data to and from the S2004. When TMODE is Low, REFCLK is used to clock data on DINx[0:7], DNx, SYNC, and KGENx into the S2004. TCLKA is used to clock parallel data DOUTx[0:7], EOFx, ERRx, and KFLAG out of the device.<br>When TMODE is High:<br>In Channel Lock Mode, TCLKA clocks data into the S2004 for all four channels and the output clock is derived from the receiver A CRU.<br>For Independent Mode, each channel is clocked by its respective TCLKx. The output clocks are derived from the receivers' CRUs. |
| CLKSEL | TTL | I | C12 | REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency equals the parallel word rate. When CLKSEL = 1, the REFCLK frequency is 1/2 the parallel data rate. |
| REFCLK | TTL | I | H17 | Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data. Also used to clock parallel data into the device when in REFCLK mode. |
| RESET | TTL | I | C15 | When Low, the S2004 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2004 operates normally. |
| RATE | TTL | I | D12 | When Low, the S2004 operates with the serial output rate equal to the VCO frequency. When High, the S2004 operates with the VCO internally divided by 2 for all functions. |

Note: All TTL inputs except REFCLK have internal pull-up networks.

***Table 13. Receiver Output Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| DOUTA7<br>DOUTA6<br>DOUTA5<br>DOUTA4<br>DOUTA3<br>DOUTA2<br>DOUTA1<br>DOUTA0 | TTL | O | J1<br>J3<br>J2<br>H1<br>H2<br>H3<br>F1<br>G2 | Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCAP in full clock mode and valid on rising edge of both RCAP and RCAN in half clock mode. |
| EOFA | TTL | O | F2 | Channel A End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:7]. |
| KFLAGA | TTL | O | G3 | Channel A K-Character Flag. A High in KFLAGA indicates that a valid control character has been detected. Data present on the parallel interface DOUTA[0:7] should be used to indicate which character was received. |
| ERRA | TTL | O | G1 | Channel A Receive Error. A High on ERRA signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. |
| RCAP<br>RCAN | TTL | O | K2<br>K1 | Receive Data Clock. Parallel receive data, DOUTA[0:7], EOFA, KFLAGA, and ERRA are valid on the rising edge of RCAP when in full clock mode and valid on the rising edge of both RCAP and RCAN in half clock mode. |
| DOUTB7<br>DOUTB6<br>DOUTB5<br>DOUTB4<br>DOUTB3<br>DOUTB2<br>DOUTB1<br>DOUTB0 | TTL | O | R1<br>P1<br>M3<br>N2<br>M2<br>N1<br>L2<br>M1 | Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCBP in full clock mode and valid on rising edge of both RCBP and RCBN in half clock mode. |
| EOFB | TTL | O | L1 | Channel B End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:7]. |
| KFLAGB | TTL | O | P2 | Channel B K-Character Flag. A High in KFLAGB indicates that a valid control character has been detected. Data present on the parallel interface DOUTB[0:7] should be used to indicate which character was received. |
| ERRB | TTL | O | K3 | Channel B Receive Error. A High on ERRB signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. |
| RCBP<br>RCBN | TTL | O | U1<br>T1 | Receive Data Clock. Parallel receive data, DOUTB[0:7], EOFB, KFLAGB, and ERRB are valid on the rising edge of RCBP when in full clock mode and valid on the rising edge of both RCBP and RCBN in half clock mode. |

***Table 13. Receiver Output Pin Assignment and Descriptions (Continued)***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| DOUTC7<br>DOUTC6<br>DOUTC5<br>DOUTC4<br>DOUTC3<br>DOUTC2<br>DOUTC1<br>DOUTC0 | TTL | O | R7<br>R6<br>T5<br>U3<br>T4<br>R5<br>U2<br>T3 | Channel C Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCCP in full clock mode and valid on the rising edge of both RCCP and RCCN in half clock mode. |
| EOFC | TTL | O | R2 | Channel C End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTC[0:7]. |
| KFLAGC | TTL | O | P3 | Channel C K-Character Flag. A High in KFLAGC indicates that a valid control character has been detected. Data present on the parallel interface DOUTC[0:7] should be used to indicate which character was received. |
| ERRC | TTL | O | T2 | Channel C Receive Error. A High on ERRC signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. |
| RCCP<br>RCCN | TTL | O | U5<br>U4 | Receive Data Clock. Parallel receive data, DOUTC[0:7], EOFC, KFLAGC, and ERRC are valid on the rising edge of RCCP when in full clock mode and valid on the rising edge of both RCCP and RCCN in half clock mode. |
| DOUTD7<br>DOUTD6<br>DOUTD5<br>DOUTD4<br>DOUTD3<br>DOUTD2<br>DOUTD1<br>DOUTD0 | TTL | O | U11<br>R10<br>U9<br>R9<br>T9<br>U8<br>U7<br>T8 | Channel D Receiver Data outputs. Parallel data on this bus is valid on the rising edge of RCDP in full clock mode and valid on rising edge of both RCDP and RCDN in half clock mode. |
| EOFD | TTL | O | U6 | Channel D End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTD[0:7]. |
| KFLAGD | TTL | O | T7 | Channel D K-Character Flag. A High in KFLAGD indicates that a valid control character has been detected. Data present on the parallel interface DOUTD[0:7] should be used to indicate which character was received. |
| ERRD | TTL | O | T6 | Channel D Receive Error. A High on ERRD signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data. |
| RCDP<br>RCDN | TTL | O | T10<br>U10 | Receive Data Clock. Parallel receive data, DOUTD[0:7], EOFD, KFLAGD, and ERRD are valid on the rising edge of RCDP when in full clock mode and valid on the rising edge of both RCDP and RCDN in half clock mode. |

***Table 14. Receiver Input Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| RXAP<br>RXAN | Diff.<br>LVPECL | I | A2<br>A3 | Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD -1.3V for AC coupled applications. |
| RXBP<br>RXBN | Diff.<br>LVPECL | I | A5<br>B5 | Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD -1.3V for AC coupled applications. |
| RXCP<br>RXCN | Diff.<br>LVPECL | I | A8<br>A9 | Differential LVPECL compatible inputs for channel C. RXCP is the positive input, RXCN is the negative. Internally biased to VDD -1.3V for AC coupled applications. |
| RXDP<br>RXDN | Diff.<br>LVPECL | I | B11<br>B12 | Differential LVPECL compatible inputs for channel D. RXDP is the positive input, RXDN is the negative. Internally biased to VDD -1.3V for AC coupled applications. |

***Table 15. Receiver Control Signals***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| LPENA<br>LPENB<br>LPENC<br>LPEND | TTL | I | D14<br>G14<br>G15<br>H14 | Loopback Enable. When Low, input source is the high speed serial input for each channel. When High, the serial output for each channel is looped back to its input. |
| CMODE | TTL | I | C2 | Clock Mode Control. When Low, the parallel output clocks (RCxP/N) rate is equal to 1/2 the data rate. When High, the parallel output clocks (RCxP/N) rate is equal to the data rate. |

Note: All TTL inputs except REFCLK have internal pull-up networks.

***Table 16. Power and Ground Signals***

| Pin Name | Qty. | Pin # | Description |
|---|---|---|---|
| VDDA | 5 | A1, A6, A13, A16 C8 | Analog Power (VDD) low noise. |
| VSSA | 5 | B7, B8, B15, C4, D11 | Analog Ground (VSS). |
| VDD | 6 | A12, A15, B4, B6, C6, D9 | Power for High Speed Circuitry (VDD). |
| VSS<br>VSSSUB | 10 | A4, A7, A11, A14, B10, B14, C13, D5, D6, D8 | Ground for High Speed Circuitry (VSS). |

***Table 16. Power and Ground Signals (Continued)***

| Pin Name | Qty. | Pin # | Description |
|---|---|---|---|
| PECLPWR | 4 | D15, E15, E16, G16 | PECL Power (VDD) |
| PECLGND | 2 | C16 H16 | PECL Ground (VSS) |
| DIGPWR | 6 | B1, B2, E3, J17, L4, P9 | Core Circuitry Power (VDD) |
| DIGGND | 8 | C1, C3, D2, F4, J15, N4, P10, R3 | Core Circuitry Ground (VSS) |
| TTLPWR | 8 | E1, G4, H4, K4, N3, P5, P7, P8 | Power for TTL I/O (VDD) |
| TTLGND | 10 | D1, E2, F3, J4, L3, M4 P4, P6, R4, R8 | Ground for TTL I/O (VSS) |
| PWR | 1 | B16 | Power |
| GND | 1 | D3 | Ground |
| CAP1 CAP2 | 2 | D13 C14 | Pins for external loop filter capacitor |
| NC | 10 | B9, C5, C7, C9, C11, D7, D16, E14, F14, F15 | Not Connected. Used as Test Pins. Do Not Connect. |

***Table 17. JTAG Test Signals***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| TMS | TTL | I | A10 | Test Mode Select. Enables JTAG testing of device. |
| TCK | TTL | I | C10 | Test Clock. JTAG test clock. |
| TDI | TTL | I | D10 | Test Data In. JTAG data input. |
| TDO | TTL | O TRISTATE | H15 | Test Data Out. JTAG data output. Can be high impedance under JTAG controller command. |
| TRS | TTL | I | B3 | Test Reset. Resets JTAG test state machine. |

***Figure 12. S2004 Pinout (Bottom View)***

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VDDA | DIGPWR | DIGGND | TTLGND | TTLPWR | DOUTA1 | ERRA | DOUTA4 | DOUTA7 | RCAN | EOFB | DOUTB0 | DOUTB2 | DOUTB6 | DOUTB7 | RCBN | RCBP |
| 2 | RXAP | DIGPWR | CMODE | DIGGND | TTLGND | EOFA | DOUTA0 | DOUTA3 | DOUTA5 | RCAP | DOUTB1 | DOUTB3 | DOUTB4 | KFLAGB | EOFC | ERRC | DOUTC1 |
| 3 | RXAN | TRS | DIGGND | GND | DIGPWR | TTLGND | KFLAGA | DOUTA2 | DOUTA6 | ERRB | TTLGND | DOUTB5 | TTLPWR | KFLAGC | DIGGND | DOUTC0 | DOUTC4 |
| 4 | VSS | VDD | VSSA | SYNC | CH_LOCK | DIGGND | TTLPWR | TTLPWR | TTLGND | TTLPWR | DIGPWR | TTLGND | DIGGND | TTLGND | TTLGND | DOUTC3 | RCCN |
| 5 | RXBP | RXBN | NC | VSSSUB | | | | | | | | | | TTLPWR | DOUTC2 | DOUTC5 | RCCP |
| 6 | VDDA | VDD | VDD | VSS | | | | | | | | | | TTLGND | DOUTC6 | ERRD | EOFD |
| 7 | VSSSUB | VSSA | NC | NC | | | | | | | | | | TTLPWR | DOUTC7 | KFLAGD | DOUTD1 |
| 8 | RXCP | VSSA | VDDA | VSSSUB | | | | | | | | | | TTLPWR | TTLGND | DOUTD0 | DOUTD2 |
| 9 | RXCN | NC | NC | VDD | | | | | | | | | | DIGPWR | DOUTD4 | DOUTD3 | DOUTD5 |
| 10 | TMS | VSS | TCK | TDI | | | | | | | | | | DIGGND | DOUTD6 | RCDP | RCDN |
| 11 | VSS | RXDP | NC | VSSA | | | | | | | | | | DINA2 | DINA1 | DINA0 | DOUTD7 |
| 12 | VDD | RXDN | CLKSEL | RATE | | | | | | | | | | DINA7 | DINA6 | DINA4 | TCLKA |
| 13 | VDDA | TMODE | VSSSUB | CAP1 | | | | | | | | | | DINB1 | TCLKB | DINA5 | DINA3 |
| 14 | VSSSUB | VSS | CAP2 | LPENA | NC | NC | LPENB | LPEND | TCLKO | DIND4 | TCLKD | DINC5 | DINC0 | DINB6 | DINB4 | DINB0 | KGENA |
| 15 | VDD | VSSA | RESET | PECL PWR | PECL PWR | NC | LPENC | TDO | DIGGND | DIND5 | DIND0 | DINC7 | DINC2 | TCLKC | DINB7 | DINB5 | DNA |
| 16 | VDDA | PWR | PECLGND | NC | PECL PWR | TXCN | PECL PWR | PECLGND | DND | DIND6 | DIND2 | DIND1 | DINC6 | DINC3 | DNB | KGENB | DINB2 |
| 17 | TXAP | TXAN | TXBP | TXBN | TXCP | TXDP | TXDN | REFCLK | DIGPWR | KGEND | DIND7 | DIND3 | DNC | KGENC | DINC4 | DINC1 | DINB3 |

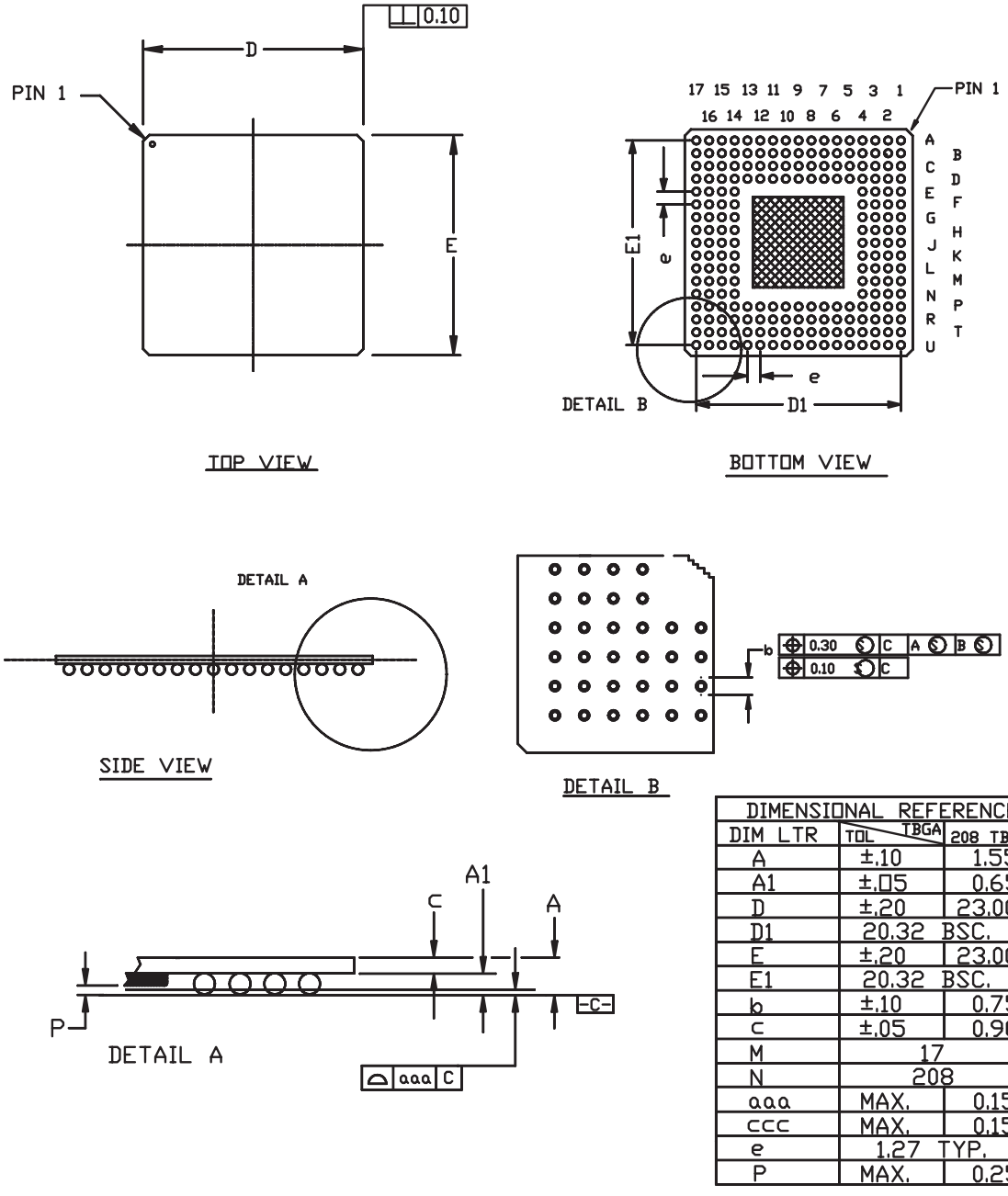
Note: NC used as Test Pins. Do Not Connect.

***Figure 13. S2004 Pinout (Top View)***

| U | T | R | P | N | M | L | K | J | H | G | F | E | D | C | B | A | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCBP | RCBN | DOUTB7 | DOUTB6 | DOUTB2 | DOUTB0 | EOFB | RCAN | DOUTA7 | DOUTA4 | ERRA | DOUTA1 | TTLPWR | TTLGND | DIGGND | DIGPWR | VDDA | 1 |
| DOUTC1 | ERRC | EOFC | KFLAGB | DOUTB4 | DOUTB3 | DOUTB1 | RCAP | DOUTA5 | DOUTA3 | DOUTA0 | EOFA | TTLGND | DIGGND | CMODE | DIGPWR | RXAP | 2 |
| DOUTC4 | DOUTC0 | DIGGND | KFLAGC | TTLPWR | DOUTB5 | TTLGND | ERRB | DOUTA6 | DOUTA2 | KFLAGA | TTLGND | DIGPWR | GND | DIGGND | TRS | RXAN | 3 |
| RCCN | DOUTC3 | TTLGND | TTLGND | DIGGND | TTLGND | DIGPWR | TTLPWR | TTLGND | TTLPWR | TTLPWR | DIGGND | CH_LOCK | SYNC | VSSA | VDD | VSS | 4 |
| RCCP | DOUTC5 | DOUTC2 | TTLPWR | | | | | | | | | | VSSSUB | NC | RXBN | RXBP | 5 |
| EOFD | ERRD | DOUTC6 | TTLGND | | | | | | | | | | VSS | VDD | VDD | VDDA | 6 |
| DOUTD1 | KFLAGD | DOUTC7 | TTLPWR | | | | | | | | | | NC | NC | VSSA | VSSSUB | 7 |
| DOUTD2 | DOUTD0 | TTLGND | TTLPWR | | | | | | | | | | VSSSUB | VDDA | VSSA | RXCP | 8 |
| DOUTD5 | DOUTD3 | DOUTD4 | DIGPWR | | | | | | | | | | VDD | NC | NC | RXCN | 9 |
| RCDN | RCDP | DOUTD6 | DIGGND | | | | | | | | | | TDI | TCK | VSS | TMS | 10 |
| DOUTD7 | DINA0 | DINA1 | DINA2 | | | | | | | | | | VSSA | NC | RXDP | VSS | 11 |
| TCLKA | DINA4 | DINA6 | DINA7 | | | | | | | | | | RATE | CLKSEL | RXDN | VDD | 12 |
| DINA3 | DINA5 | TCLKB | DINB1 | | | | | | | | | | CAP1 | VSSSUB | TMODE | VDDA | 13 |
| KGENA | DINB0 | DINB4 | DINB6 | DINC0 | DINC5 | TCLKD | DIND4 | TCLKO | LPEND | LPENB | NC | NC | LPENA | CAP2 | VSS | VSSSUB | 14 |
| DNA | DINB5 | DINB7 | TCLKC | DINC2 | DINC7 | DIND0 | DIND5 | DIGGND | TDO | LPENC | NC | PECL PWR | PECL PWR | RESET | VSSA | VDD | 15 |
| DINB2 | KGENB | DNB | DINC3 | DINC6 | DIND1 | DIND2 | DIND6 | DND | PECLGND | PECL PWR | TXCN | PECL PWR | NC | PECLGND | PWR | VDDA | 16 |
| DINB3 | DINC1 | DINC4 | KGENC | DNC | DIND3 | DIND7 | KGEND | DIGPWR | REFCLK | TXDN | TXDP | TXCP | TXBN | TXBP | TXAN | TXAP | 17 |

Note: NC used as Test Pins. Do Not Connect.

***Figure 14. Compact 23mm x 23mm 208 TBGA Package***




| DIMENSIONAL REFERENCES | | |
|---|---|---|
| DIM LTR | TOL / TBGA | 208 TBGA |
| A | ±.10 | 1.55 |
| A1 | ±.05 | 0.65 |
| D | ±.20 | 23.00 |
| D1 | 20.32 BSC. | |
| E | ±.20 | 23.00 |
| E1 | 20.32 BSC. | |
| b | ±.10 | 0.75 |
| c | ±.05 | 0.90 |
| M | 17 | |
| N | 208 | |
| aaa | MAX. | 0.15 |
| ccc | MAX. | 0.15 |
| e | 1.27 TYP. | |
| P | MAX. | 0.25 |

***Thermal Management***

| Device | Θja (Still Air) | Θjc |
|---|---|---|
| S2004 | 17.7° C/W | 3.5° C/W |

***Figure 15. Transmitter Timing (Normal or Channel Lock Mode, TMODE = 0)***

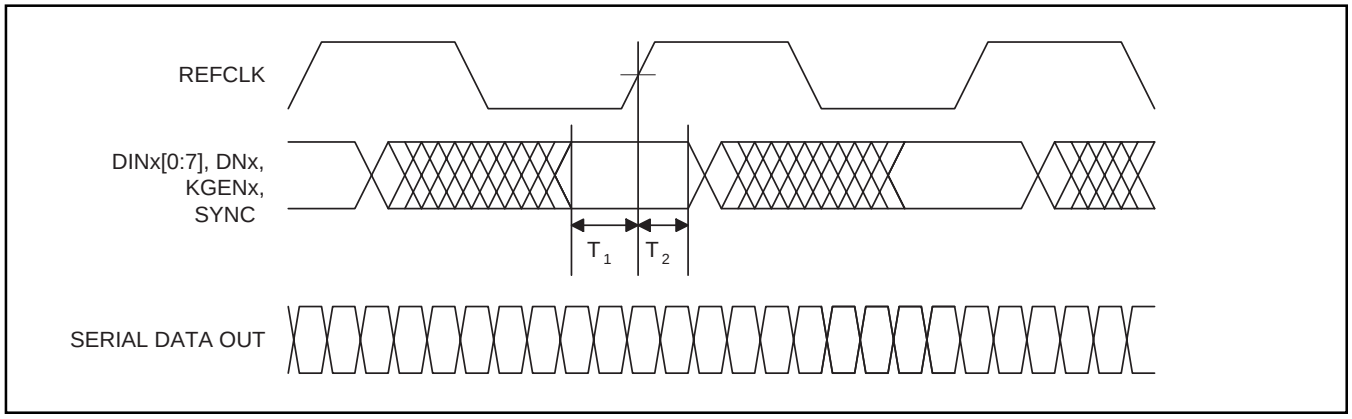



***Table 18. S2004 Transmitter Timing (Normal or Channel Lock Mode, TMODE = 0)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_1$ | Data Setup w.r.t. ↑REFCLK | 0.5 | - | ns | See Note 1. |
| $T_2$ | Data Hold w.r.t. ↑REFCLK | 1.5 | - | ns | |

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

***Figure 16. Transmitter Timing (Normal or Channel Lock Mode, TMODE = 1)***

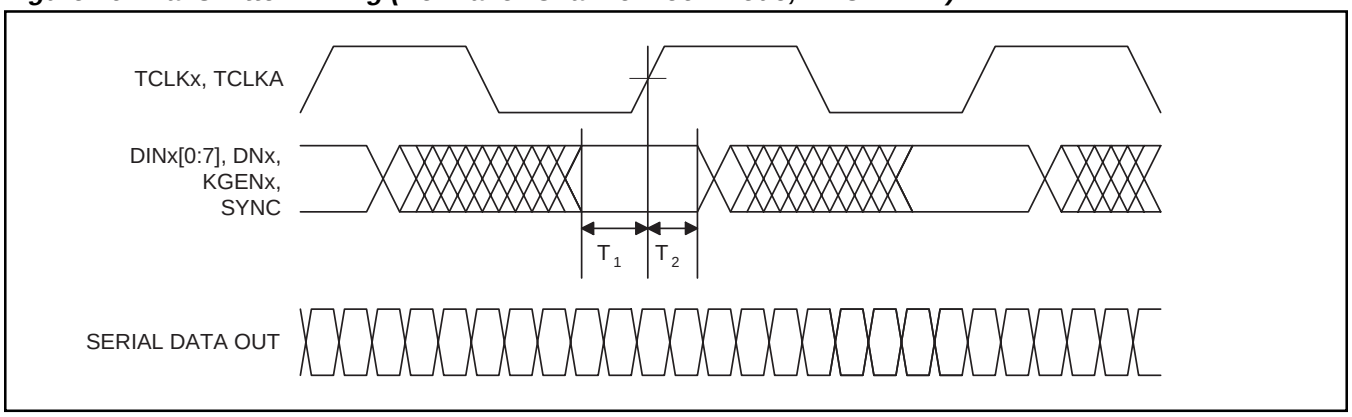



***Table 19. S2004 Transmitter Timing (Normal or Channel Lock Mode, TMODE = 1)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_1$ | Data Setup w.r.t. ↑TCLK | 1.0 | - | ns | See Note 1. |
| $T_2$ | Data Hold w.r.t. ↑TCLK | 0.5 | - | ns | |
| | Phase drift between TCLKx and REFCLK | -3 | +3 | ns | |

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

***Table 20. S2004 Receiver Timing (Full and Half Clock Mode)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_3$ | Data Setup w.r.t. ↑ RCxP/N | 2.5<br>3.0<br>X<br>X | | ns<br>ns<br>ns<br>ns | 1.25 Gbps TMODE = 1<br>1.062 Gbps TMODE = 1<br>1.25 Gbps TMODE = 0<br>1.062 Gbps TMODE = 0 |
| $T_4$ | Data Hold w.r.t. ↑ RCxP/N | 2.5<br>X | | ns<br>ns | TMODE = 1<br>TMODE = 0 |
| $T_5$ | Data Setup w.r.t. ↑ RCxP/N | 2.5<br>3.0 | | ns | at 1.25 Gbps TMODE = 1<br>at 1.062 Gbps[1,2] TMODE = 1 |
| $T_6$ | Data Hold w.r.t. ↑ RCxP/N | 2.5 | | ns | TMODE = 1 |
| $T_7$ | Time from RCxP rise to RCxN rise | 7.5<br>8.9 | 8.5<br>9.9 | ns<br>ns | at 1.25 Gbps<br>at 1.062 Gbps[1,2] |
| $T_{RP}$, $T_{FP}$ | RCxP Rise and Fall Times | | 2.4 | ns | See note 2. See Figure 22. |
| $T_{RN}$, $T_{FN}$ | RCxN Rise and Fall Times | | 2.4 | ns | See note 2. See Figure 22. |
| $T_{DR}$, $T_{DF}$ | DOUTx Rise and Fall Times | | 2.4 | ns | See note 2. See Figure 21. |
| Duty Cycle | RCxP/N Duty Cycle | 40 | 60 | % | See note 1. |

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).
2. TTL/CMOS AC timing measurements are assumed to have an output load of 10pf.

***Table 21. Receiver Timing (External Clock Mode)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_8$ | TCLKA to DOUTx Propagation Delay | 3.0 | 8.0 | ns | 10pf load capacitance at the end of a 3 inch 50 Ω transmission line. |

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

***Figure 17. Receiver Timing (Full Clock Mode, CMODE = 1)***

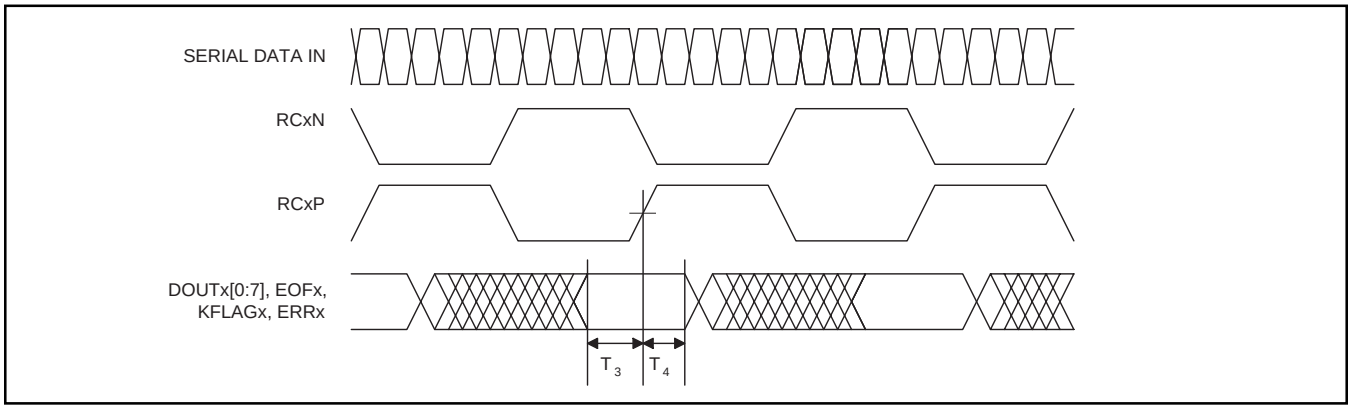



***Figure 18. Receiver Timing (Half Clock Mode, CMODE = 0, TMODE = 1)***

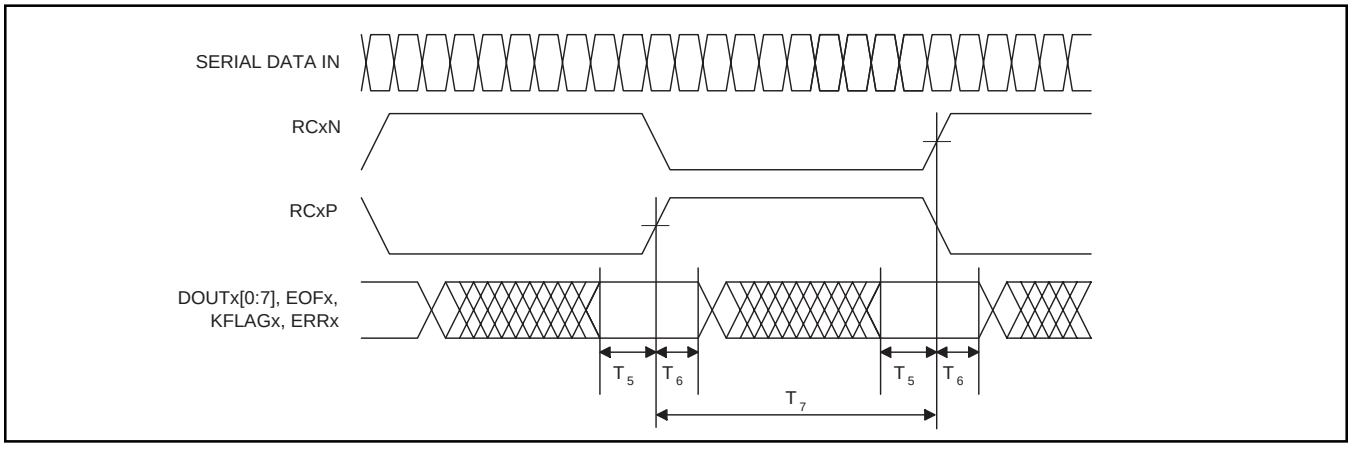



***Figure 19. Receiver Timing (External Clock Mode)***
***(TCLKA to DATA Propagation Delay, TMODE = 0)***

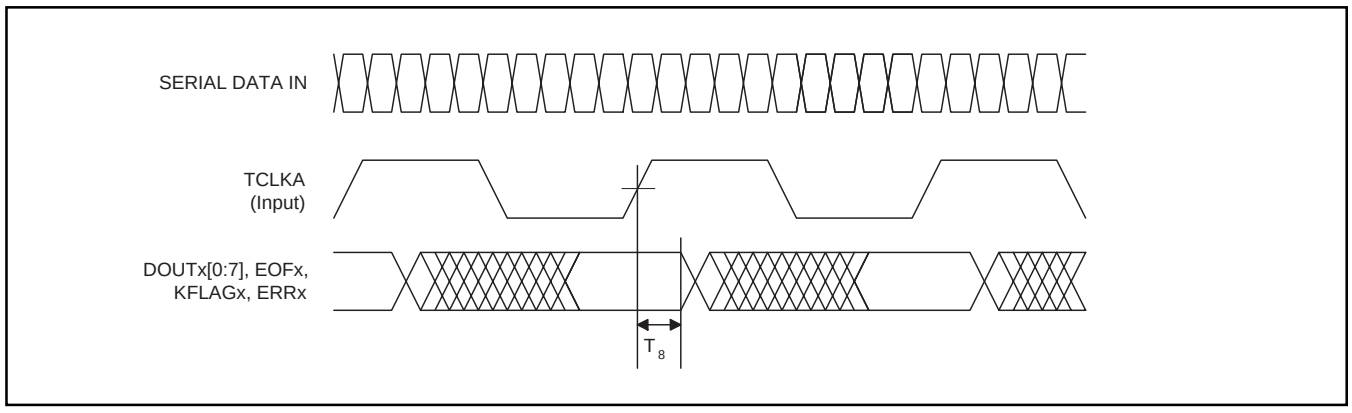


***Figure 20. TCLKO Timing***

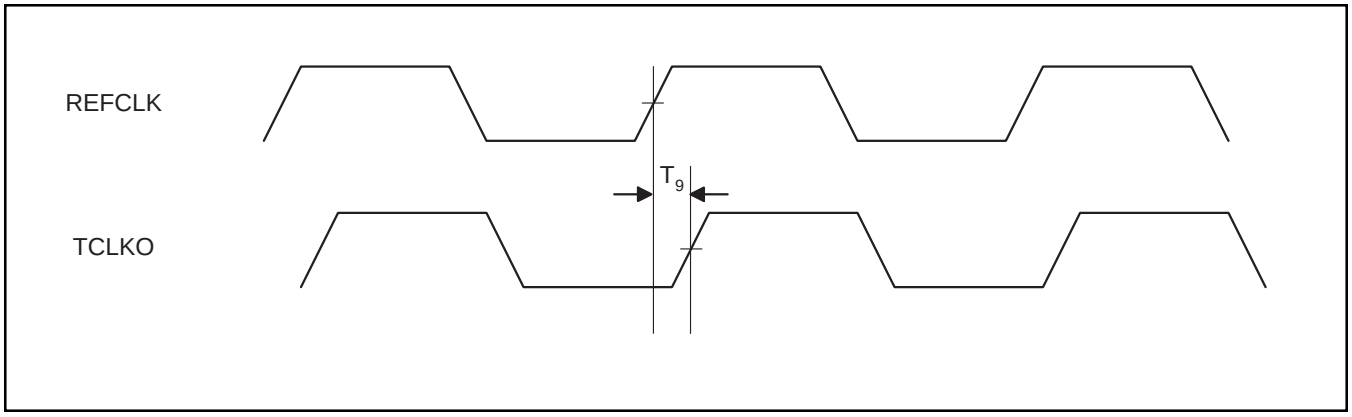



***Table 22. S2004 Transmitter (TCLKO Timing)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_9$ | ↑TCLKO w.r.t. ↑REFCLK | 1.0 | 6.5 | ns | |
| TCLKO Duty Cycle | | 45% | 55% | % | |

Note: Measurements are made at 1.4V level of clocks.

***Table 23. Absolute Maximum Ratings***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Storage Temperature | -65 | | 150 | ˚C |
| Voltage on VDD with Respect to GND | -0.5 | | +5.0 | V |
| Voltage on any TTL Input Pin | -0.5 | | 3.47 | V |
| Voltage on any PECL Input Pin | 0 | | VDD | V |
| TTL Output Sink Current | | | 8 | mA |
| TTL Output Source Current | | | 8 | mA |
| High Speed PECL Output Source Current | | | 25 | mA |
| ESD Sensitivity[1] | Over 500 V | | | |

1. Human body model.

***Table 24. Recommended Operating Conditions***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Ambient Temperature Under Bias | 0 | | 70 | ˚C |
| Junction Temperature Under Bias | | | 130 | ˚C |
| Voltage on any Power Pin with respect to GND/VSS | 3.13 | 3.3 | 3.47 | V |
| Voltage on any TTL Input Pin | 0 | | 3.47 | V |
| Voltage on any PECL Input Pin | VDD -2V | | VDD | V |

***Table 25. Reference Clock Requirements***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| FT | Frequency Tolerance | -100 | +100 | ppm | |
| $TD_{1-2}$ | Symmetry | 40 | 60 | % | Duty Cycle at 50% pt. |
| $T_{RCR}$, $T_{RCF}$ | REFCLK Rise and Fall Time | | 2 | ns | 20% - 80%. |
| — | Jitter | | 80 | ps | Peak-to-Peak, to maintain ≥ 77% eye opening. |

***Table 26. Serial Data Timing, Transmit Outputs***

| Parameters | Description | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| Total Jitter | Serial Data output total jitter | | | 192 | ps | Peak-to-Peak. |
| $T_{DJ}$ | Serial data output deterministic jitter | | | 80 | ps | Peak-to-Peak. |
| $T_{SR}$, $T_{SF}$ | Serial Data Output rise and fall time | | | 300 | ps | 20% - 80%. |

***Table 27. Serial Data Timing, Receive Inputs***

| Parameters | Description | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{LOCK}$ (Frequency) | Frequency Acquisition Lock Time (Loss of Lock) (1.25 Gbps) | | | 175 | µs | 8B/10B idle pattern sample basis, from device start up. |
| $T_{LOCK}$ (Phase) | Phase Acquisition Lock Time (Phase Discontinuity) (1.25 Gbps) | | | 150 | ns | 90% input data eye (see Figure 26). |
| | | | | 180 | ns | 70% input data eye. |
| $T_{DJ}$ | Deterministic Input Jitter Tolerance | 370 | | | ps | |
| Input Jitter Tolerance | Serial Data Input total jitter tolerance | 599 | | | ps | Peak-to-Peak, as specified by IEEE 802.3z. |
| $R_{SR}$, $R_{SF}$ | Serial Data Input rise and fall time | | | 330 | ps | 20% - 80%. |

***Table 28. DC Characteristics***

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage (TTL) | 2.4 | 2.8 | VDD | V | VDD = min $I_{OH}$ = -4mA |
| $V_{OL}$ | Output Low Voltage (TTL) | GND | .025 | 0.5 | V | VDD = min $I_{OL}$ = 4mA |
| $V_{IH}$ | Input High Voltage (TTL) | 2.0 | | | V | |
| $V_{IL}$ | Input Low Voltage (TTL) | GND | | 0.8 | V | |
| $I_{IH}$ | Input High Current (TTL) | | | 40 | µA | $V_{IN}$ = 2.4 V, VDD = Max |
| $I_{IL}$ | Input Low Current (TTL) | | | 600 | µA | $V_{IN}$ = .8 V, VDD = Max |
| IDD | Supply Current | | 760 | 980 | mA | 1010 Pattern. |
| $P_D$ | Power Dissipation | | 2.5 | 3.4 | W | 1010 Pattern. |
| $V_{DIFF}$ | Min. differential input voltage swing for differential PECL inputs | 100 | | 2600 | mV | See Figure 24. |
| $\Delta V_{OUT}$ | Differential Serial Output Voltage Swing | 1400 | | 2600 | mV | See Figure 23. |
| $C_{IN}$ | Input Capacitance | | | 3 | pf | |

## OUTPUT LOAD

The S2004 serial outputs do not require output pulldown resistors.

## ACQUISITION TIME

With the input eye diagram shown in Figure 26, the S2004 will recover data with a ≤1E-9 BER within the time specified by $T_{LOCK}$ in Table 27 after an instantaneous phase shift of the incoming data.

***Figure 21. Serial Input/Output Rise and Fall Time***

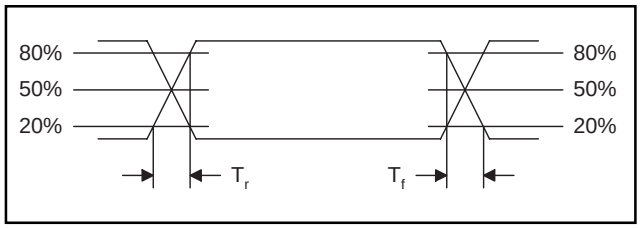



***Figure 22. TTL Input/Output Rise and Fall Time***

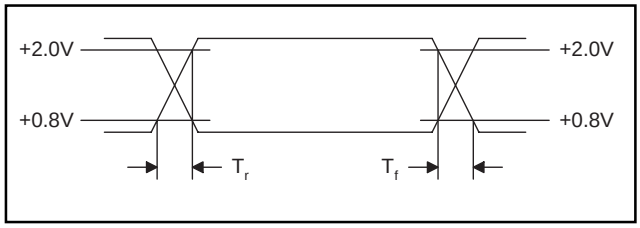



***Figure 23. Serial Output Load***

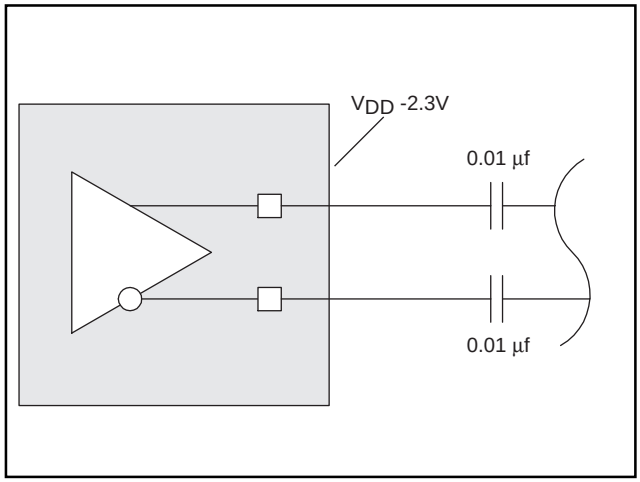



***Figure 24. High Speed Differential Inputs***

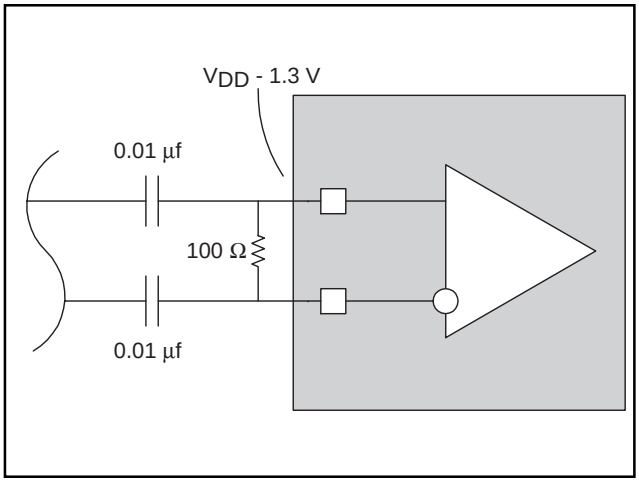



***Figure 25. Receiver Input Eye Diagram Jitter Mask***

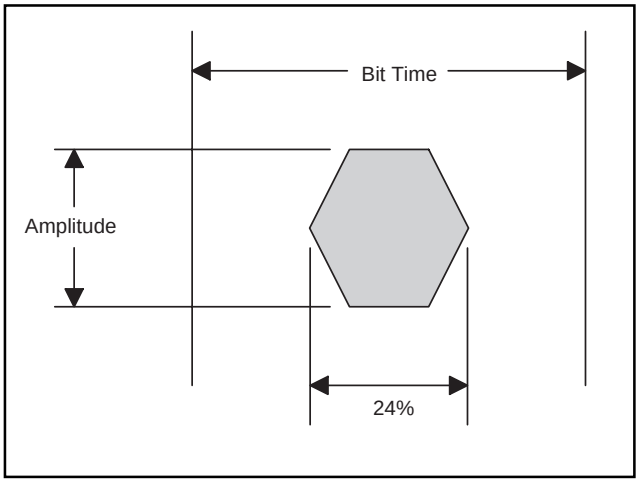



***Figure 26. Acquisition Time Eye Diagram***

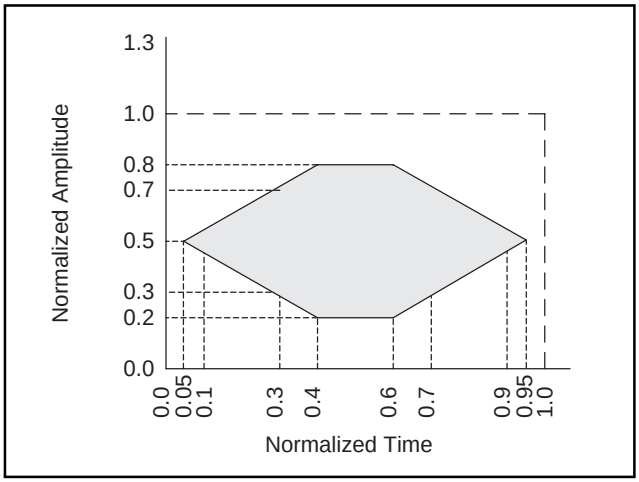
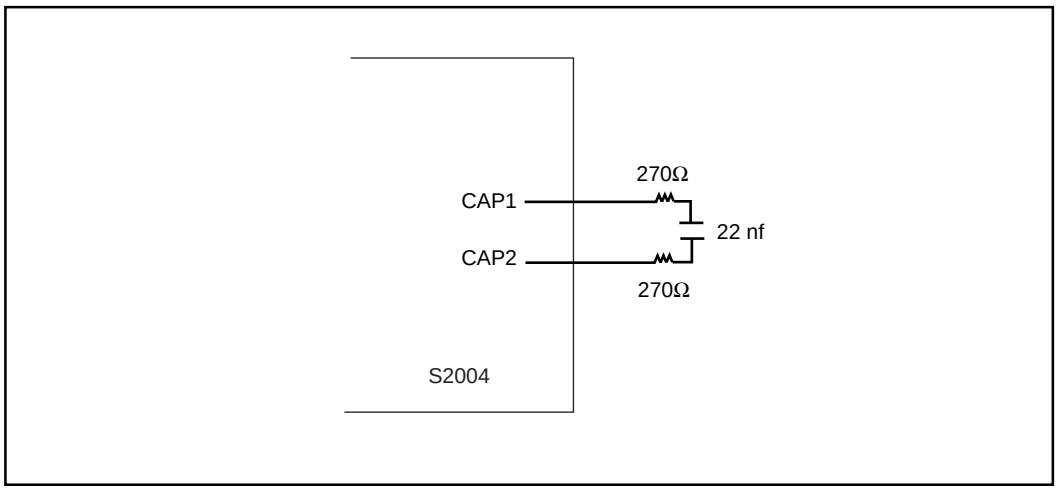
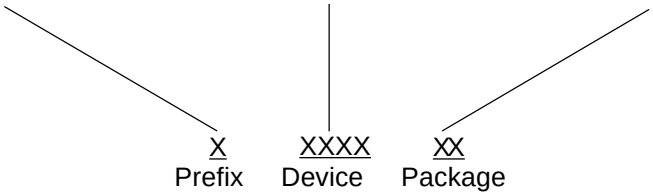


***Figure 27. Loop Filter Capacitor Connections***



***Ordering Information***

| PREFIX | DEVICE | PACKAGE |
|---|---|---|
| S- Integrated Circuit | 2004 | TB – 208 TBGA |

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