

•HYUNDAI

HYM5V64124A Q-Series

SO DIMM 1M x 64-bit CMOS DRAM MODULE
with EXTENDED DATA OUT

DESCRIPTION

The HYM5V64124A is a 1M x 64-bit EDO mode CMOS DRAM module consisting of four HY51V18164B in 42/42 pin SOJ or 44/50 pin TSOP-II and one 2048 bit EEPROM on a 144 Zig Zag Dual pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM5V64124AQQ/ATQG/ASLQG/ASLTQG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- Low power dissipation
Max. self-refresh 7.7mW (SL-part)
Max. battery back-up 9.9mW (SL-part)
Max. CMOS standby 4.4mW (SL-part)
22.0mW

Max. TTL standby 44.0mW
Max. operating

Speed	Power
60	3.74W
70	3.30W
80	2.86W

- Single power supply of 3.3V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

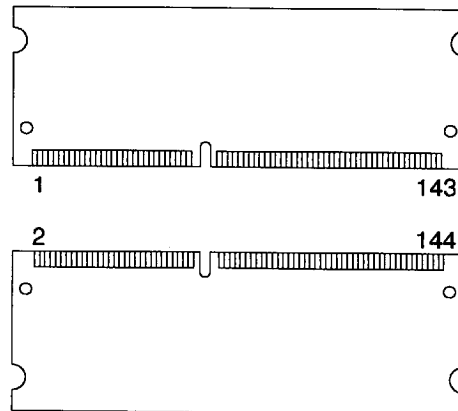
Speed	t _{RAC}	t _{CAC}	t _{HPC}
60	60ns	17ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- EDO mode operation
- CAS-before-RAS, RAS-only, Hidden refresh and Self-refresh
- 1024 refresh cycles / 256ms (SL-part)
1024 refresh cycles / 16ms
- Serial Presence Detect

PIN DESCRIPTION

RAS0	Row Address Strobe
CAS0 - CAS7	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A9	Address Input
DQ0-DQ63	Data Input/Output
SLC	Serial PD Clock Input
SDA	Serial PD Data Input/Output
Vcc	Power (+ 3.3V)
Vss	Ground

PIN CONNECTION



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PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	2	Vss	73	OE	74	NC
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	CAS0	24	CAS4	95	DQ21	96	DQ53
25	CAS1	26	CAS5	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	NC
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	NC
39	DQ9	40	DQ41	111	NC	112	NC
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	CAS2	116	CAS6
45	Vcc	46	vcc	117	CAS3	118	CAS7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	Vcc	130	Vcc
59	NC	60	NC	131	DQ28	132	DQ60
61	NC	62	NC	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	NC	66	NC	137	DQ31	138	DQ63
67	WE	68	NC	139	Vss	140	Vss
69	RAS0	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	Vcc	144	Vcc

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SERIAL PD BYTE DEFINITION

BYTENUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE
Byte 0	Number of Byte written during module production	15 Bytes	0Fh
Byte 1	Total Byte of Serial Presence Detect Device	256 Bytes	08h
Byte 2	Memory Type	EDO	02h
Byte 3	Number of ROW Addresses	10	0Bh
Byte 4	Number of COLUMN Addresses	10	0Ah
Byte 5	Number of Banks	1 Bank	01h
Byte 6	Module Data Width	64bit	60h
Byte 7	Module Data Width(Continued)	Not Used	00h
Byte 8	Module Interface Levels	LVTTTL	01h
Byte 9	tRAC	60ns 70ns 80ns	3Ch 46h 50h
Byte 10	tCAC	17ns 20ns 20ns	11h 14h 14h
Byte 11	Module Configuration Type	None	00h
Byte 12	Refresh Rate/Type	Normal(15.6μs) SL-Part(250μs)	00h 86h
Byte 13	Primary DRAM Width	x16	10h
Byte 14	Error Checking DRAM Width	None	00h
Byte 15 - 255	Undefined	Undefined	Undefined

NOTE:

1. Serial PD interface is standard IIC architecture.
2. Pull-up resistors(4.7K typical value) are required on all open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA (IOL max) must be at least 3ma to maintain a valid low level.

IIC BUS INTERFACE

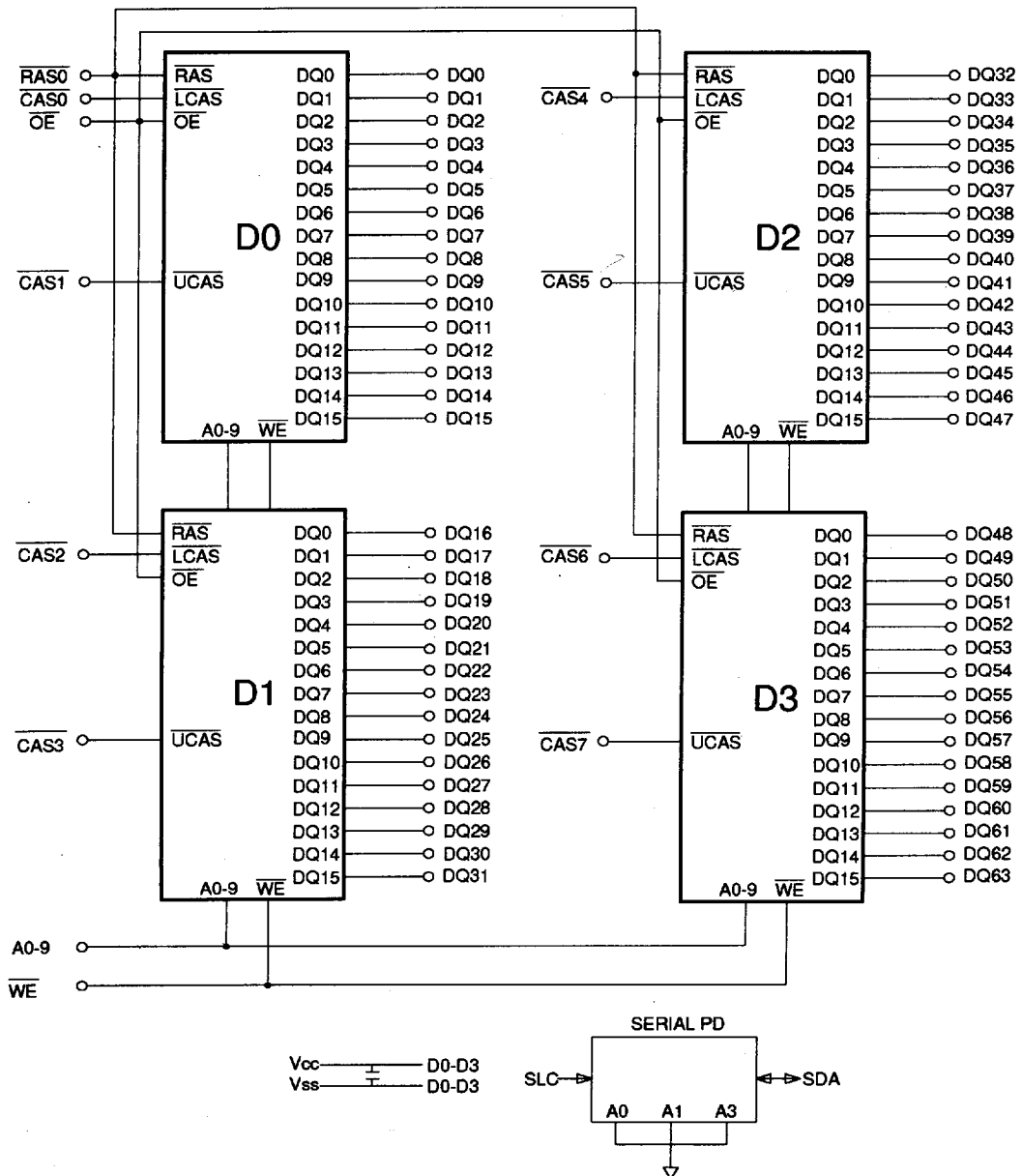
SYMBOL	RATING	NOTE
C _{MAX}	400pF	1
f _{MAX}	80 KHz(3.3V) 100 KHz(5.0V)	2
IOL _{MAX}	3mA	

NOTE:

1. The maximum number of devices connected on the IIC bus is controlled by the maximum allowable capacitance which is 400pF per line.
2. The maximum IIC system clock frequency depends on Vcc.

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 4.6	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 4.6	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	2.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	Vcc+ 0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to Vss.

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DC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 3.3V± 10%, Vss= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC+ 1.0, other pins not under test= Vss		-40	40	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
Icc1	Vcc Supply Current, Operating	tRC= tRC (min.)	60 70 80	- - -	680 600 520	mA	1,2,3
Icc2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ Vss		-	8	mA	
Icc3	Vcc Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	- - -	680 600 520	mA	1,3
Icc4	Vcc Supply Current, EDO mode	tHPC= tHPC (min.)	60 70 80	- - -	560 480 440	mA	1,2,3
Icc5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc-0.2V	SL-part	-	4 0.8	mA	
Icc6	Vcc Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	- - -	680 600 520	mA	1,3
Icc7	Vcc Supply Current, Battery Back Up (SL-part only)	tRC= 250μs CAS= CBR cycling or 0.2V WE= Vcc-0.2V, A0-A9= Vcc - 0.2V or 0.2V DQ0-DQ63= Vcc - 0.2V, 0.2V or open	tRAS ≤ 300ns tRAS ≤ 1μs	- - -	1.4 1.8	mA	1,4,5
Icc8	Vcc Supply Current, Self Refresh (SL-part)	RAS & CAS= VIL OE & WE & A0-A9= Vcc - 0.2V or 0.2V DQ0-DQ63= Vcc - 0.2V, 0.2 or open		-	1.4	mA	5
VOL	Output Low Voltage	IOL= 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2.0mA		2.4	-	V	

NOTE :

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
- Icc1, Icc3, Icc4, and Icc6 depend on output loading. Specified values are obtained with the output open.
- Icc is specified as average current. for Icc1, Icc3, and Icc6, address can be changed maximum two times while RAS= VIL for Icc4, address can be changed maximum once while CAS= VIH.
- Only tRAS(max.)= 1μs is applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operation.
- Icc5(max.)= 0.8mA, Icc7 and Icc8 are applied to SL-part (HYM5V64124ASLQG/ASLTQG).

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AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 3.3V± 10%, Vss = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V64124A Q-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	142	-	167	-	187	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	73	-	85	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	13	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	40	-	50	-	60	-	ns	
17	tCAS	CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	30	-	35	-	35	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	30	-	35	-	35	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	15	-	ns	
35	tCWL	Write Command to CAS Lead Time	13	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	30	-	35	-	35	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

continued

#	SYMBOL	PARAMETER	HYM5V64124A Q-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	37	-	45	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	80	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	50	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	17	-	20	-	20	ns	
50	tOED	OE to Data Delay	15	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	15	ns	5
52	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	

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NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM5V64124A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY51V18164B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. (VOH= 2.0V, VOL= 0.8V)
5. tCEZ(max.), tOEZ(MAX), tREZ(MAX) and tWEZ(MAX) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in late write or read-modify-write cycles.
8. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. Measured with the specified current load and 100pF.
12. A burst of 1024 CAS-before-RAS refresh cycles must be executed within 16ms after exiting self refresh (for SL-part).
13. If tcWD $\geq$ twCS(MIN.), tRWD $\geq$ tRWD(MIN.), tAWD $\geq$ tAWD(MIN.) and tCPWD $\geq$ tCPWD(MIN.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until CAS goes back to VIH) is indeterminated.
14. In CAS before RAS self refresh mode.
In case of using distributed CAS before RAS refresh, refresh 1024 times during a 256ms after reset
In case of using burst CAS before RAS refresh, refresh 1024 times during a 16ms after reset
In case of using RAS only refresh, refresh against all refresh address during a 16ms after reset
15. If RAS goes to high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes to high before RAS high going, the open circuit condition of the output is achieved by RAS high going.

CAPACITANCE

(TA= 25°C, VCC= 3.3V $\pm$ 10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	30	pF
CIN2	Input Capacitance (WE,OE)	-	38	pF
CIN3	Input Capacitance (RAS0)	-	40	pF
CIN4	Input Capacitance (CAS0-CAS7)	-	17	pF
CbQ	Data Input/output Capacitance (DQ0-DQ63)	-	17	pF

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144 pin Small Out-line Dual In-line Memory Module(QG ; Gold plated)[illegible]

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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V64124AQQ	60/70/80		DIMM	Gold
HYM5V64124ASLQG	60/70/80	SL-part	DIMM	Gold
HYM5V64124ATQG	60/70/80		DIMM	Gold
HYM5V64124ASLTQG	60/70/80	SL-part	DIMM	Gold

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