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FAST Products	

FAST 74F378

Flip-Flop

Hex D Flip-Flop With Enable

FEATURES

- 6-bit high-speed parallel register
- Positive edge-triggered D-type Inputs
- Fully buffered common Clock and Enable inputs
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\bar{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output. The $\bar{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
16-Pin Plastic DIP	N74F378N
16-Pin Plastic SO	N74F378D

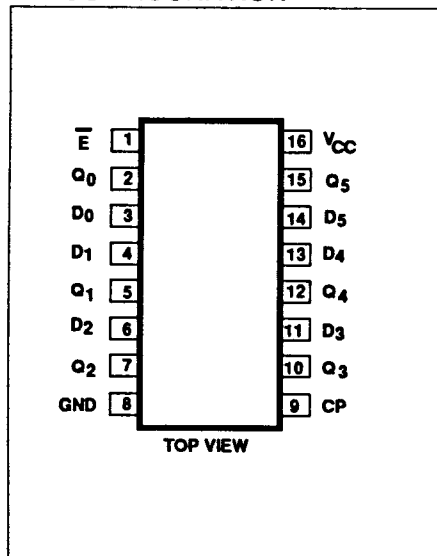
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_5$	Data inputs	1.0/1.0	20 μ A/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
$\bar{E}$	Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
$Q_0 - Q_5$	Data outputs	50/33	1.0mA/20mA

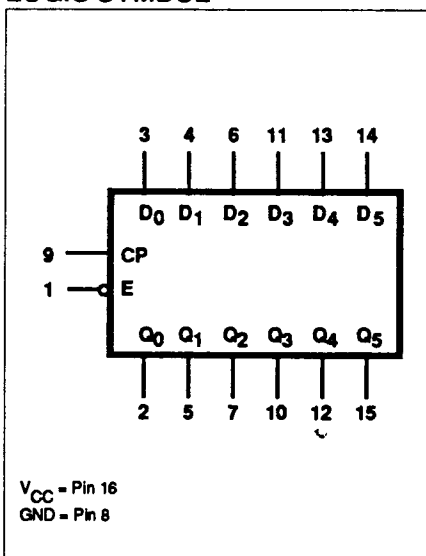
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

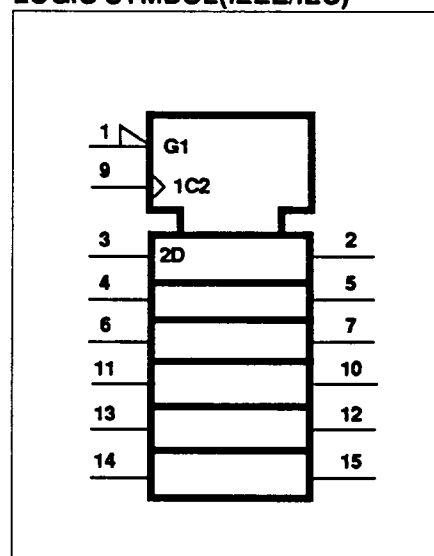
PIN CONFIGURATION



LOGIC SYMBOL



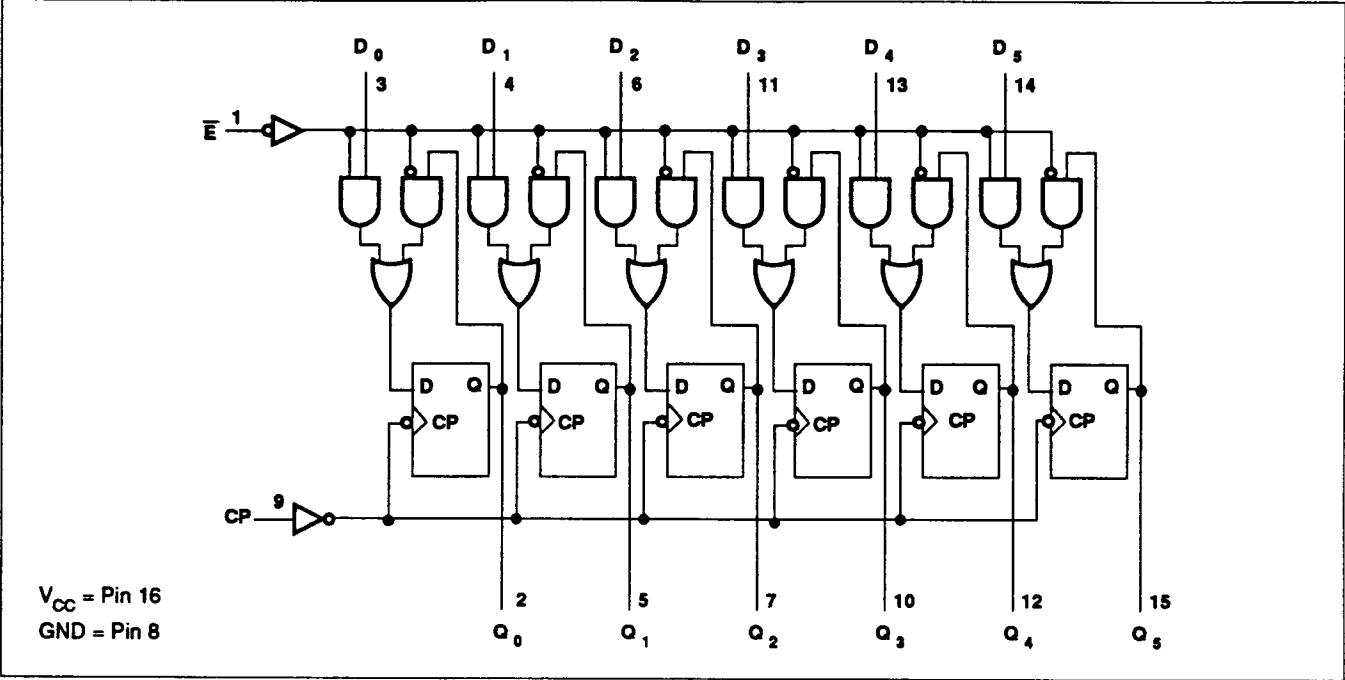
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	D_n	Q_n	
l	$\uparrow$	h	H	Load "1"
l	$\uparrow$	l	L	Load "0"
h	$\uparrow$	X	no change	Hold (do nothing)
H	X	X	no change	

- H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
 $\uparrow$ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

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RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT
				Min	Typ ²	Max	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\% V_{CC}$	2.5			V
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\% V_{CC}$	2.7	3.4		-V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\% V_{CC}$		0.30	0.50	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\% V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA
I_{ILL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		32	45	mA
		I_{CCL}			35	45	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable typ5
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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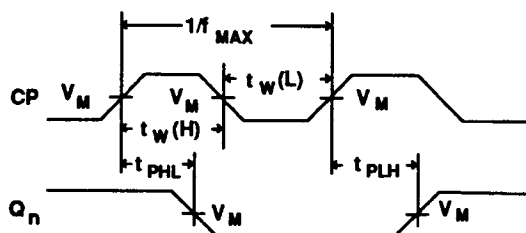
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns

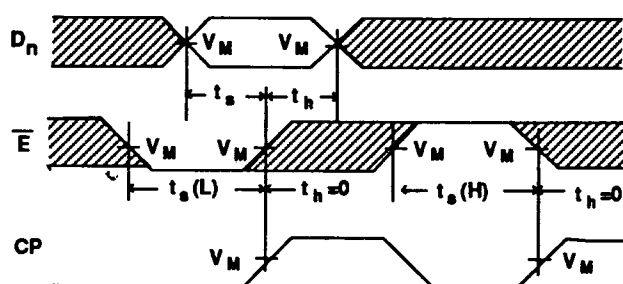
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low D_n to CP	Waveform 2	0 0			0 0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $\overline{\text{E}}$ to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $\overline{\text{E}}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2.
Data And Enable Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5\text{V}$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS

