



Complete, 8-Channel, 12-Bit Data-Acquisition Systems

MAX180/MAX181/883B

1.0 SCOPE

- 1.1** This specification covers the detail requirements for two data-acquisition systems. These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's standard data books.

1.2 Part Numbers

Device	Part Number
-1	MAX180AM(X)L
-2	MAX180BM(X)L
-3	MAX180CM(X)L
-4	MAX181AM(X)L
-5	MAX181BM(X)L
-6	MAX181CM(X)L

1.3 Package

(X)	Package	Description
J	J-40	40-Pin Ceramic Dual-In-Line Package (CERDIP)
D	D-40	40-Pin Ceramic Sidebrazed Package

Note: See *Package Information* section for drawing and dimensions.

1.4 Absolute Maximum Ratings

V_{DD} to DGND	-0.3V, +7V
V_{SS} to DGND	-0.3V, -17V
AGND to DGND	-0.3V, ($V_{DD} + 0.3V$)
A_{IN-} , MUXOUT, ADCIN, REFADJ, OFFADJ to REFIN	-0.3V, ($V_{DD} + 0.3V$)
REFIN to DGND	+0.3V, ($V_{SS} - 0.3V$)
\overline{CS} , \overline{WR} , \overline{RD} , CLK, A2-A0, BIP, DIFF, HBEN to DGND	-0.3V, ($V_{DD} + 0.3V$)
\overline{BUSY} , D0-D11 to DGND	-0.3V, ($V_{DD} + 0.3V$)
Continuous Power Dissipation ($T_j = +150^\circ\text{C}$)	
to $+70^\circ\text{C}$	1000mW
derates above $+70^\circ\text{C}$ by	10mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+160^\circ\text{C}$
Lead Temperature (soldering, 10sec)	$+300^\circ\text{C}$



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1.5 Thermal Resistance $\theta_{JC} = 25^{\circ}\text{C/W}$ for J-40
 $\theta_{JA} = 50^{\circ}\text{C/W}$ for J-40

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	CONDITIONS (Notes 1, 2)	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
ACCURACY (Note 3)							
Resolution	N		All	1, 2, 3	12		Bits
Integral Nonlinearity Error	INL	MAX18_A	-1, -4	1, 2, 3	±3/4		LSB
		MAX18_B/C	-2, -3, -5, -6		±1		
Differential Nonlinearity	DNL	Guaranteed monotonic over temp.	All	1, 2, 3	±1		LSB
Unipolar Offset Error (Note 4)			All	1, 2, 3	±4		LSB
Bipolar Offset Error (Note 4)			All	1, 2, 3	±6		LSB
Unipolar Gain Error			All	1, 2, 3	±10		LSB
Bipolar Gain Error			All	1, 2, 3	±15		LSB
Gain-Error Tempco (Notes 5, 6)			All		±5		ppm/°C
DYNAMIC PERFORMANCE (Note 3)							
Signal-to-Noise + Distortion Ratio	SINAD	10kHz input signal, 100kHz sampling rate, bipolar mode, $T_A = +25^{\circ}\text{C}$	All	9	70		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	10kHz input signal, 100kHz sampling rate, bipolar mode, $T_A = +25^{\circ}\text{C}$	All	9	-80		dB
Spurious-Free Dynamic Range	SFDR	10kHz input signal, 100kHz sampling rate, bipolar mode, $T_A = +25^{\circ}\text{C}$	All	9	80		dB
Full-Power Sampling Bandwidth (Note 5)		In track mode, undersampled	All		6		MHz
Track/Hold Acquisition Time (Note 5)	t_{ACQ}		All		1.875		μs
Conversion Time	t_{CONV}	Asynchronous hold mode (Note 5)	All	9, 10, 11	7.500	8.125	μs
		ROM, slow-memory, and I/O port modes; 15-16 clock cycles			9.375	10.000	

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TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS (Notes 1, 2)	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
ANALOG INPUT							
Voltage Range		AIN ₋ , MUXOUT, and ADCIN	All	1, 2, 3	REFIN	V _{DD}	V
Unipolar, Single-Ended Range		AIN ₋ to AGND	All	1, 2, 3	0	5.0	
Unipolar, Differential Range		AIN ₊ to AIN ₋	All	1, 2, 3	0	5.0	
Bipolar, Single-Ended Range		AIN ₋ to AGND	All	1, 2, 3	-2.5	2.5	
Bipolar, Differential Range		AIN ₊ to AIN ₋	All	1, 2, 3	-2.5	2.5	
Input Current		AIN ₋ , MAX180	-1, -2, -3	1, 2, 3	±1.0		µA
		ADCIN, MAX181	-4, -5, -6		±0.1		
Mux-On Resistance	r _{ON}	AIN ₋ = 2.5V, I _{MUXOUT} = 1.25mA, MAX181	-4, -5, -6	1, 2, 3	2		kΩ
Mux-On Leakage Current	I _{ON}	AIN ₋ = MUXOUT = ±5V, MAX181	-4, -5, -6	1, 2, 3	±100		nA
Mux-Off Leakage Current	I _{IN(OFF)}	AIN ₋ = ±5V, V _{OUT} = ±5V, MAX181	-4, -5, -6	1, 2, 3	±100		nA
	I _{OUT(OFF)}	AIN ₋ = ±5V, V _{OUT} = ±5V, MAX181	-4, -5, -6	1, 2, 3	±100		
Input Capacitance (Note 5)	C _{IN}	AIN ₋ , ADCIN	-4, -5, -6		35		pF
		MUXOUT	-4, -5, -6		45		
REFERENCE INPUT							
Input Range (Note 5)			All		-4.92	-5.08	V
Input Current			All	1, 2, 3	-2		mA
Input Resistance			All	1, 2, 3	2.5		kΩ
REFERENCE OUTPUT							
VREF Output Voltage		T _A = +25°C	All	1	-4.98	-5.02	V
VREF Output Tempco (Note 7)		MAX18_A/B	-1, -2, -4, -5	1, 2, 3	25		ppm°C
		MAX18_C	-3, -6		45		
VREF Load Regulation (Note 8)		I _{OUT} = 0mA to 5mA, T _A = +25°C	-3, -6	1	1.0		mV/mA
REFADJ, OFFADJ							
Input Current		V _{REFADJ} , V _{OFFADJ} = V _{DD} to REF _{IN}	All	1, 2, 3	±1		µA
Disable Threshold			All	1, 2, 3	4.5		V
REFADJ Adjustment Range		REF _{IN} < REFADJ < AGND	All	1, 2, 3	±60		mV
OFFADJ Adjustment Range		REF _{IN} < OFFADJ < AGND	All	1, 2, 3	±15		LSB

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TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS	
					MIN	MAX		
LOGIC INPUTS								
Input Low Voltage	V _{IL}	MODE	All	1, 2, 3	0.5		V	
		\overline{CS} , \overline{RD} , \overline{WR} , CLK, A2-A0, DIFF, BIP, HBEN	All	1, 2, 3	0.8			
Input High Voltage	V _{IH}	MODE	All	1, 2, 3	4.5		V	
		\overline{CS} , \overline{RD} , \overline{WR} , CLK, A2-A0, DIFF, BIP, HBEN	All	1, 2, 3	2.4			
Input Mid-Level Voltage	V _{MID}	MODE	All	1, 2, 3	1.5	3.5	V	
Input Floating Voltage (Note 5)	V _{FLT}	MODE	All		2.5		V	
Input Current	I _{IN}	MODE	All	1	±100		µA	
					T _A = T _{MIN} to T _{MAX}	±100		
		\overline{CS} , \overline{RD} , \overline{WR} , CLK, A2-A0, DIFF, BIP, HBEN		T _A = +25°C	1	±1		
					1, 2, 3	±10		
Input Capacitance (Note 5)	C _{IN}		All		15		pF	
LOGIC OUTPUTS								
Output Low Voltage	V _{OL}	D11-D0, \overline{BUSY} , RDY, ISINK = 1.6mA	All	1, 2, 3	0.4		V	
Output High Voltage	V _{OH}	D11-D0, \overline{BUSY} , RDY, ISOURCE = 360µA	All	1, 2, 3	4.0		V	
Floating-State Leakage Current	I _{LKG}	D11-D0, V _{OUT} = 0V to V _{DD}	All	1, 2, 3	±10		µA	
Floating-State Output Capacitance (Note 5)	C _{OUT}		All		15		pF	
POWER REQUIREMENTS								
Supply Voltage (Note 2)	V _{DD}		All	1, 2, 3	4.75	5.25	V	
	V _{SS}				-11.40	-15.75		
Supply Current	I _{DD}	V _{DD} = 5V	All	1, 2, 3	7.0		mA	
	I _{SS}	V _{SS} = -15V			10.0			
Power Dissipation	PD	V _{DD} = 5V, V _{SS} = -15V	All	1, 2, 3	155		mW	
Power-Supply Rejection with Internal Reference	PSR	Input near FS, V _{SS} = -12V, V _{DD} = 4.75V to 5.25V	All	1, 2, 3	±1		LSB	
		Input near FS, V _{DD} = 5V, V _{SS} = -14.25V to -15.75V			±1/2			
		Input near FS, V _{DD} = 5V, V _{SS} = -11.4V to -12.6V			±1/2			

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TABLE 2. TIMING CHARACTERISTICS

CHARACTERISTICS	SYMBOL	CONDITIONS (Notes 3, 9)	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
\overline{CS} to \overline{RD} Setup Time	t ₁	(Note 5)	All		0		ns
\overline{CS} to \overline{RD} Hold Time	t ₂		All	9, 10, 11	0		ns
\overline{CS} to \overline{WR} Setup Time	t ₃		All	9, 10, 11	0		ns
\overline{CS} to \overline{WR} Hold Time	t ₄	(Note 5)	All		0		ns
\overline{WR} Low Pulse Width	t ₅		All	9, 10, 11	120		ns
\overline{WR} High Pulse Width	t ₆	MODE = 0 or 1 (Note 5)	All		200		ns
DATA IN to \overline{WR} Setup Time	t ₇		All	9 10, 11	80 120		ns
DATA IN to \overline{WR} Hold Time	t ₈		All	9, 10, 11	0		ns
\overline{WR} Rising to \overline{BUSY} Delay	t ₉	C _L = 50pF, MODE = 1	All	9 10, 11	160 200		ns
\overline{WR} Falling to \overline{BUSY} Delay	t ₁₀	C _L = 50pF, MODE = open	All	9 10, 11	220 280		ns
\overline{RD} Low Pulse Width	t ₁₁		All	9 10, 11	100 150		ns
\overline{RD} High Pulse Width	t ₁₂	(Note 5)	All		200		ns
DATA IN to \overline{RD} Setup Time	t ₁₃		All	9 10, 11	80 120		ns
DATA IN to \overline{RD} Hold Time	t ₁₄		All	9, 10, 11	0		ns
\overline{RD} to \overline{BUSY} Fall Delay	t ₁₅	C _L = 50pF	All	9 10, 11	150 200		ns
\overline{RD} to Data Out Valid	t ₁₆	C _L = 100pF (Note 10)	All	9 10, 11	100 150		ns
\overline{RD} to Data Out Three-State	t ₁₇	(Notes 10, 11)	All	9 10, 11	50 75		ns
HBEN to \overline{RD} or \overline{WR} Setup Time	t ₁₈		All	9 10, 11	80 120		ns

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TABLE 2. TIMING CHARACTERISTICS (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS (Notes 3, 9)	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
HBEN to \overline{RD} or \overline{WR} Hold Time	t ₁₉		All	9, 10, 11	0		ns
\overline{CS} to \overline{READY} Fall Delay	t ₂₀	C _L = 50pF	All	9	110	ns	
				10, 11	150		
\overline{BUSY} to Data Out Valid	t ₂₁	C _L = 100pF (Note 10)	All	9	125	ns	
				10, 11	170		
\overline{CS} , \overline{RD} or \overline{WR} to CLK Setup Time for 15 Clock Conversion	t ₂₂	(Note 5)	All		220	ns	
\overline{CS} , \overline{RD} or \overline{WR} to CLK Setup Time for 16 Clock Conversion	t ₂₃	(Note 5)	All		0	ns	

Note 1: V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, internal reference mode, bipolar mode, slow-memory mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Note 2: Performance at power-supply tolerance limits guaranteed by power-supply rejection test.

Note 3: V_{DD} = +5V, V_{SS} = -12V, f_{CLK} = 1.6MHz, internal reference mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Note 4: Typical change over temperature is ±1LSB.

Note 5: Characteristics supplied for use as a typical design limit, but not production tested.

Note 6: FS Tempco = ΔFS/ΔT, where FS is full-scale change from T_A = +25°C to T_{MIN} or to T_{MAX}.

Note 7: REFIN TC = ΔREFIN/ΔT, where ΔREFIN is reference voltage change from T_A = +25°C to T_{MIN} or to T_{MAX}.

Note 8: Load current should remain constant during conversion. This current is in addition to the DAC input current.

Note 9: All inputs are 0V to +5V swing with t_r = t_f = 5ns (10% to 90% of 5V) and timed from a +1.6V voltage level.

Note 10: t₁₆ and t₂₁ are measured with the load circuits of Figure 1 (C_L = 100pF) and defined as the time required for an output to cross 0.8V or 2.4V.

Note 11: t₁₇ is defined as the time required for the data lines to change 0.5V when the circuit load is as shown in Figure 2 (C_L = 10pF).

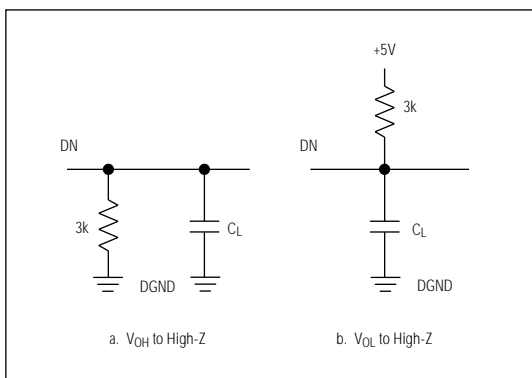


Figure 1. Load Circuits for Bus-Relinquish Time

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3.0 QUALITY ASSURANCE

- 3.1** Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.
- 3.2** Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
- (1) Test condition A, B, C, or D.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Interim and final electrical test requirements shall be as specified in Table 3.
- 3.3** Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C and D inspection.
- Group A inspection:
- (1) Tests as specified in Table 3.
 - (2) Selected subgroups in Tables 1 and 2, Method 5005 of MIL-STD-883 shall be omitted.
 - (3) Subgroup 4 (C_{IN} and C_{OUT}) shall be measured only for the initial test and after process or design changes, which may affect input or output capacitance.
- 3.4** Groups C and D inspections:
- a. End-point electrical parameters shall be specified in Tables 1 and 2.
 - b. Steady-state life test (Method 1005 of MIL-STD-883):
 - (1) Test conditions A, B, C, or D.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 3. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Tables 1 and 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,*2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3 ,4,** 9
Groups C and D End-Point Electrical Parameters (Method 5005)	1
Additional Electrical Subgroups for Group C Periodic Inspections	1

*PDA applies to Subgroup 1 only.

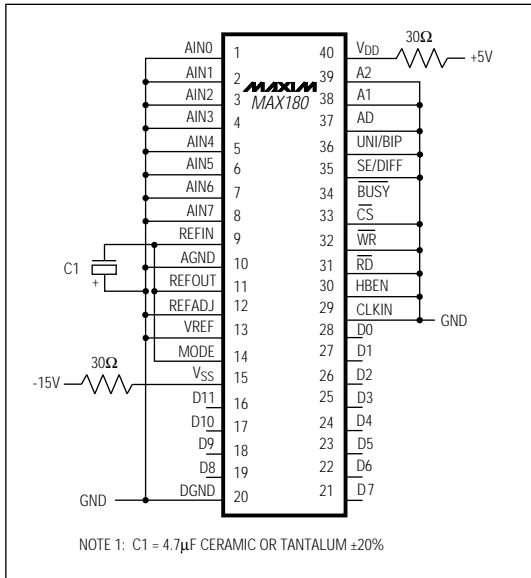
**Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.

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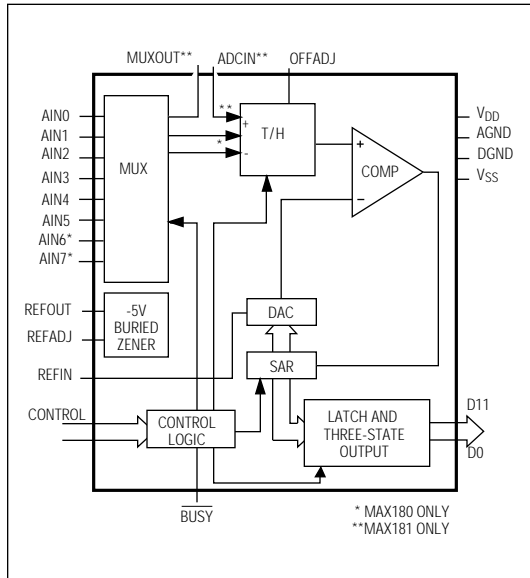
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4.0 DETAILED DESCRIPTION

4.1 Life Test/Burn-in Circuits



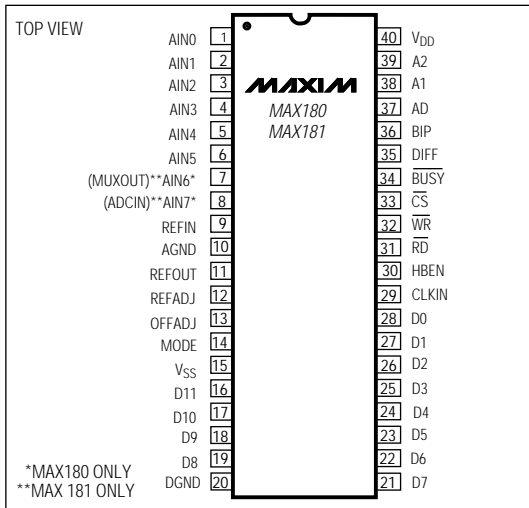
4.2 Functional Diagram



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4.3 Pin Configuration



4.4 Pin Description

NAME	MAX180	MAX181	FUNCTION
AIN0-AIN5	1-6	1-6	Analog inputs to the mux: 0V to +5V unipolar, -2.5V to +2.5V bipolar
AIN6-AIN7	7, 8		Analog inputs to the mux: 0V to +5V unipolar, -2.5V to +2.5V bipolar
MUXOUT		7	Multiplexer Output
ADCIN		8	Analog Input to track/hold
REFIN	9	9	Reference Input
AGND	10	10	Analog Ground
REFOUT	11	11	-5V Reference Output
REFADJ	12	12	-5V Reference Adjust. Connect to V _{DD} if not required.
OFFADJ	13	13	Offset Adjust. Connect to V _{DD} if not required.
MODE	14	14	Interface Mode Select pin.
V _{SS}	15	15	Negative Supply: -15V or -12V
D11-D8	16-19	16-19	Three-State Data Outputs, MSB = D11
DGND	20	20	Digital Ground
D7-D0	21-28	21-28	Three-State Data Outputs, LSB = D0
CLKIN	29	29	Clock Input, TTL/CMOS compatible
HBEN	30	30	High-Byte Enable Input
RD	31	31	READ Input
WR	32	32	WRITE Input (MODE = 1 or Open) READY Output (MODE = 0)
CS	33	33	CHIP-SELECT Input
BUSY	34	34	BUSY Output
DIFF	35	35	Single-Ended Mode: DIFF = 0, Differential Mode: DIFF = 1
BIP	36	36	Unipolar Mode: BIP = 0, Bipolar Mode: BIP = 1
A0-A2	37-39	37-39	Multiplexer Channel Address Input: A2 = MSB, A0 = LSB
V _{DD}	40	40	Positive Supply: +5V Input (substrate connected to V _{DD})

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4.5 Address vs. Channel Selection Table

PART(S)	A2	A1	A0	SE/DIFF	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	COM
MAX180/MAX181	0	0	0	0	+								-
MAX180/MAX181	0	0	1	0		+							-
MAX180/MAX181	0	1	0	0			+						-
MAX180/MAX181	0	1	1	0				+					-
MAX180/MAX181	1	0	0	0					+				-
MAX180/MAX181	1	0	1	0						+			-
MAX180	1	1	0	0							+		-
MAX181	1	1	0	0	MUXOUT CONNECTED TO AGND								+,-
MAX180	1	1	1	0								+	-
MAX181	1	1	1	0	CH 0-5, AND MUXOUT ARE OPEN								-
MAX180/MAX181	0	0	0	1	+	-							
MAX180/MAX181	0	0	1	1	-	+							
MAX180/MAX181	0	1	0	1			+	-					
MAX180/MAX181	0	1	1	1			-	+					
MAX180/MAX181	1	0	0	1					+	-			
MAX180/MAX181	1	0	1	1					-	+			
MAX180	1	1	0	1							+	-	
MAX180	1	1	1	1							-	+	
MAX181	1	1	0	1	MUXOUT CONNECTED TO AGND								+,-
MAX181	1	1	1	1	CH 0-5, AND MUXOUT ARE OPEN								-

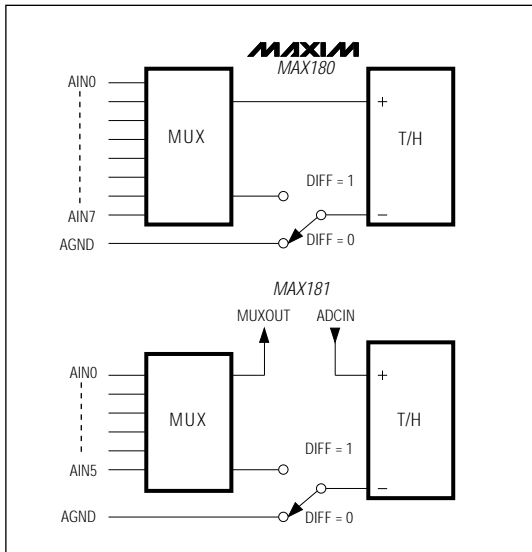


Figure 2. Multiplexer Channel Configuration

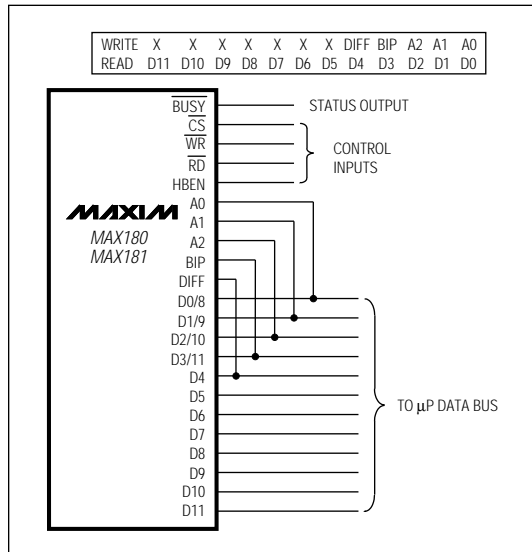


Figure 3. Input/Output Port Mode (12-Bit-Wide Data Bus Shown)

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4.6 Timing Diagrams

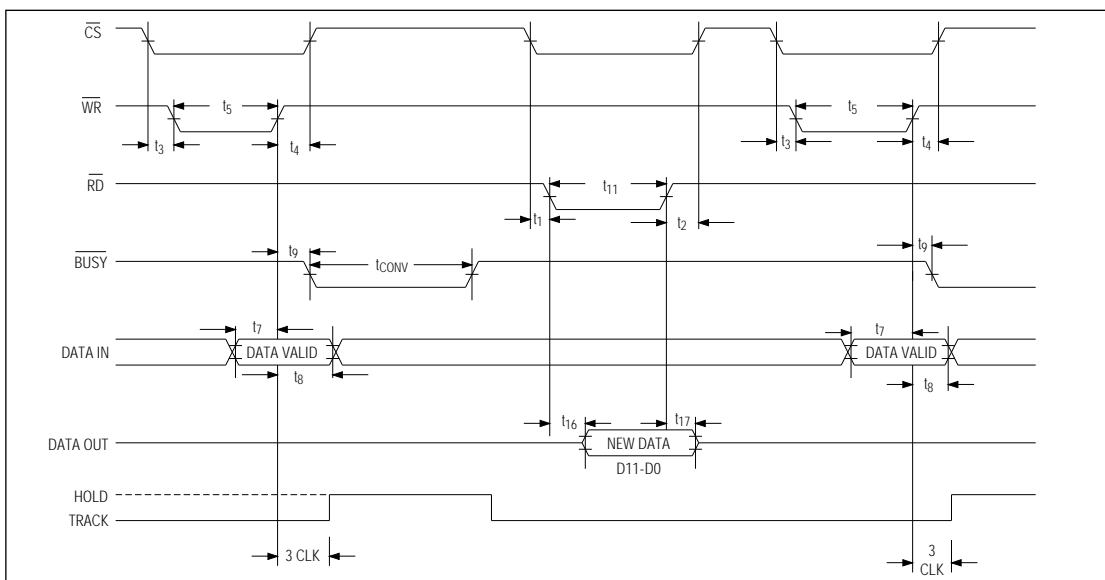


Figure 4a. Input/Output Port-Mode Timing, Parallel Read (MODE = 1, HBEN = 0)

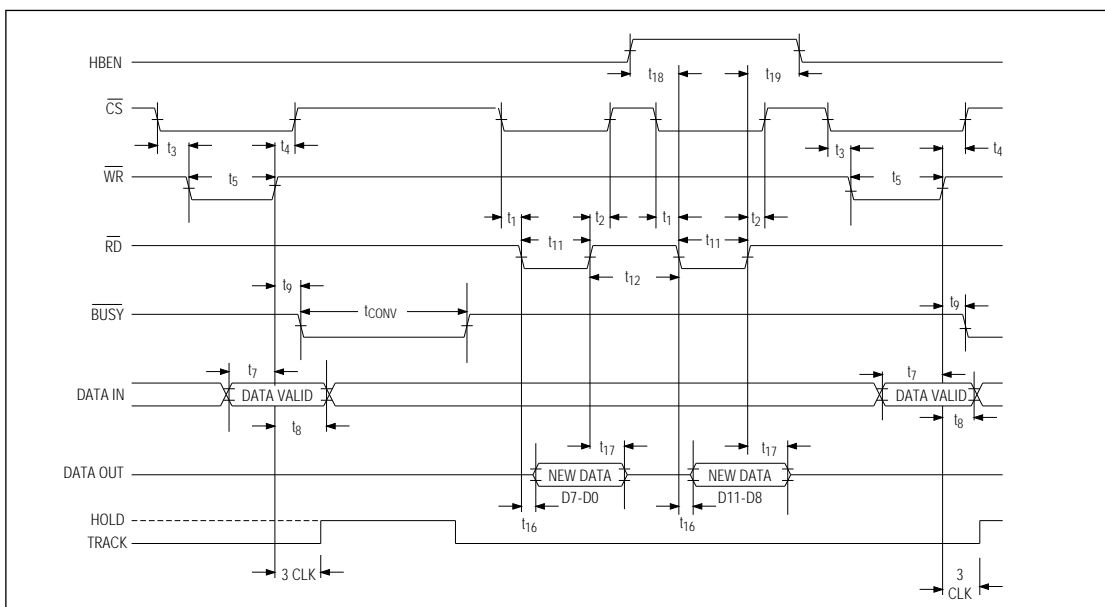


Figure 4b. Input/Output Port-Mode Timing, Two-Byte Read (MODE = 1)

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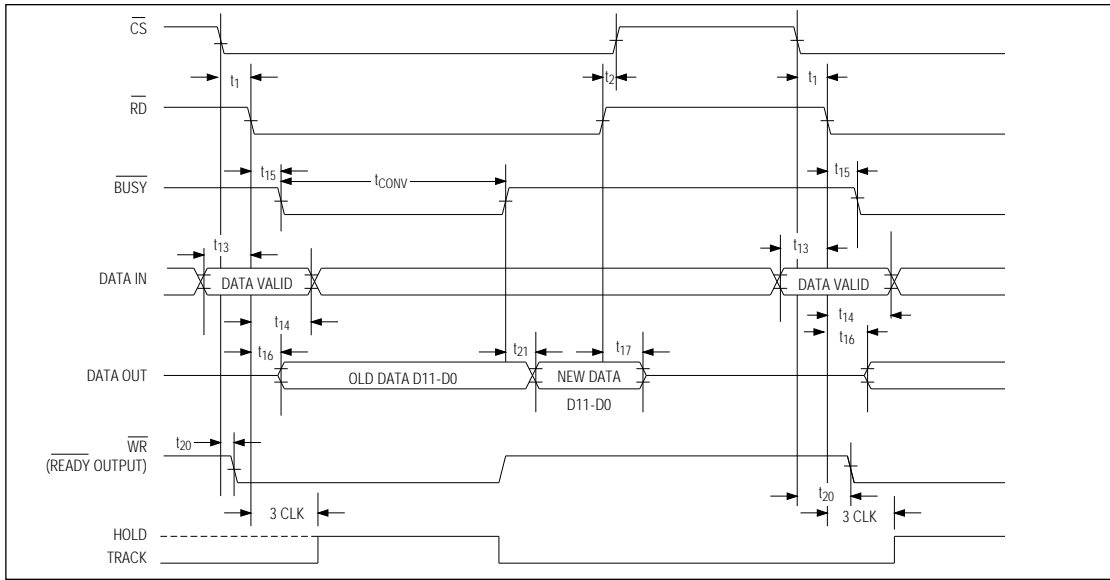


Figure 5a. Slow-Memory Mode Timing, Parallel Read (MODE = 0, HBEN = 0)

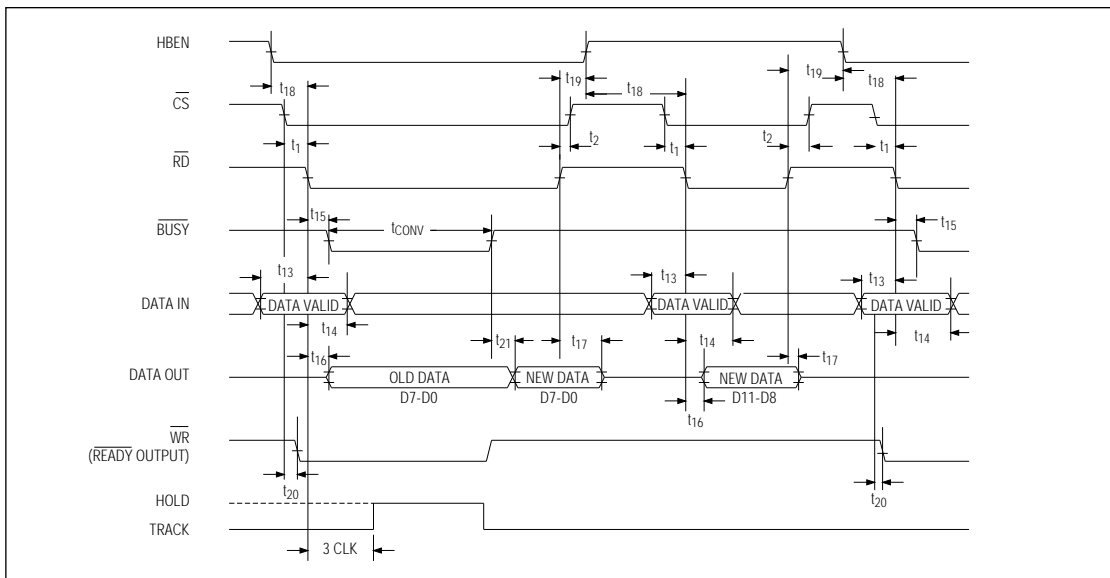


Figure 5b. Slow-Memory Mode Timing, Two-Byte Read (MODE = 0)

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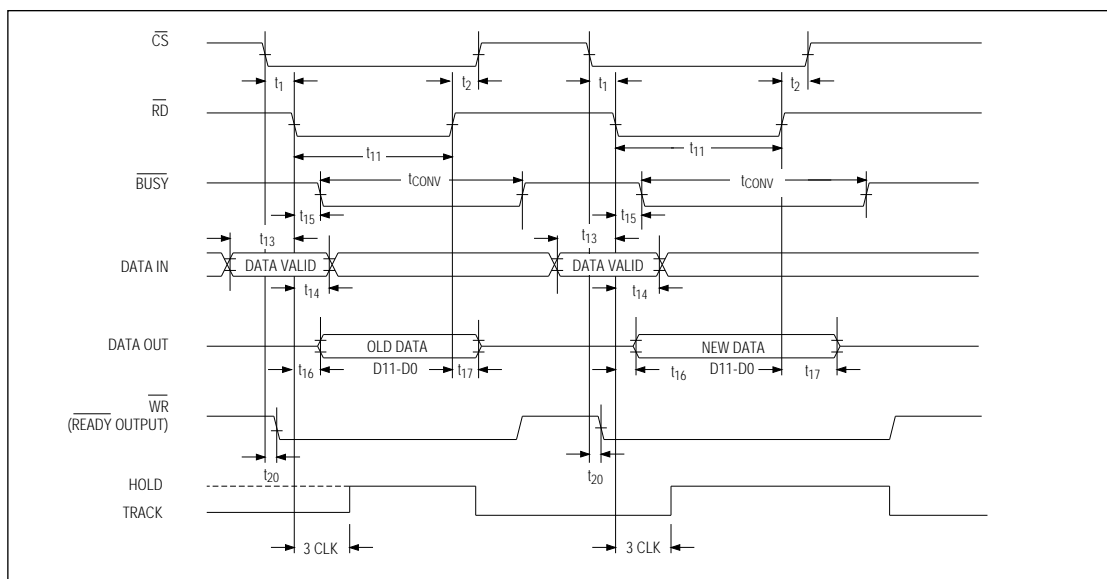


Figure 6a. ROM Mode Timing, Parallel Read (MODE = 0, HBEN = 0)

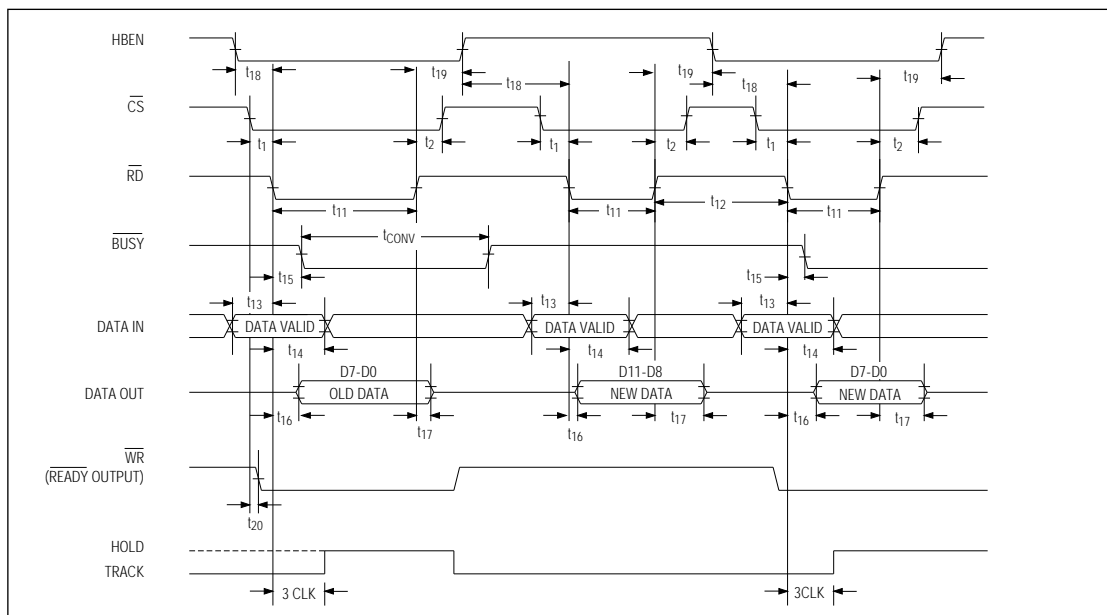


Figure 6b. ROM Mode Timing, Two-Byte Read (MODE = 0)

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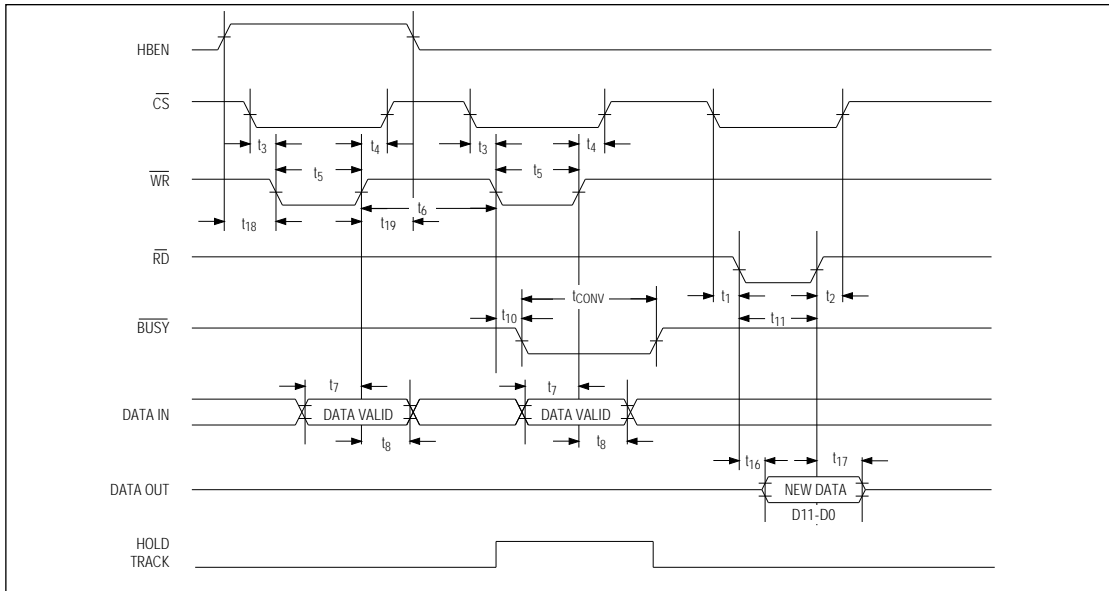


Figure 7a. Asynchronous Hold Mode Timing, Parallel Read (MODE = Open Circuit)

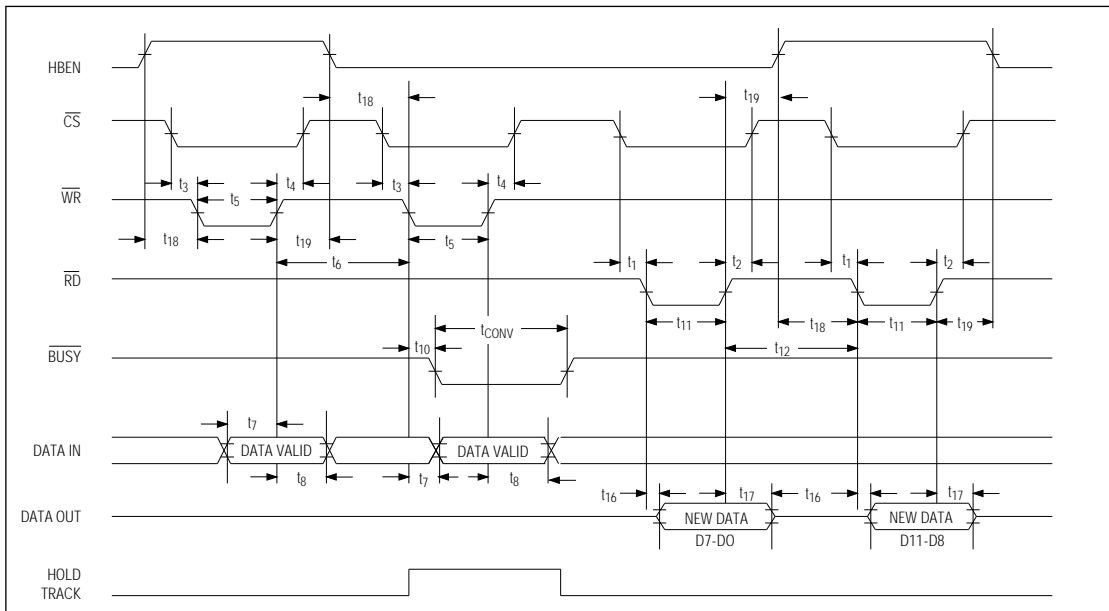


Figure 7b. Asynchronous Hold Mode Timing, Two-Byte Read (MODE = Open Circuit)

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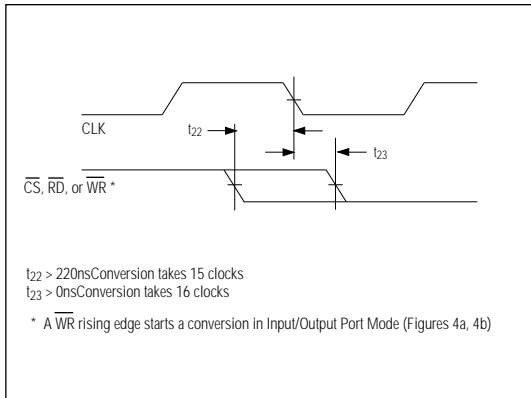
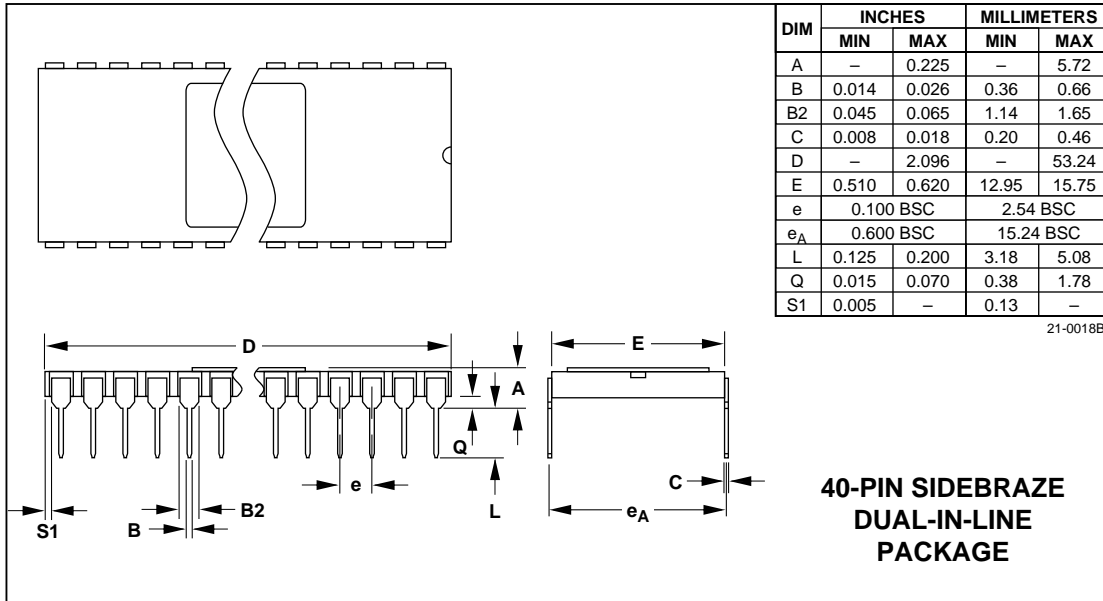


Figure 8. \overline{CS} , \overline{RD} , or \overline{WR} to CLK Setup and Hold Time for Synchronous Operation

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

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4.7 Package Information



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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