XR-215

Monolithic
Phase–Locked Loop

...the analog plus company™

June 1996-2

FEATURES

- Wide Frequency Range: 0.5Hz to 25MHz
- Wide Supply Voltage Range: 5V to 26V
- Wide Dynamic Range: 300μV to 3V, nominally
- ON–OFF Keying and Sweep Capability
- Wide Tracking Range: Adjustable from ±1% to 50%
- High–Quality FM Detection: Distortion 0.15% Signal/Noise 65dB

APPLICATIONS

- FM Demodulation
- Frequency Synthesis
- FSK Coding/Decoding (MODEM)
- Tracking Filters
- Signal Conditioning
- Tone Decoding
- Data Synchronization
- Telemetry Coding/Decoding
- FM, FSK and Sweep Generation
- Crystal–Controlled Clock Recovery
- Wideband Frequency Discrimination
- Voltage–to–Frequency Conversion

GENERAL DESCRIPTION

The XR–215 is a highly versatile monolithic phase–locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR–215 can operate over a large choice of power supply voltages ranging from 5V to 26V and a wide frequency band of 0.5Hz to 25MHz. It can accommodate analog signals between 300 microvolts and 3 volts.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR–215CP	PDIP	0°C to 70°C
XR–215D	SOIC	0°C to 70°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7010

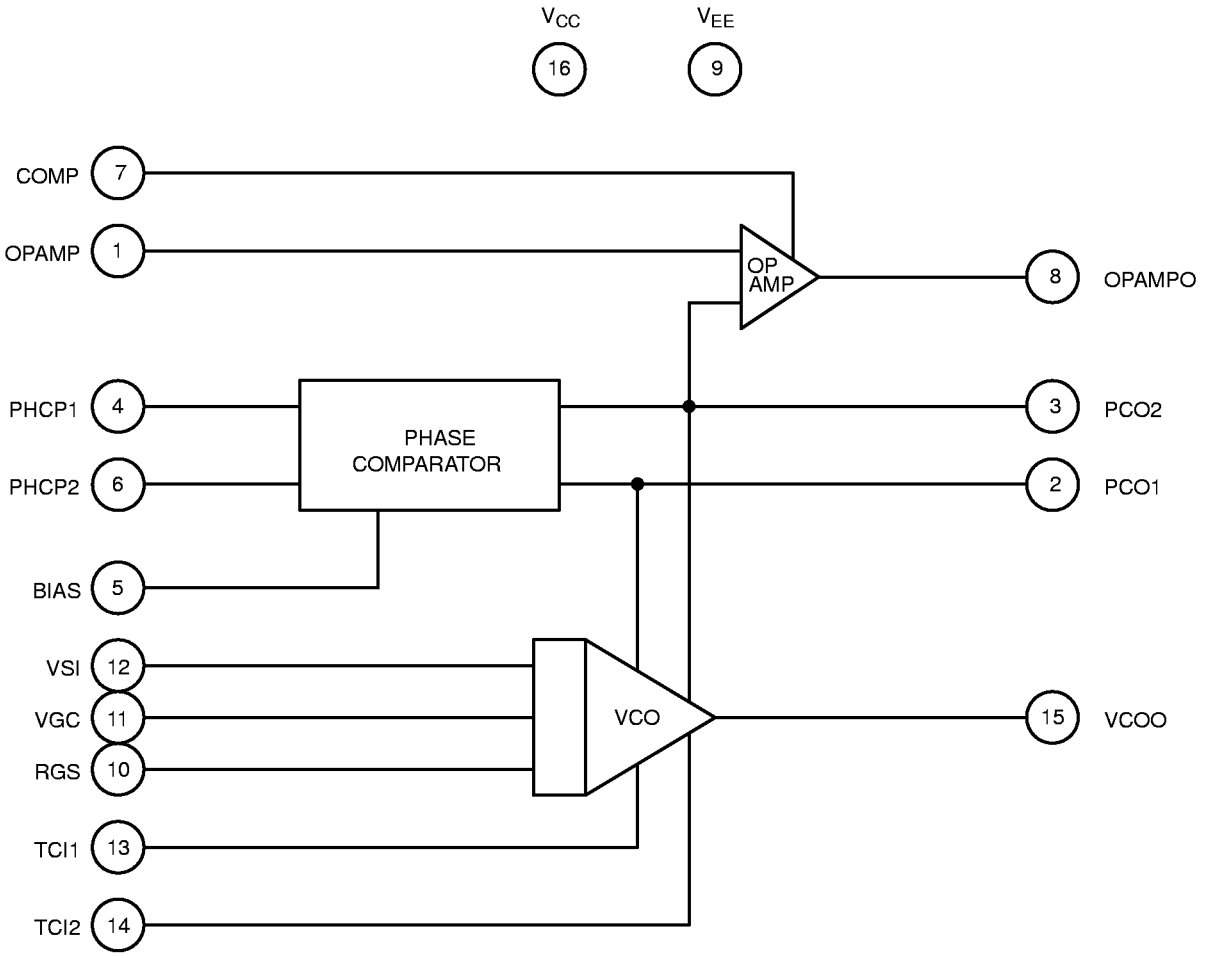
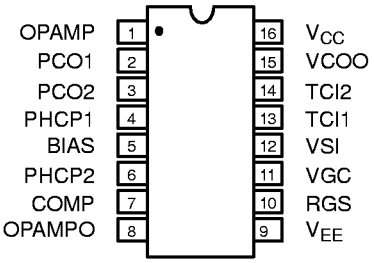
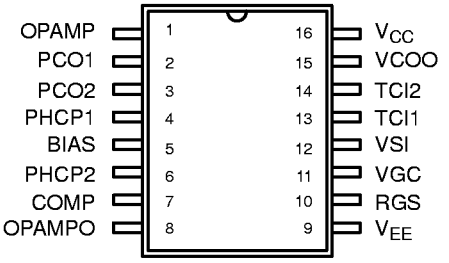


Figure 1. XR–215 Block Diagram

PIN CONFIGURATION



16 Pin PDIP



16 Pin SOIC

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	OPAMP	I	Operational amplifier input.
2	PCO1	O	Phase comparator output 1.
3	PCO2	O	Phase comparator output 2.
4	PHCP1	I	Phase comparator input 1.
5	BIAS	I	Phase comparator bias input.
6	PHCP2	I	Phase comparator input 2.
7	COMP	I	Operational amplifier frequency compensation input.
8	OPAMPO	O	Operational amplifier output.
9	V_{EE}	–	Negative power supply.
10	RGS	I	Range select input.
11	VGC	I	VCO gain control.
12	VSI	I	VCO sweep voltage input.
13	TCI1	I	Timing capacitor input. The timing capacitor connects between this pin and pin 14.
14	TCI2	I	Timing capacitor input. The timing capacitor connects between this pin and pin 13.
15	VCOO	O	VCO output.
16	V_{CC}	–	Positive power supply.

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC}= **12V** (single supply), T_A **= 25°C**, Test Circuit of *Figure 3.* with C_0 = 100 pF, (silver–mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.

	LIMITS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
I – GENERAL CHARACTERISTICS					
SUPPLY VOLTAGE					
Single Supply	5		26	V	*Figure 3.*
Split Supply	±2.5		±13	V	*Figure 4.*
Supply Current	**8**	11	**15**	mA	*Figure 3.*
Upper Frequency Limit	20	25		MHz	*Figure 3.*, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500µF (non–polarized)
VCO SECTION:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 7, 0°C ≤ T_T < 70°C
Power Supply		**0.1**		%/V	V_{CC} > 10V
Sweep Range	**5:1**	8:1			S_3 closed, S_4 open, 0 < V_S < 6V See *Figure 10.*, C_0 = 2000pF
Output Voltage Swing	**1.5**	2.5		Vp–p	S_5 open
Rise Time		20		ns	
Fall Time		30		ns	10pF to ground at Pin 15
PHASE COMPARATOR SECTION:					
Conversion Gain		2		V/rad	V_{IN} > 50mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	**100**	mV	Measured across Pins 2 and 3 V_{IN} = 0, S_5 open
OP AMP SECTION:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/µ sec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		Vp–p	R_L = 30kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	

Note: *Bold face parameters are covered by production test and quaranteed over operating temperatiure range.*

	LIMITS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
II – SPECIAL APPLICATIONS					
A) FM Demodulation Test Conditions: Test circuit of *Figure 5.*, **V_{CC} = 12V**, input signal = **10.7MHz** FM with Δf = **75kHz**. f_{mod} = **1kHz.**					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude		500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{IN} = 10mV rms, 30% AM
Output Signal/Noise		65		dB	
B) Tracking Filter Test Conditions: Test circuit of *Figure 6.*, **V_{CC} = 12V**, f_0 = **1 MHz**, V_{IN} = **100mV** rms, **50Ω source.**					
Tracking Range (% of f_0)		±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{OUT}}{\Delta f / f_0}$		50		mV/%	Adjustable – See applications information

Note: *Bold face parameters are covered by production test and quaranteed over operating temperatiure range.*

ABSOLUTE MAXIMUM RATINGS

Power Supply . . . . . 26 volts
Power Dissipation (Package Limitation)
Plastic Package 625mW
Derate above 25°C . . . . . 5mW/°C
SOIC Package 500mW
Derate above 25°C . . . . . 4mW/°C
Temperature
Storage . . . . . –65°C to +150°C

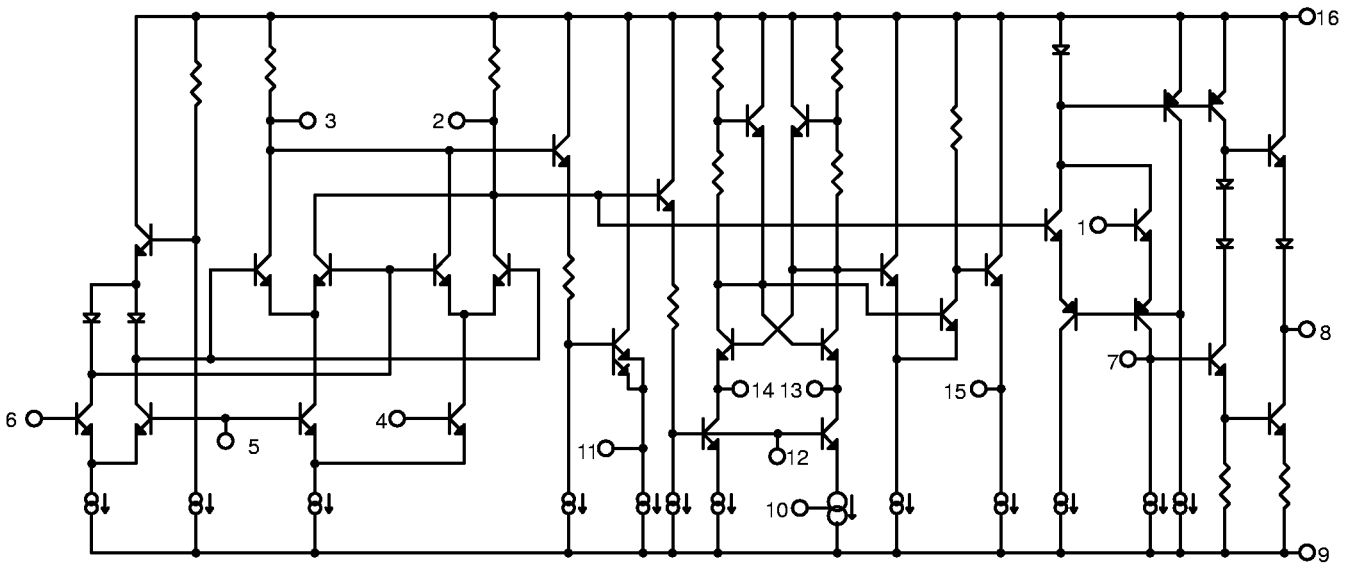


Figure 2. Equivalent Schematic Diagram

SYSTEM DESCRIPTION

The XR–215 monolithic PLL system consists of a balanced phase comparator, a highly stable voltage–controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the noninverting input of the operational amplifier. A self–contained PLL System is formed by simply AC coupling the VCO output to either of the phase comparator inputs and adding a low–pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on–off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single external capacitor. The operational amplifier can be used for audio preamplification in FM detector applications or as a high speed sense amplifier (or comparator) in FSK demodulation.

DESCRIPTION OF CIRCUIT CONTROLS

Phase Comparator Inputs (Pins 4 and 6)

One input to the phase comparator is used as the signal input. The remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see *Figure 3.*) For split supply operation, these inputs are biased from ground as shown in *Figure 4.* For single supply operation, a resistive bias string similar to that shown in *Figure 3.* should be used to set the bias level at approximately $V_{CC}/2$. The dc bias current at these terminals is nominally 8μA.

Phase Comparator Bias (Pin 5)

This terminal should be dc biased as shown in *Figure 3.* and 4, and ac grounded with a bypass capacitor.

Phase Comparator Outputs (Pins 2 and 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase comparator inputs (pins 4 and 6). The phase comparator outputs are internally connected to the VCO control terminals (see *Figure 2.*) One of the outputs (pin 3) is internally connected to the noninverting input of the operational amplifier. The low–pass filter is achieved by connecting an RC network to the phase comparator outputs as shown in *Figure 15.*

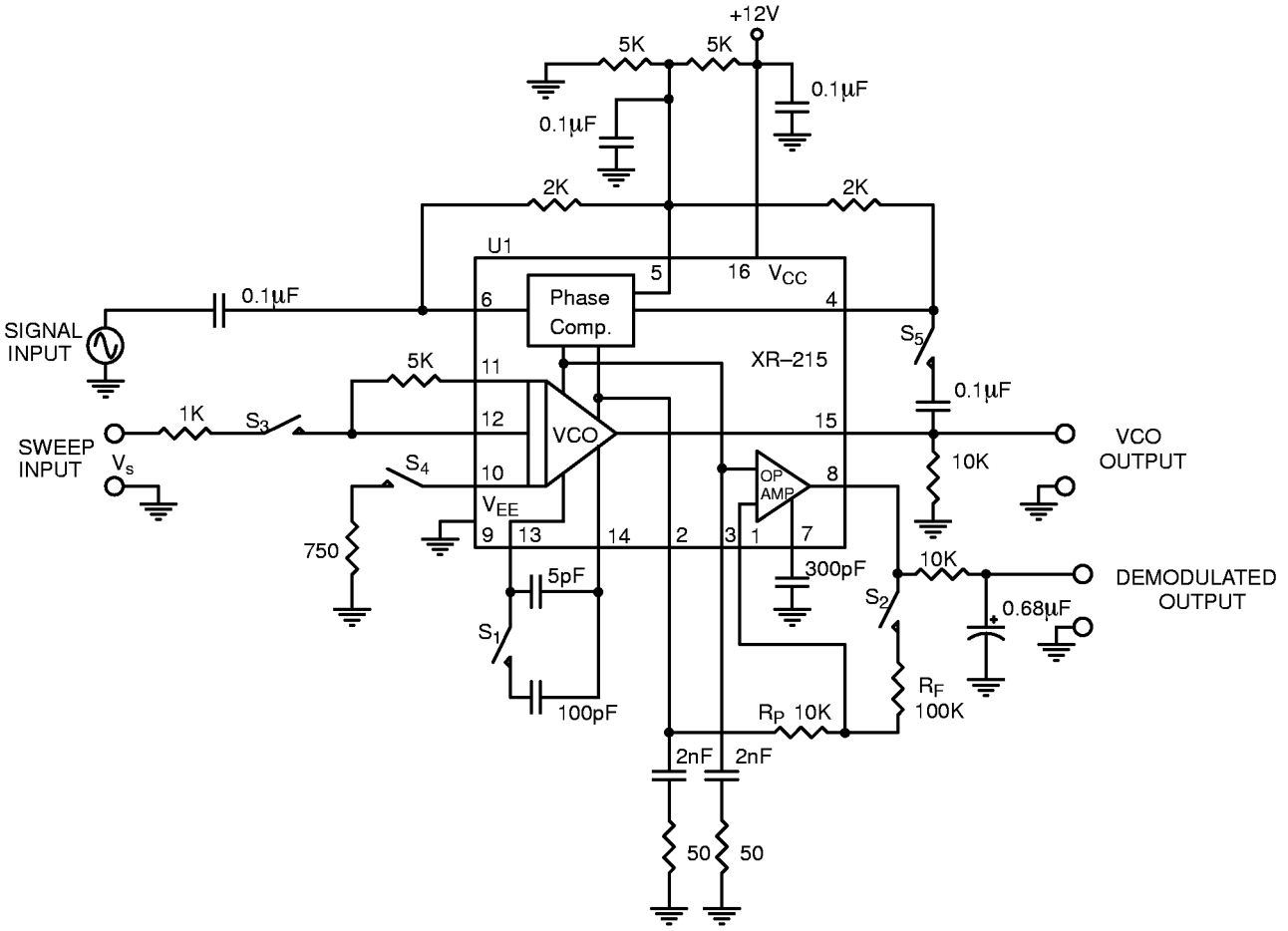


Figure 3. Test Circuit for Single Supply Operation

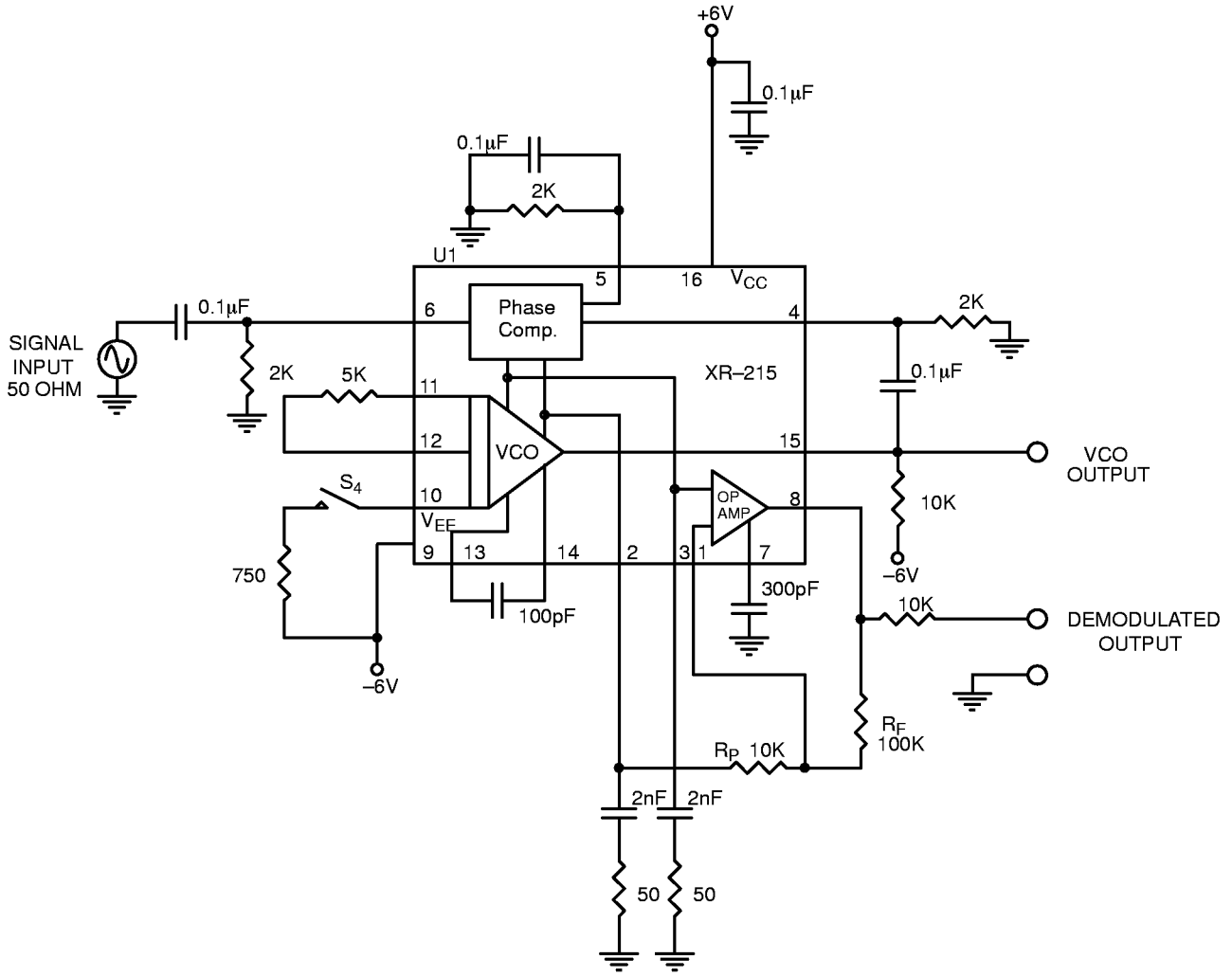


Figure 4. Test Circuit for Split–Supply Operation

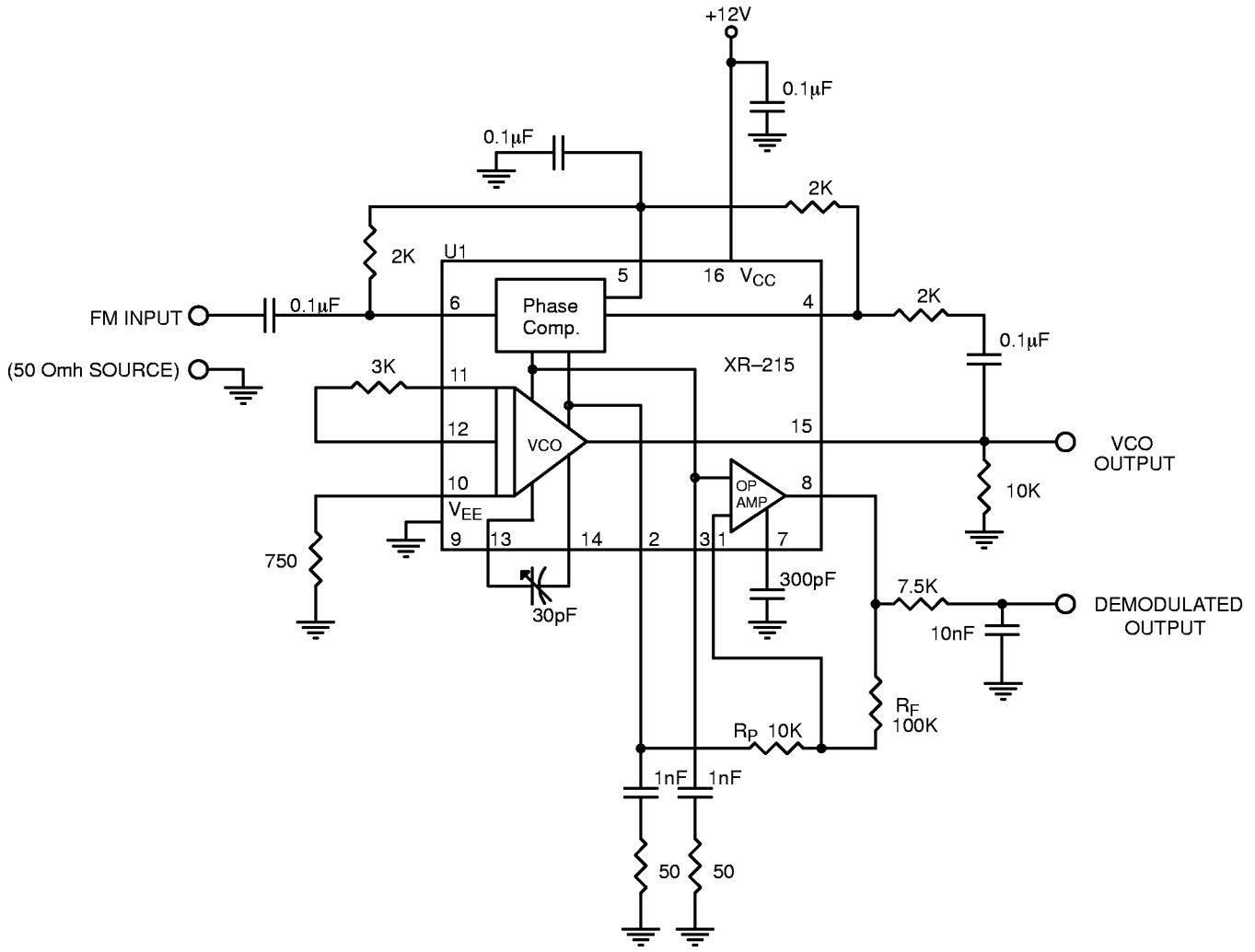


Figure 5. Test Circuit for FM Demodulation

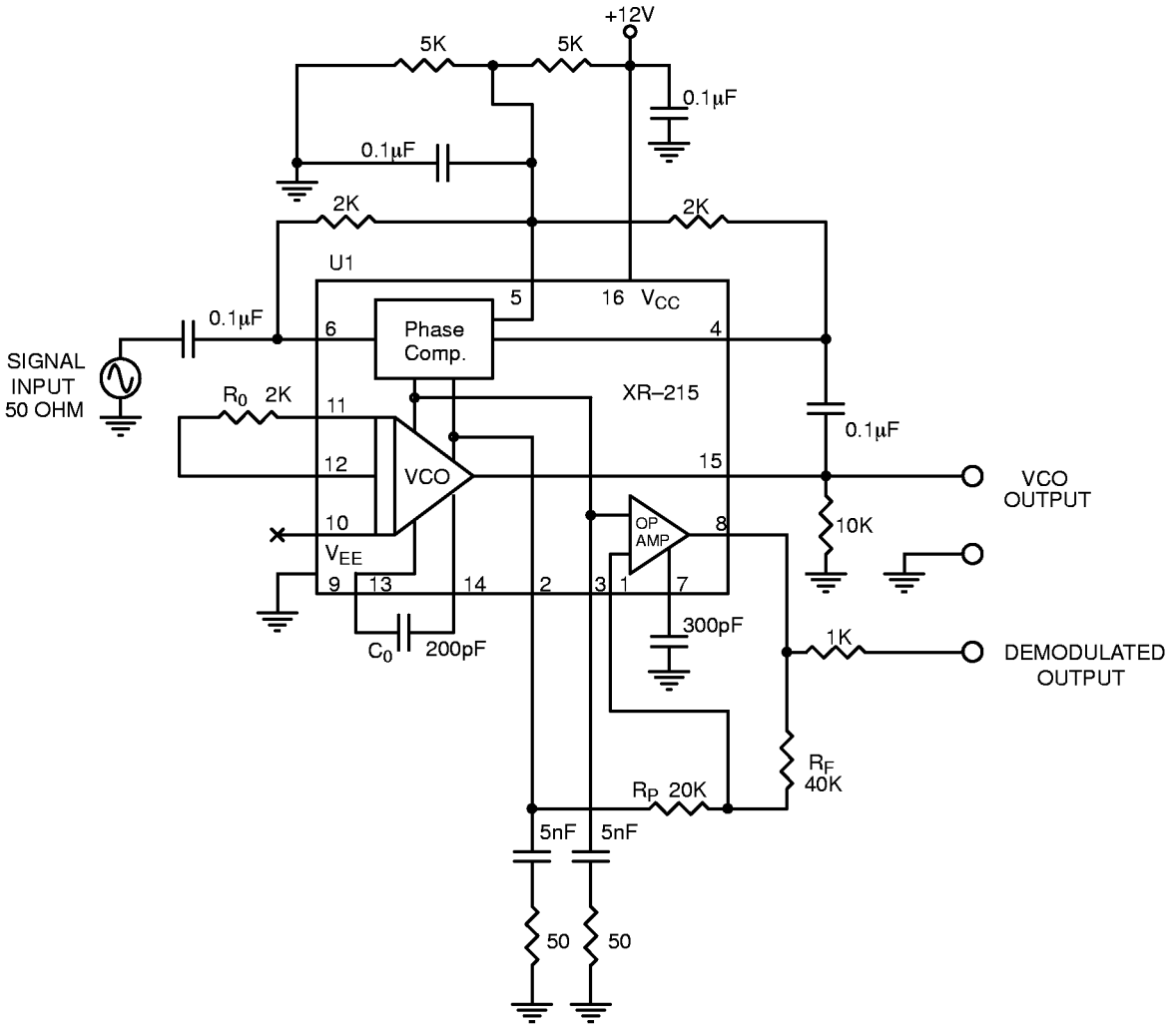


Figure 6. Test Circuit For Tracking Filter

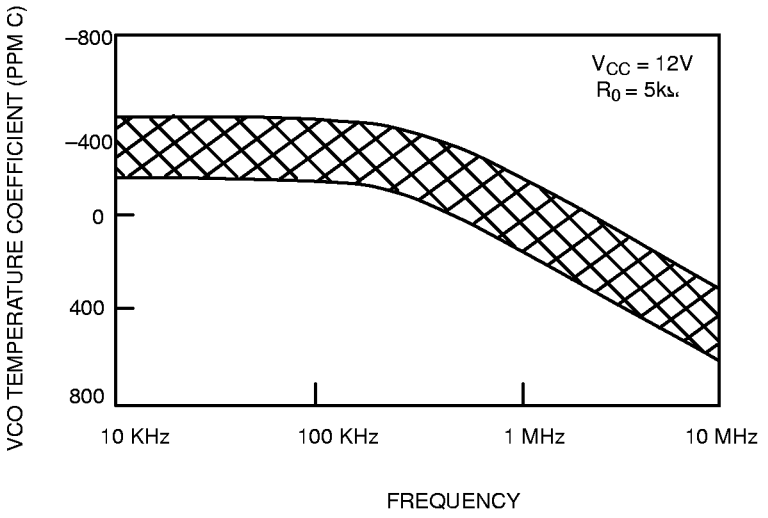


Figure 7. Typical VCO Temperature Coefficient Range as a Function of Operating Frequency (Pin 10 open)

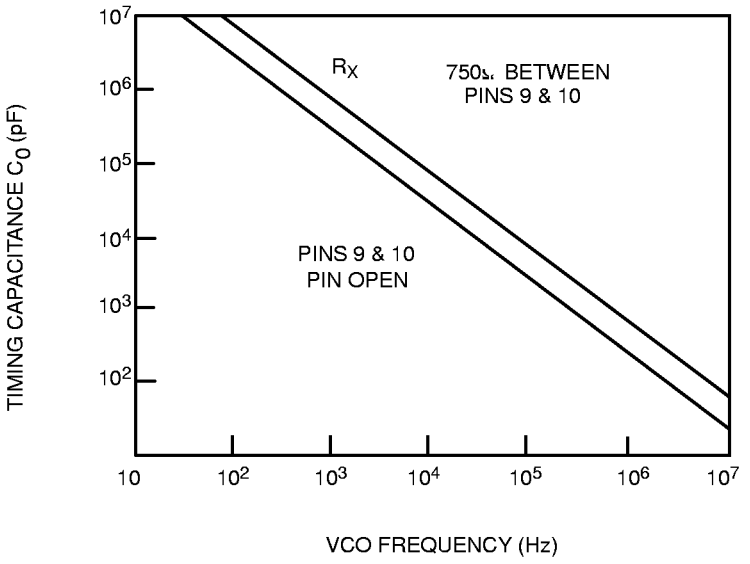


Figure 8. VCO Free Running Frequency vs. Timing Capacitor

VCO Timing Capacitor (Pins 13 and 14)

The VCO free–running frequency, f0, is inversely proportional to timing capacitor C_0 connected between pins 13 and 14. (See *Figure 8*.)

VCO Output (Pin 15)

The VCO produces approximately a 2.5Vp–p output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 9 through a 10kΩ resistor to increase the output current drive capability. For high voltage operation (V_{CC} > 20V), a 20kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output for short circuit protection.

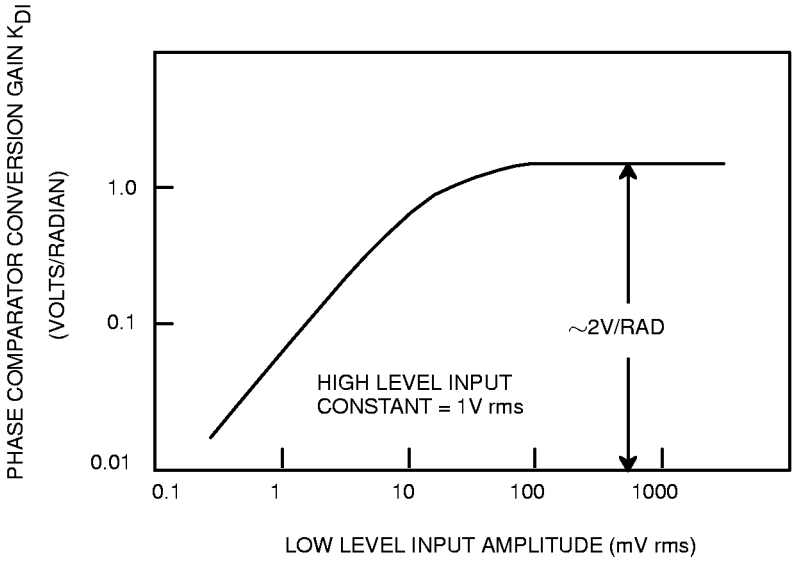


Figure 9. Phase Comparator Conversion Gain, K_d, versus Input Amplitude

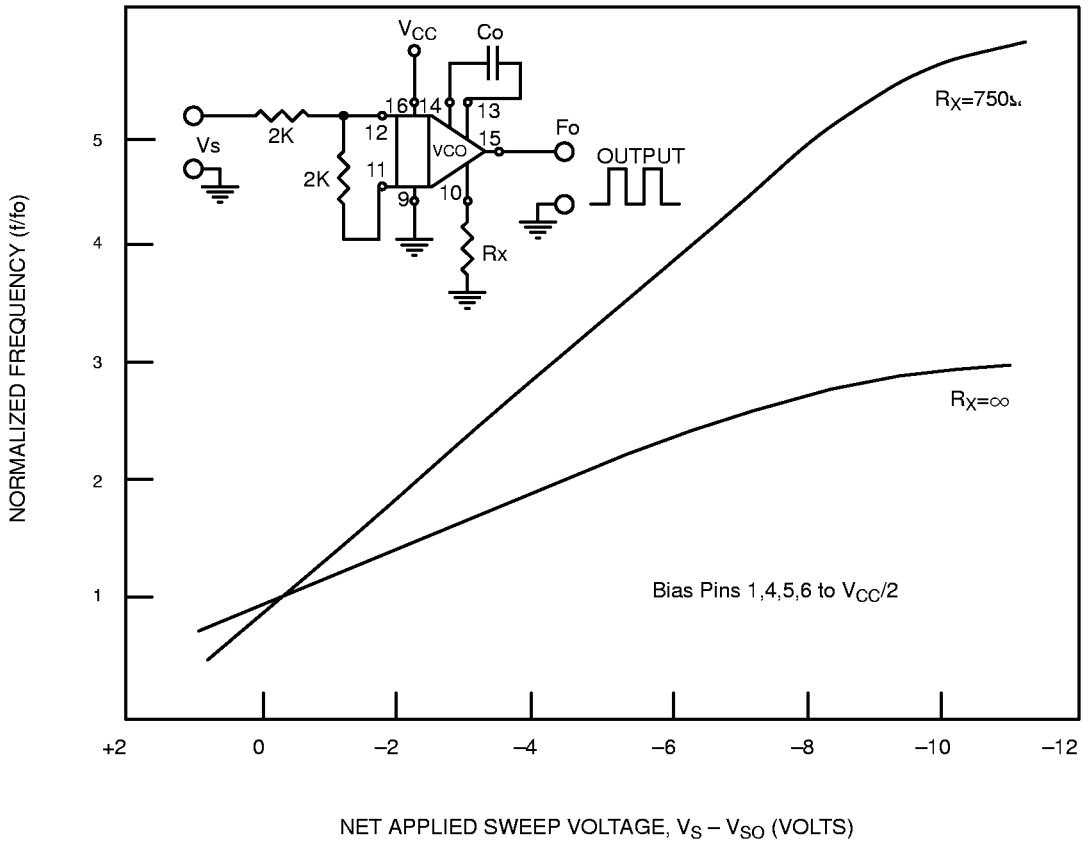


Figure 10. Typical Frequency Sweep Characteristics as a Funciton of Applied Sweep Voltage

Note: *$V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12*

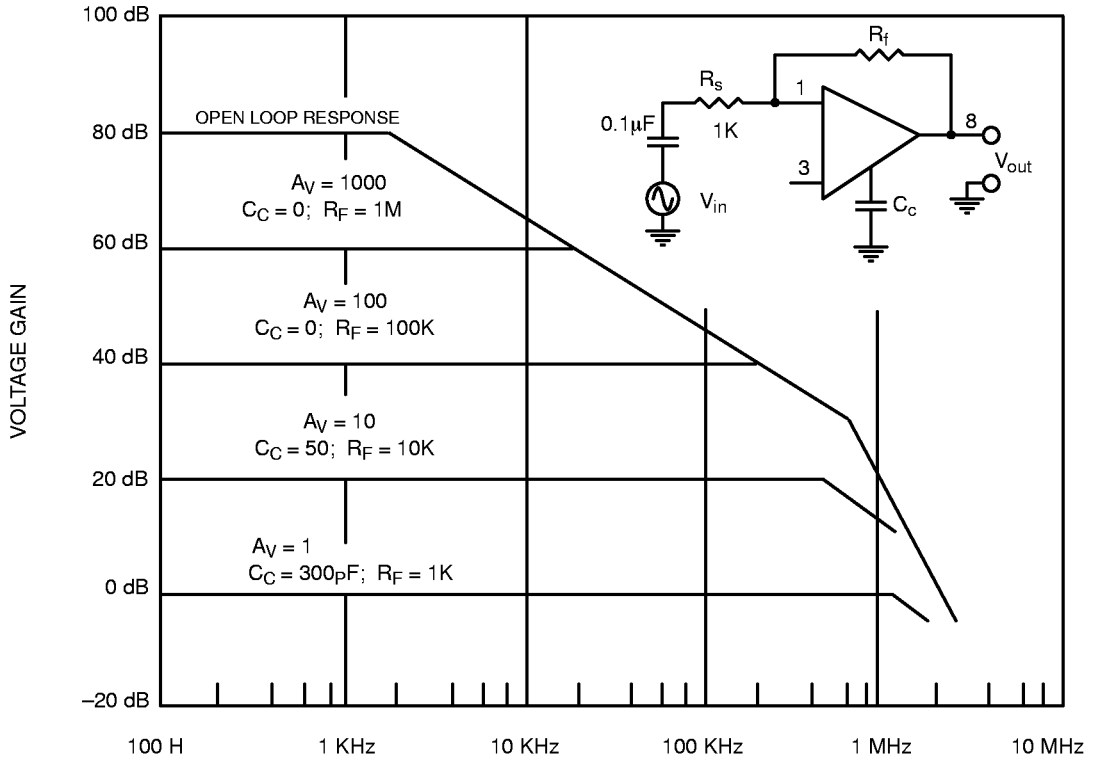


Figure 11. XR–215 Op Amp Frequency Response

VCO Sweep Input (Pin 12)

The VCO Frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see *Figure 10.*) The impedance looking into the sweep input is approximately 50kΩ. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in *Figure 10.* The VCO temperature dependence is minimum when the sweep input is not used.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5mA or less under all operating conditions.

ON–OFF KEYING: With pin 10 open circuited, the VCO can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 2 kΩ, oscillations will stop if the applied potential at pin 12 is raised 3 volts above its open–circuit value. When sweep, sync, or on–off keying functions are not used, R_S should be left open circuited.

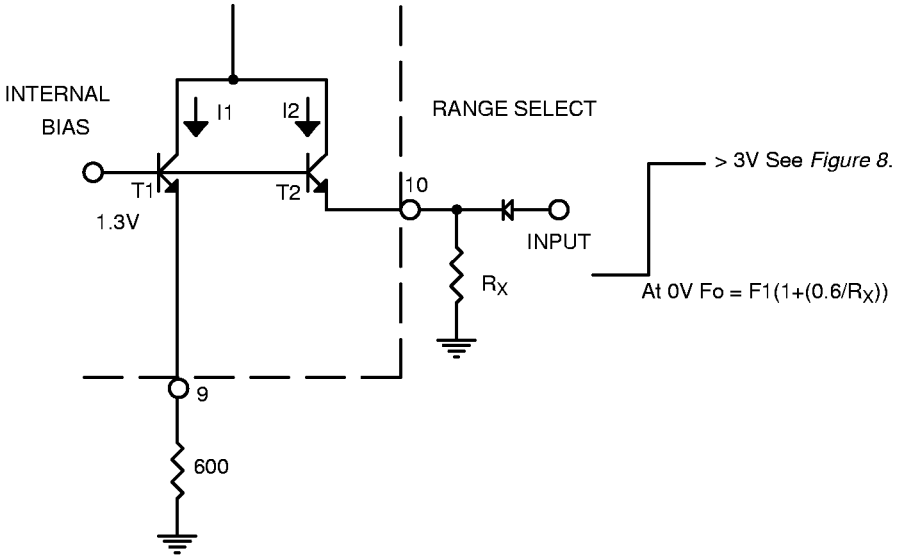


Figure 12. Explanation of VCO Range–Select Controls

Range–Select (Pin 10)

The frequency range of the XR–215 can be extended by connecting an external resistor, R_X, between pins 9 and 10. With reference to *Figure 12.*, the operation of the range–select terminal can be explained as follows: The VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I1 is set internally, whereas I_2 is set by the external resistor R_X. Thus, at any C_0 setting, the VCO frequency can be expressed as:

$$f_0 = f_1 \left(1 + \frac{0.6}{R_x} \right)$$

where f1 is the frequency with pin 10 open circuited and R_X is in kΩ. External resistor R_X (≈750Ω) is recommended for operation at frequencies in excess of 5MHz.

The range select terminal can also be used for fine tuning the VCO frequency, by varying the value of R_X. Similarly, the VCO frequency can be changed in discrete steps by switching in different values of R_X between pins 9 and 10.

Digital Programming

Using the range select control, the VCO frequency can be stepped in a binary manner, by applying a logic signal to pin 10, as shown in *Figure 12.* For high level logic inputs, transistor T2 is turned off, and R_X is effectively switched out of the circuit. Using the digital programming capability, the XR–215 can be time–multiplexed between two separate input frequencies, as shown in *Figure 19.* and *Figure 20.*

Amplifier Input (Pin 1)

This pin provides the inverting input for the operational amplifier section. Normally it is connected to pin 2 through a 10 kΩ external resistor (see *Figure 3.* or *Figure 4.*)

Amplifier Output (Pin 8)

This pin is used as the output terminal for FM or FSK demodulation. The amplifier gain is determined by the external feedback resistor, R_F, connected between pins 1 and 8. Frequency response characteristics of the amplifier section are shown in *Figure 11.*

Amplifier Compensation (Pin 7)

The operational amplifier can be compensated by a single 300 pF capacitor from pin 7 to ground. (See *Figure 11.*)

BASIC PHASE–LOCKED LOOP OPERATION

Principle of Operation

The phase–locked loop (PLL) is a unique and versatile circuit technique which provides frequency selective tuning and filtering without the need for coils or inductors. As shown in *Figure 13.*, the PLL is a feedback system comprised of three basic functional blocks: phase comparator, low–pass filter and voltage–controlled oscillator (VCO). The basic principle of operation of a PLL can be briefly explained as follows: with no input signal applied to the system, the error voltage V_d, is equal to zero. The VCO operates at a set frequency, f_0, which is known as the "free–running" frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, fs, is sufficiently close to f_0, the feedback nature of the PLL causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

A Linearized Model for PLL

When the PLL is in lock, it can be approximated by the linear feedback system shown in *Figure 14.* $\oslash_s$ and $\oslash_o$ are the respective phase angles associated with the input signal and the VCO output, F(s) is the low–pass filter response in frequency domain, and K_d and K_o are the conversion gains associated with the phase comparator and VCO sections of the PLL.

DEFINITION OF XR–215 PARAMETERS FOR PLL APPLICATIONS

VCO Free–Running Frequency, f_o

The VCO frequency with no input signal. It is determined by selection of C_0 across pins 13 and 14 and can be increased by connecting an external resistor R_X between pins 9 and 10. It can be approximated as:

$$f_0 \approx \frac{220}{C_0}\left(1 + \frac{0.6}{R_X}\right)$$

where C_0 is in µF and R_X is in kΩ. (See *Figure 8.*)

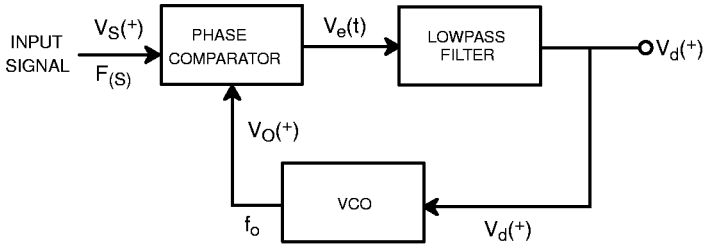


Figure 13. Block Diagram of a Phase–Locked Loop

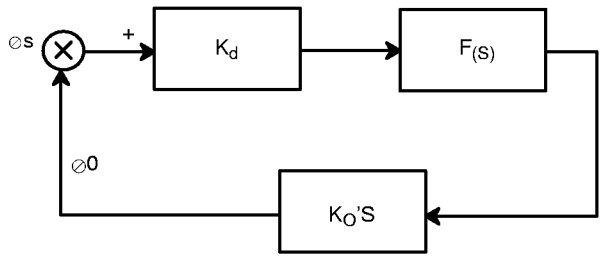


Figure 14. Linearized Model of a PLL as a Negative Feedback System

Phase Comparator Gain K_d

The output voltage from the phase comparator per radian of phase difference at the phase comparator inputs (pins 4 and 6). The units are volts/radians.

VCO Conversion Gain Ko

The VCO vollage–to–frequency conversion gain is determined by the choice of timing capacitor C_0 and gain control resistor, R_0 connected externally across pins 11 and 12. It can be expressed as:

$$K_0 \approx \frac{700}{C_0 R_0} \text{ (radians/sec/volt)}$$

where C_0 is in µF and R0 is in kΩ. For most applications, recommended values for R_0 range from 1kΩ to 10kΩ.

ABSOLUTE MAXIMUM RATINGS

Lock Range (Δ wL)

The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the "tracking" or "holding" range. If saturation or limiting does not occur, the lock range is equal to the loop gain, i.e. $\Delta\omega_L = K_T = K_d K_o$.

Capture Range (Δ wC)

The band of frequencies in the vicinity of fo where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. It is always smaller than the lock range and is related to the low–pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L \, |F(j\Delta\omega_C|$$

where $|F(j\Delta\omega_C|$ is the low–pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_c \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

where T_1 is the filter time constant.

Amplifier Gain AV

The voltage gain of the amplifier section is determined by feedback resistors R_F and Rp between pins (8,1) and 2,1) respectively. (See *Figure 3.* and *Figure 4.*). It is given by:

$$A_V \approx \frac{-R_F}{R_1 + R_P}$$

where R_1 is the (6KΩ) internal impedance at pin 2, and R_p is the external resistor between pins 1 and 2.

Low–Pass Filter

The low–pass filter section is formed by connecting an external capacitor or RC network across terminals 2 and 3. The low–pass filter components can be connected either between pins 2 and 3 or, from each pin to ground. Typical filter configurations and corresponding filter transfer functions are shown in *Figure 15.* where R_{INT} (6kΩ) is the internal impedance at pins 2 and 3. It should be noted that the rejection of the low pass filter decreases above 2MHz when the capacitor is tied from Pin 2 to 3.

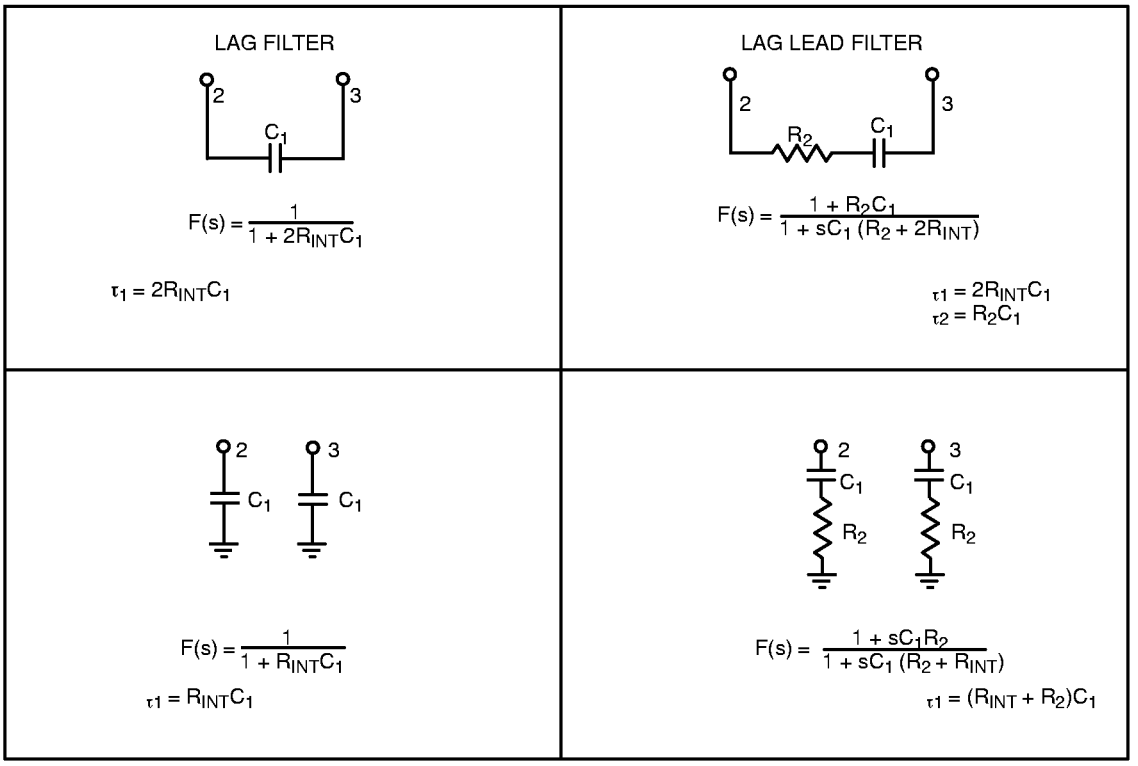


Figure 15.

APPLICATIONS INFORMATION

FM Demodulation

Figure 16. shows the external circuit connections to the XR–215 for frequency–selective FM demodulation. The choice of C_0 is determined by the FM carrier frequency (see *Figure 8.*) The low–pass filter capacitor C_1 is determined by the selectivity requirements. For carrier frequencies of 1 to 10MHz, C_1 is in the range of 10 C_0 to 30 C_0. The feedback resistor R_F can be used as a "volume–control" adjustment to set the amplitude of the demodulated output. The demodulated output amplitude is proportional to the FM deviation and to resistors R_0 and R_F For ±1% FM deviation it can be approximated as:

$$V_{OUT} \approx R_0 R_F \left(1 + \frac{0.6}{R_X}\right) mV, \ rms$$

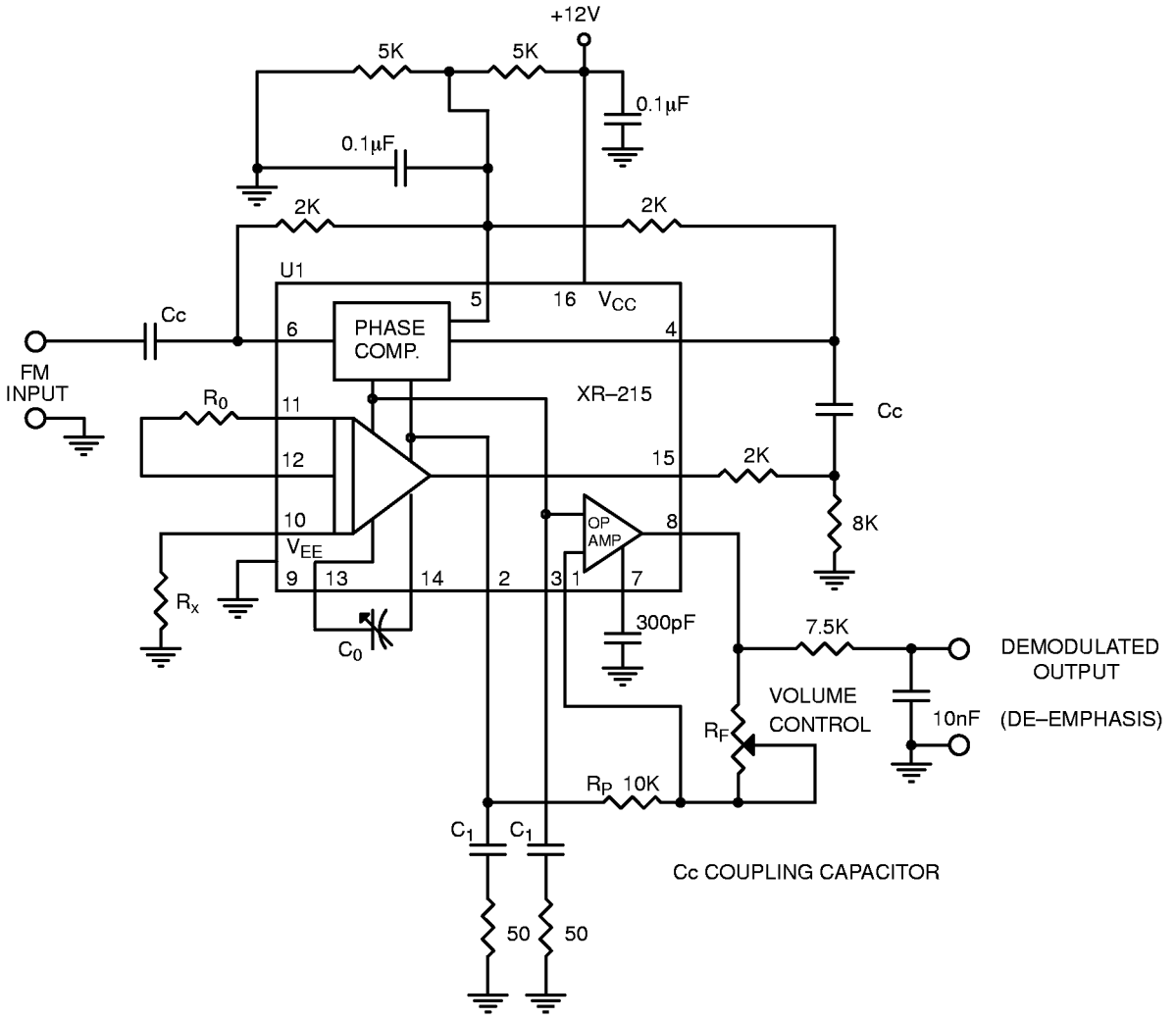


Figure 16. Circuit Connection for FM Demodulation

The damping factor can be calculated by using:

$$\zeta = 1/2\left(\frac{K_0 K_d}{\tau_1}\right)^{1/2} \cdot \tau_2 + \left(\frac{1}{K_0 K_d}\right)$$

where all resistors are in kΩ and R_X is the range extension resistor connected across pins 9 and 10. For circuit operation below 5MHz, R_X can be open circuited. For operation above 5MHz, $R_X \approx 750\Omega$ is recommended.

Typical output signal/noise ratio and harmonic distortion are shown in *Figure 17.* and *Figure 18.* as a function of FM deviation, for the component values shown in Figure 5.

Multi–Channel Demodulation

The ac digital programming capability of the XR–215 allows a single circuit be time–shared or multiplexed between two information channels, and thereby selectively demodulate two separate carrier frequencies. *Figure 19.* shows a practical circuit configuration for time– multiplexing the XR–215 between two FM channels, at 1MHz and 1.1MHz respectively. The channel–select logic signal is applied to pin 10, as shown in *Figure 19.* with both input channels simultaneously present at the PLL input (pin 4). *Figure 20.* shows the demodulated output as a function of the channel–select pulse where the two inputs have sinusoidal and triangular FM modulation respectively.

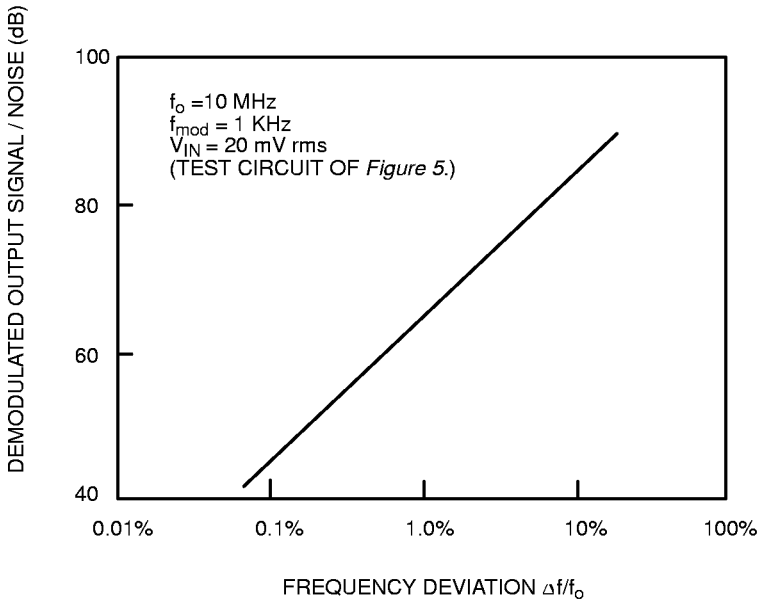


Figure 17. Output Signal/Noise Ratio as a Funciton of FM Deviation

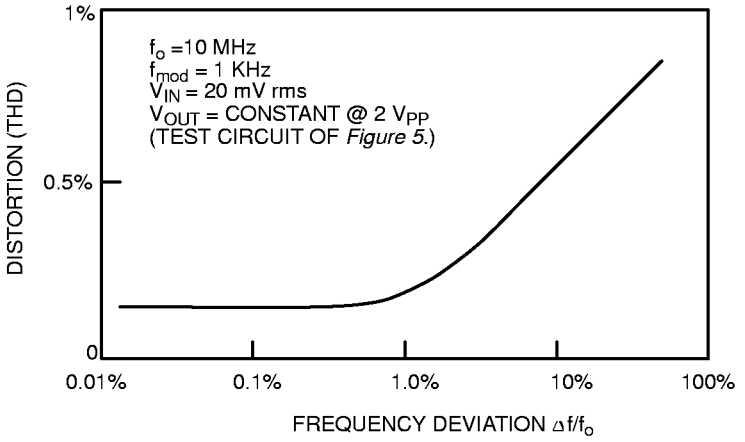


Figure 18. Output Distortion as a Function of FM Deviation

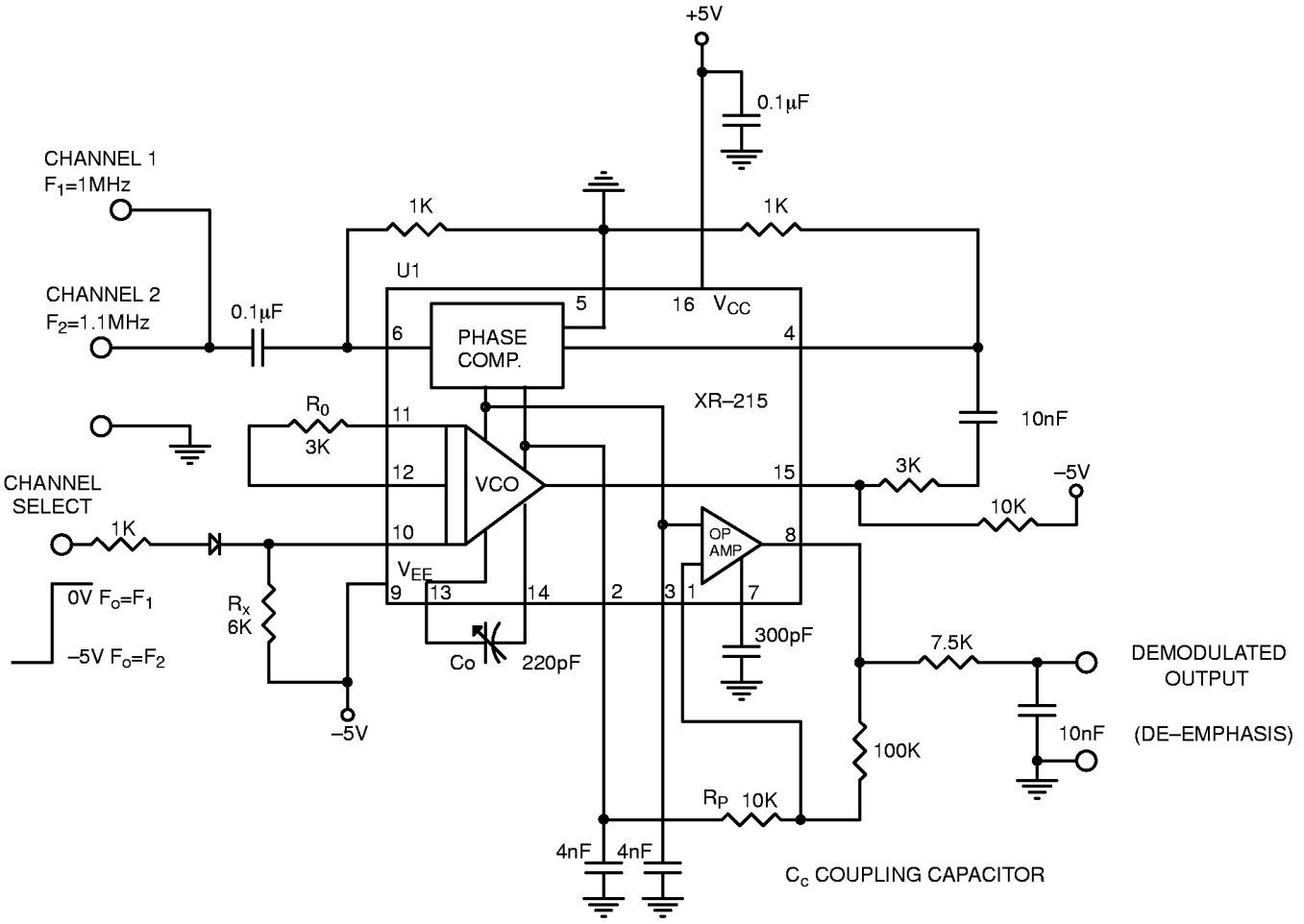


Figure 19. Time–Multiplexing XR–215 Between Two Simultaneous FM Channels

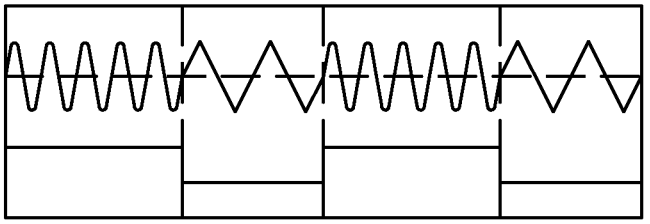


Figure 20. Demodulated Output Waveforms for Time–Multiplexed Operation

FSK Demodulation

Figure 21. contains a typical circuit connection for FSK demodulation. When the input frequency is shifted, corresponding to a data bit, the dc voltage at the phase comparator outputs (pins 2 and 3) also reverses polarity. The operational amplifier section is connected as a comparator, and converts the dc level shift to a binary output pulse. One of the phase comparator outputs (pin 3) is ac grounded and serves as the bias reference for the operational amplifier section. Capacitor C_1 serves as the PLL loop filter, and C_2 and C_3 as post–detection filters. Range select resistor, R_X, can be used as a fine– tune adjustment to set the VCO frequency.

Typical component values for 300 baud and 1200 baud operation are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070Hz	R_0 = 5kΩ, C_0 = 0.17μF
f_2 = 1270Hz	$C_1 = C_2$ = 0.047μF,
	C_3 = 0.033μF
High Band: f_1 = 2025Hz	R_0 = 8kΩ, C_0 = 0.1μF
f_2 = 2225Hz	$C_1 = C_2 = C_3$ = 0.033μF
1200 Baud	R_0 = 2kΩ, C_0 = 0.12μF
f_1 = 1200Hz	$C_1 = C_3$ = 0.003μF
f_2 = 2200Hz	C_2 = 0.01μF

Note: *For 300 Baud operation the circuit can be time–multiplexed between high and low bands by switching the external resistor R_X in and out of the circuit with a control signal, as shown in Figure 12.*

FSK Generation

The digital programming capability of the XR–215 can be used for FSK generation. A typical circuit connection for this application is shown in *Figure 22.* The VCO frequency can be shifted between the mark (f_2) and space (f_1) frequencies by applying a logic pulse to pin 10. The circuit can provide two separate FSK outputs: a low level (2.5 Vp–p) output at pin 15 or a high amplitude (10 Vp–p) output at pin 8. The output at each of these termihals is a symmetrical squarewave with a typical second harmonic content of less than 0.3%.

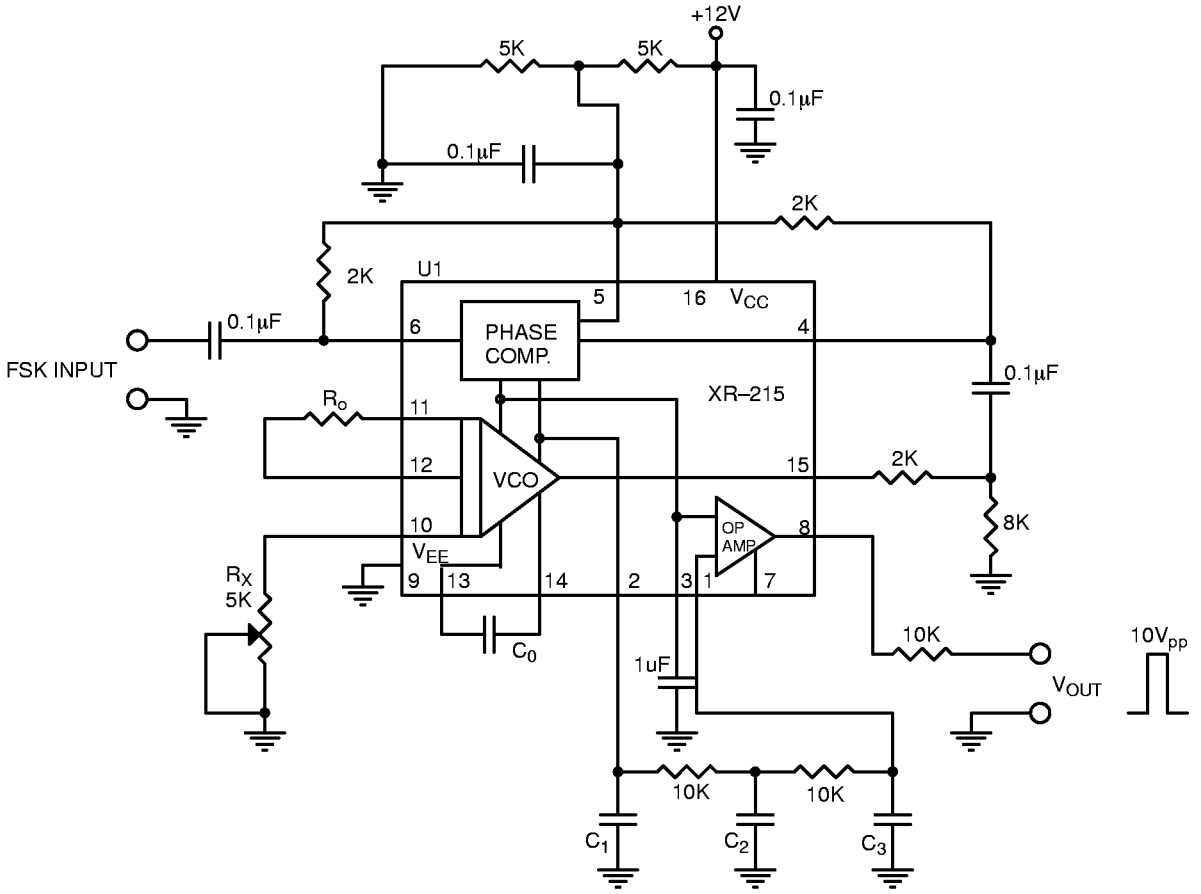


Figure 21. Circuit Connection for FSK Demodulation

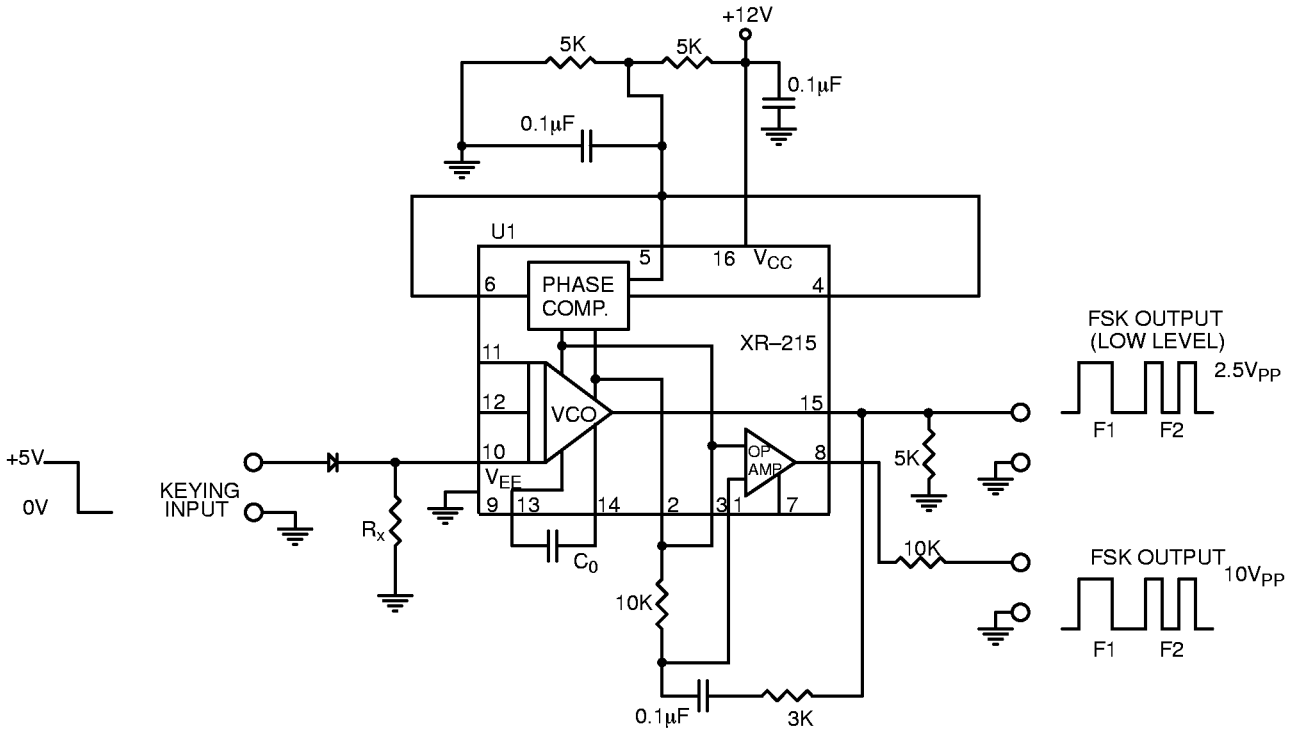


Figure 22. Circuit Connection For FSK Generation

Frequency Synthesis

In frequency synthesis applications, a programmable counter or divide–by–N circuit is connected between the VCO output (pin 15) and one of the phase detector inputs (pins 4 or 6), as shown in *Figure 23.* The principle of operation of the circuit can be briefly explained as follows: The counter divides down the oscillator frequency by the programmable divider modulus, N. Thus, when the entire system is phase–locked to an input signal at frequency, f_s, the oscillator output at pin 15 is at a frequency (Nf_s), where N is the divider modulus. By proper choice of the divider modulus, a large number of discrete frequencies can be synthesized from a given reference frequency. The low–pass filter capacitor C_1 is normally chosen to provide a cut–off frequency equal to 0.1% to 2% of the signal frequency, f_s.

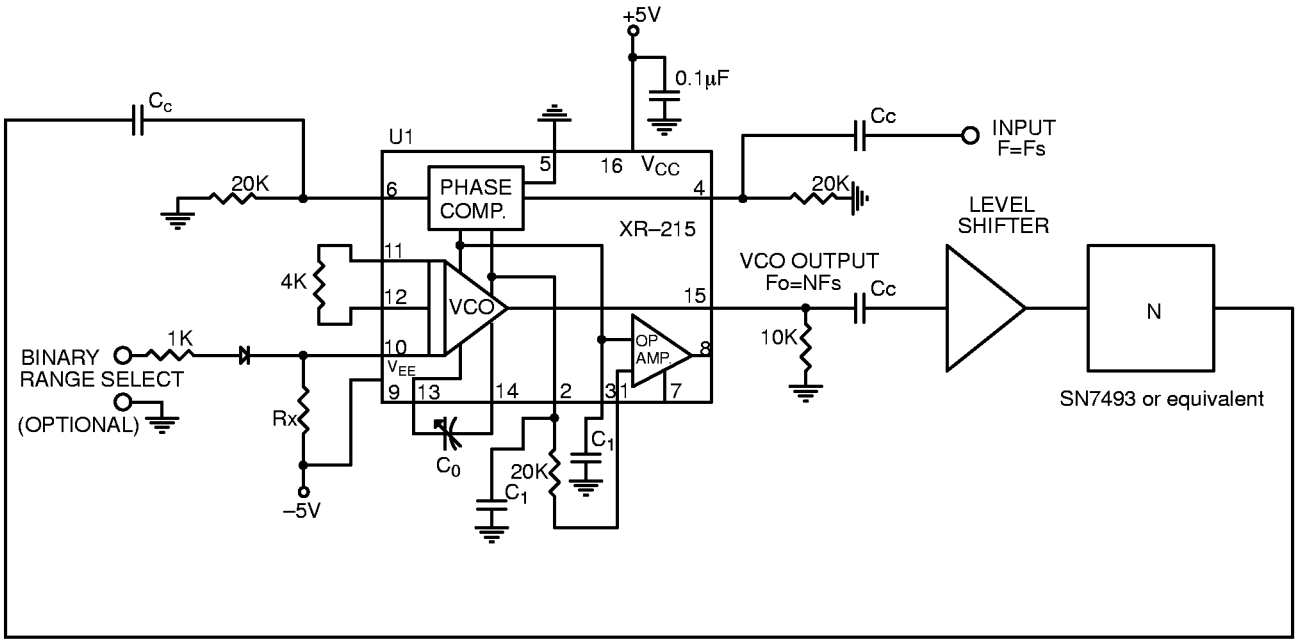


Figure 23. Circuit Connection For Frequency Synthesis

The circuit was designed to operate with commercially available monolithic programmable counter circuits using TTL logic, such as MC4016, SN5493 or equivalent. The digital or analog tuning characteristics of the VCO can be used to extend the available range of frequencies of the system, for a given setting of the timing capacitor C_0.

Typical input and output waveforms for N = 16 operation with f_s = 100kHz and f_o = 1.6MHz are shown in *Figure 24.*

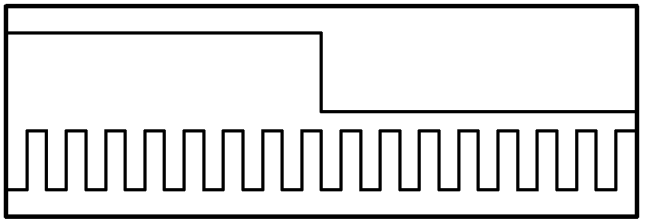


Figure 24. Typical Input/Output Waveforms for N=16
Top: Input (100kHz)
Bottom: VCO Output (1.6MHz)

Tracking Filter/Discriminator

The wide tracking range of the XR–215 allows the system to track an input signal over a 3:1 frequency range, centered about the VCO free running frequency. The tracking range is maximum when the binary range–select (pin 10) is open circuited. The circuit connections for this application are shown in *Figure 25.* Typical tracking range for a given input signal amplitude is shown in *Figure 26.* Recommended values of external components are: $1k\Omega < R_0 < 4k\Omega$ and $30\ C_0 < C_1 < 300\ C_0$ where the timing capacitor C_0 is determined by the center frequency requirements (see Figure 8).

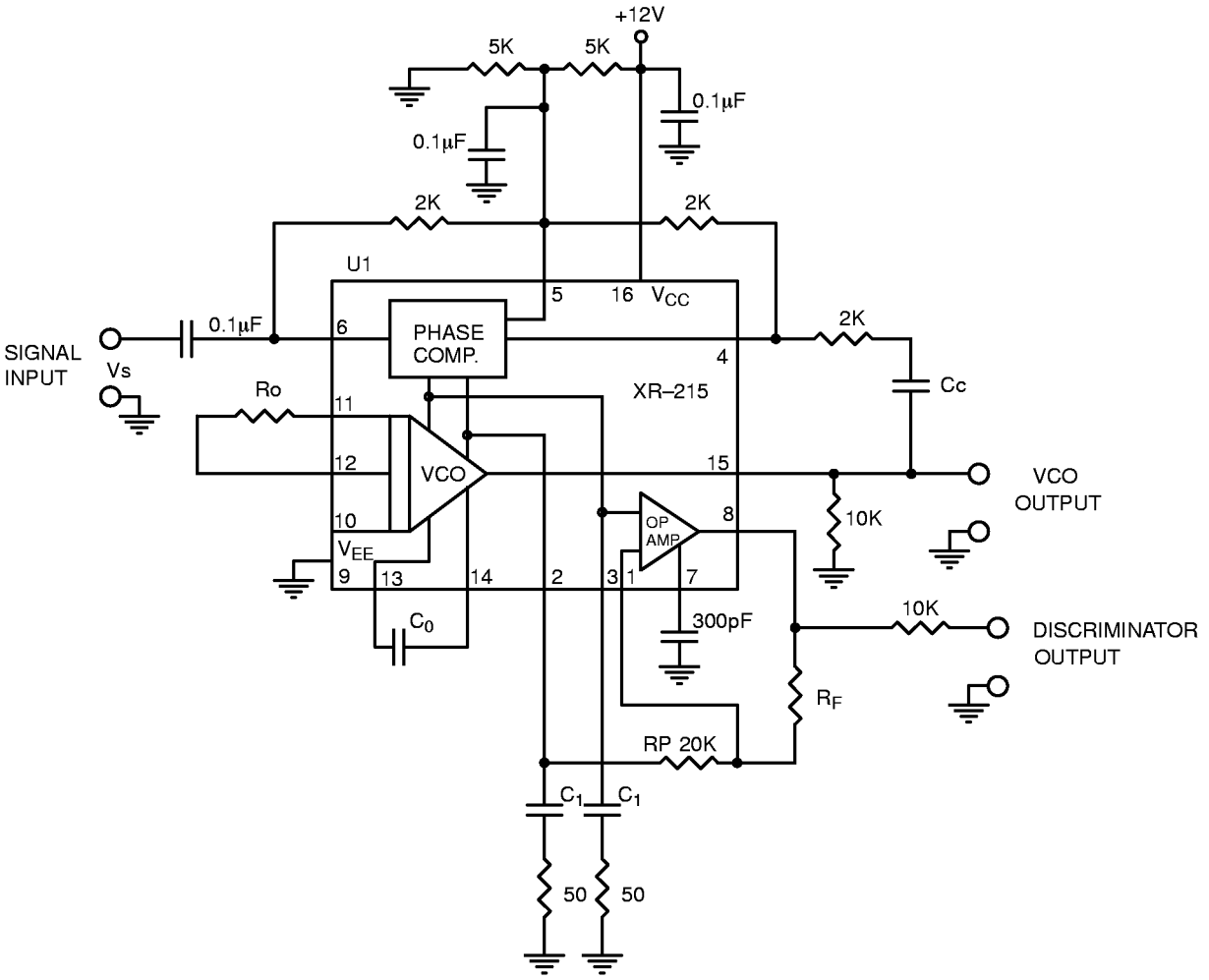


Figure 25. Circuit Connection For Tracking Filter Applications

The phase–comparator output voltage is a linear measure of the VCO frequency deviation from its free– running value. The amplifier section, therefore, can be used to provide a filtered and amplified version of the loop error voltage. In this case, the dc output level at pin 15 can be adjusted to be directly proportional to the difference between the VCO free–running frequency, fo, and the input signal, fs. The entire system can operate as a "linear discriminator" or analog "frequency–meter" over a 3:1 change of input frequency. The discriminator gain can be adjusted by proper choice of R_0 or R_F, for the test circuit of *Figure 25.*, the discriminator output is approximately (0.7 R_0R_F) mV per % of frequency deviation where R_0 and R_F are in kΩ. Output non–linearity is typically less than 1% for frequency deviations up to ±15%. *Figure 28.* shows the normalized output characteristics as a function of input frequency, with R_0 = 2kΩ and R_F = 36kΩ.

Crystal–Controlled PLL

The XR–215 can be operated as a crystal–controlled phase–locked loop by replacing the timing capacitor with a crystal. A circuit connection for this application is shown in *Figure 28.* Normally a small tuning capacitor (≈ 30 pF) is required in series with the crystal to set the crystal frequency. For this application the crystal should be operated in its fundamental mode. Typical pull–in range of the circuits is 11kHz at 10MHz. There is some distortion on the demodulated output.

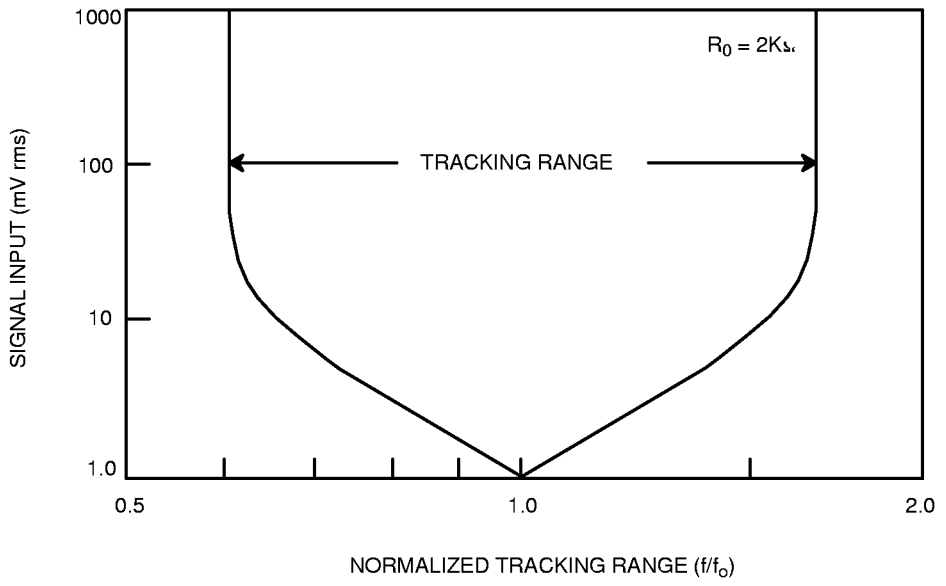


Figure 26. Tracking Range vs Input Amplitude (Pin 10 Open Circuited)

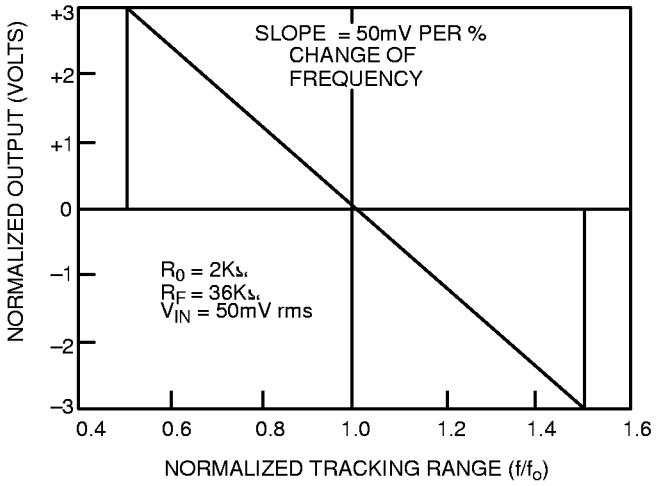


Figure 27. Typical Discriminator Output Characteristics for Tracking Filter Applications

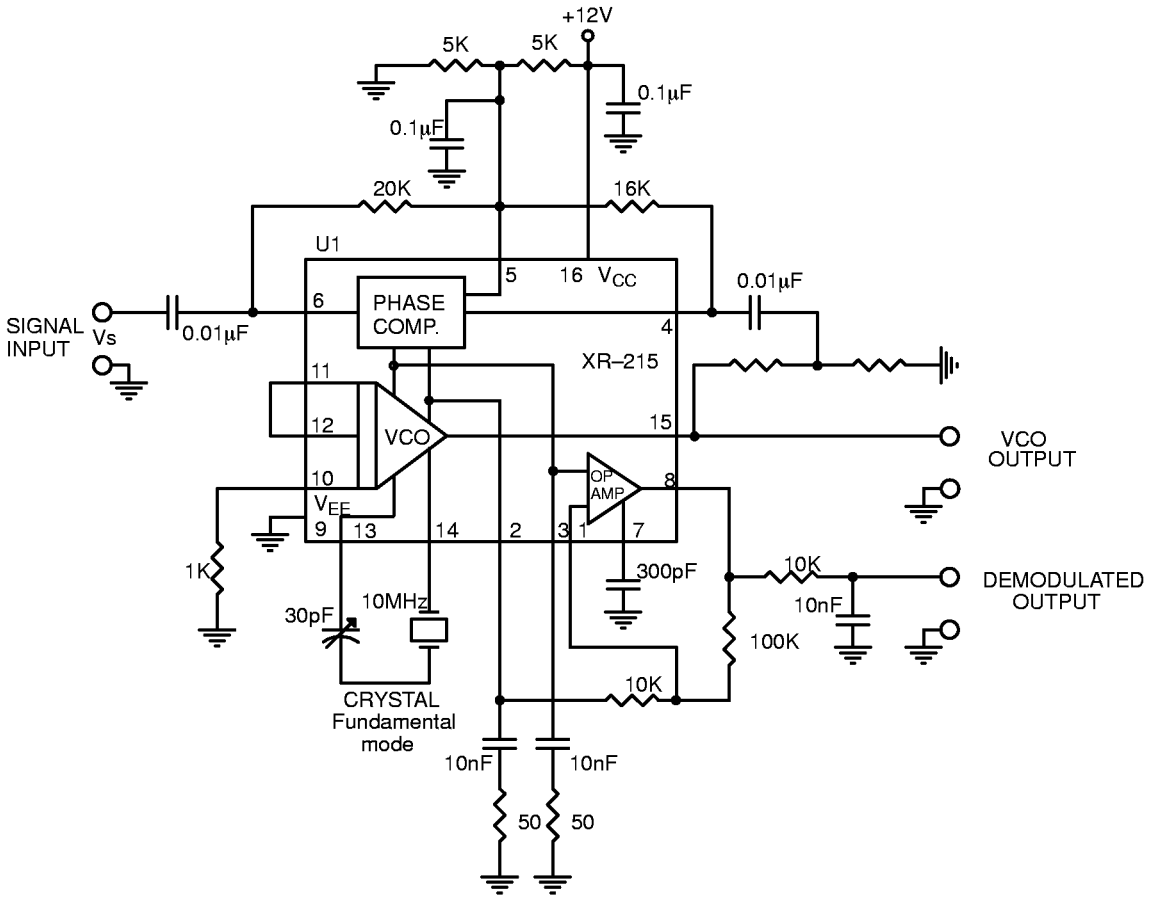
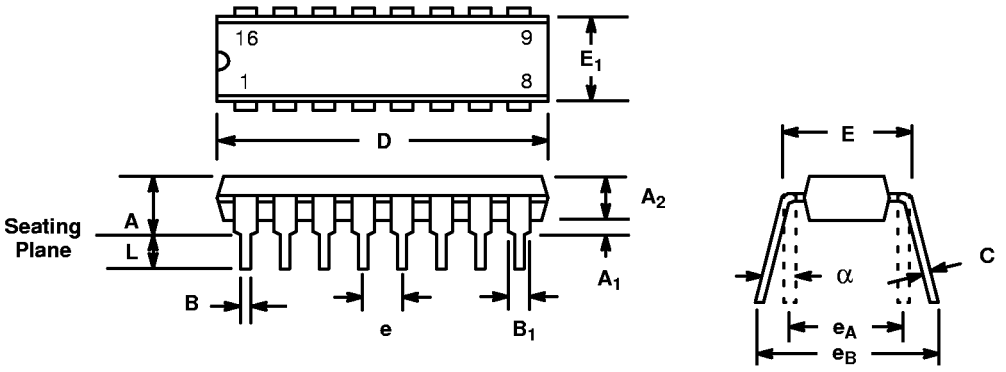


Figure 28. Typical Circuit Connection for Crystal–Controlled Clock Recovery.

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

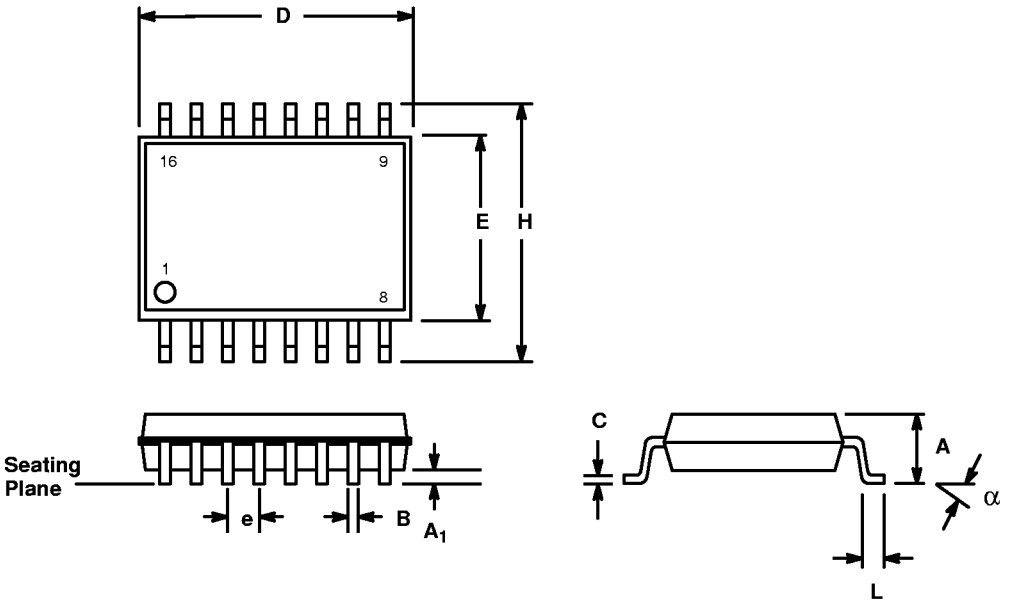


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column