DATA SHEET

PCF8549
65 × 102 pixels matrix LCD driver

Product specification
File under Integrated Circuits, IC12

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Philips
Semiconductors

PHILIPS

65 × 102 pixels matrix LCD driver PCF8549

FEATURES

- Single chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Generation of LCD supply voltage
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz Fast I²C Interface
- CMOS compatible inputs
- Mux rate: 65
- Logic supply voltage range $V_{DD1} - V_{SS}$: 1.5 to 6 V
- Voltage generator voltage range $V_{DD2/2\_HV} - V_{SS}$: 2.4 to 5 V
- Display supply voltage range $V_{LCD} - V_{SS}$: 7.0 to 16 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Interlacing for better display quality
- Slim chip layout, suited for chip-on-glass applications.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF8549 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8549 interfaces to most microcontrollers via an I²C interface.

Packages

The PCF8549U/2 is available as bumped die. Sawn wafer as chip sorted in chip tray. For further details see Section “Bonding pads”.

Customized TCP upon request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8549U/2/F1	TRAY	chip with bumps in tray	

BLOCK DIAGRAM

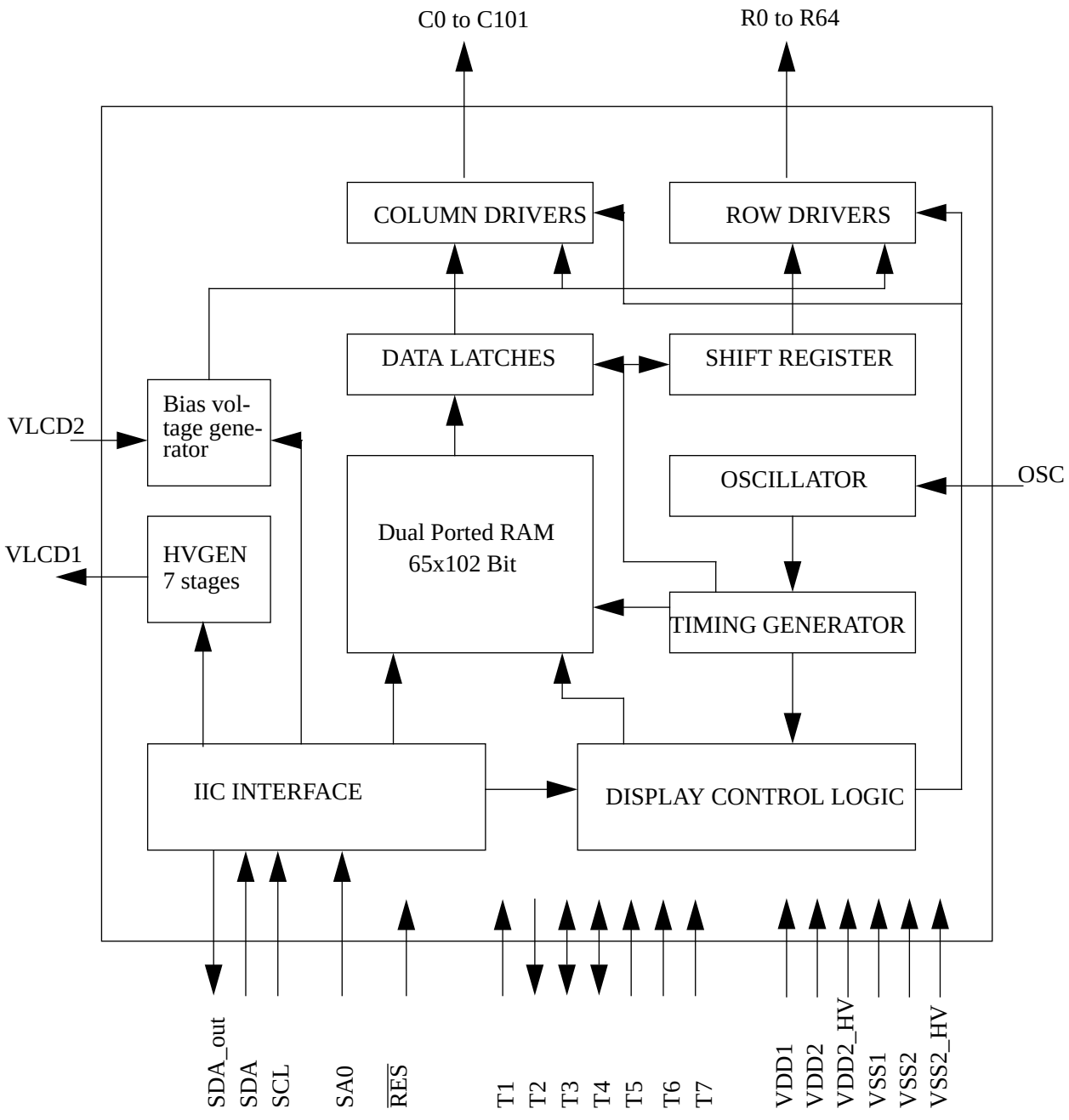


Fig.1 Block diagram.

PINNING

SYMBOL	DESCRIPTION
R0 to R64	LCD row driver outputs
C0 to C101	LCD column driver outputs
$V_{SS1,2,2\_HV}$	negative power supply
$V_{DD1,2,2\_HV}$	supply voltage
$V_{LCD1,2}$	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 I/O
T4	test 4 I/O
T5	test 5 input
T6	test 6 input
T7	test 7 input
SDA	I^2C data input
SCL	I^2C clock line
SDA_OUT	I^2C output
SA0	least significant bit of slave address
OSC	oscillator
$\overline{RES}$	external reset input, low active

Pin functions

R0 TO R64: ROW DRIVER OUTPUTS

These pads output the row signals.

C0 TO C101: COLUMN DRIVER OUTPUTS

These pads output the column signals.

$V_{SS1,2,2\_HV}$: NEGATIVE POWER SUPPLY RAILS

Negative power supplies.

$V_{DD1,2,2\_HV}$: POSITIVE POWER SUPPLY RAILS

V_{DD2} and V_{DD2_HV} are the supply voltages for the internal voltage generator. Both have to be on the same voltage and may be connected together outside of the chip. If the internal voltage generator is not used, they should be both connected to ground. V_{DD1} is used as power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD2_HV}.

$V_{LCD1,2}$: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCD1} and V_{LCD2} must be connected together. An external LCD supply voltage can be supplied using the V pad. In this case, V_{LCD1} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8549 is in power-down mode, the external LCD supply voltage has to be switched off.

T1, T2, T3, T4, T5, T6 AND T7: TEST PADS

T1, T3, T4, T5, T6 and T7 must be connected to V_{SS1}, T2 is to be left open. Not accessible to user.

SDA/SDA_OUT: I²C DATA LINES

Output and input are separated. If both pads are connected together they behave like a standard I²C pad.

SCL: I²C CLOCK SIGNAL

Input for the I²C-bus clock signal.

SA0: SLAVE ADDRESS

With the SA0 pin two different slave addresses can be selected. That allows to connect two PCF8549 LCD drivers to the same I²C-bus.

OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

$\overline{RES}$: RESET

This signal will reset the device. Signal is active low.

FUNCTIONAL DESCRIPTION

Block diagram functions

OSCILLATOR

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

I²C INTERFACE

The I²C interface receives and executes the commands sent via the I²C-bus. It also receives RAM-data and sends them to the RAM. During read access the 8-bit parallel data or the status register content is converted to a serial data stream and output via the I²C-bus.

DISPLAY CONTROL LOGIC

The display control logic generates the control signals to read out the RAM via the 101 bit parallel port. It also generates the control signals for the row, and column drivers.

DISPLAY DATA RAM (DDRAM)

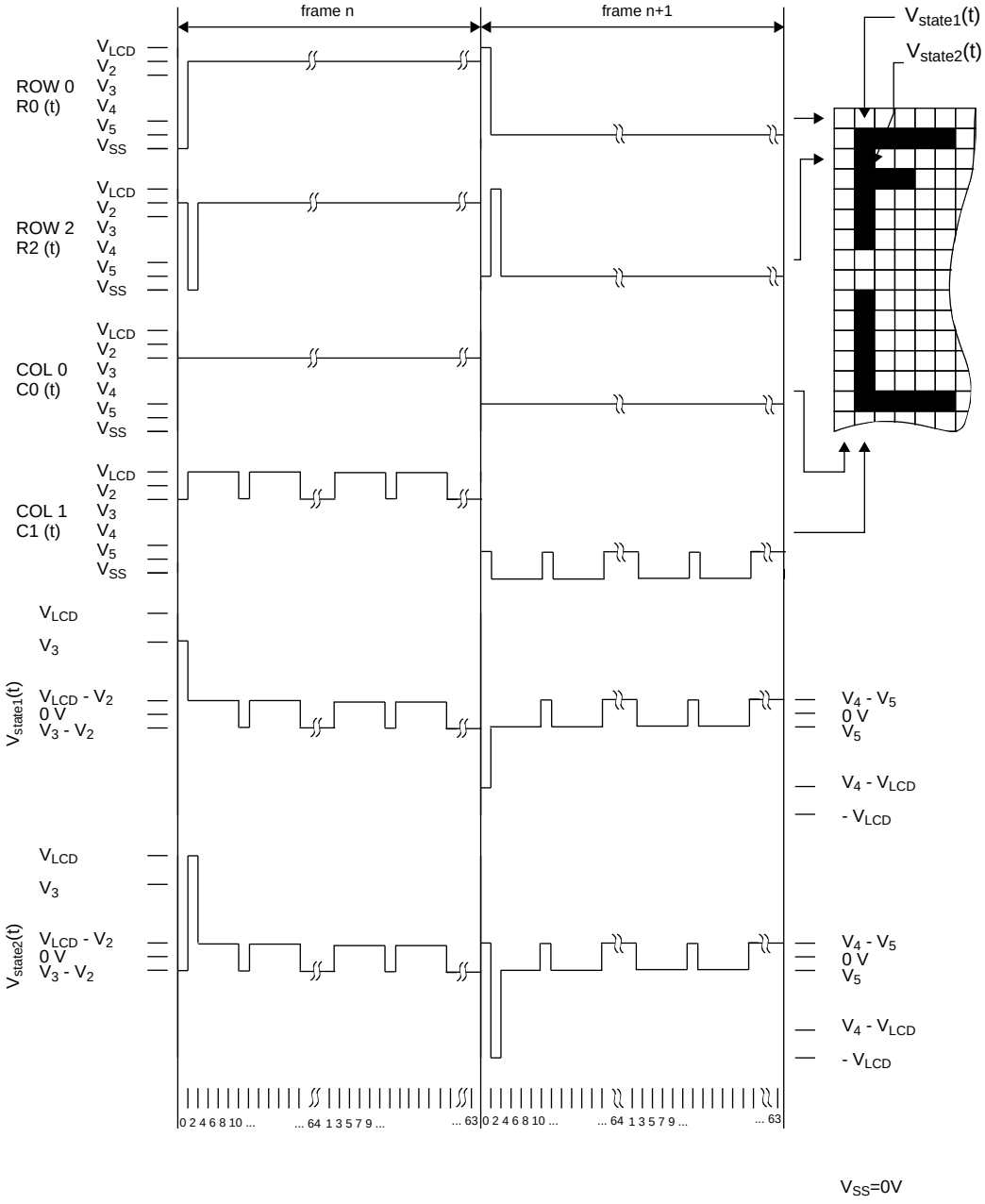
The PCF8549 contains a 65 × 102 bit static RAM which stores the display data. The RAM is divided into 8 banks of 102 bytes and one bank of 102 bits ((8 × 8 + 1) × 102 bits). During RAM access, data is transferred to the RAM via the I²C interface. There is a direct correspondence between X-address and column output number.

TIMING GENERATOR

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the I²C-bus.

LCD ROW AND COLUMN DRIVERS

The PCF8549 contains 65 row and 102 column drivers, which connect the appropriate LCD bias voltages to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



$V_{state1}(t) = C1(t) - R0(t)$
$V_{state2}(t) = C1(t) - R2(t)$

Fig.2 Typical LCD driver waveforms.

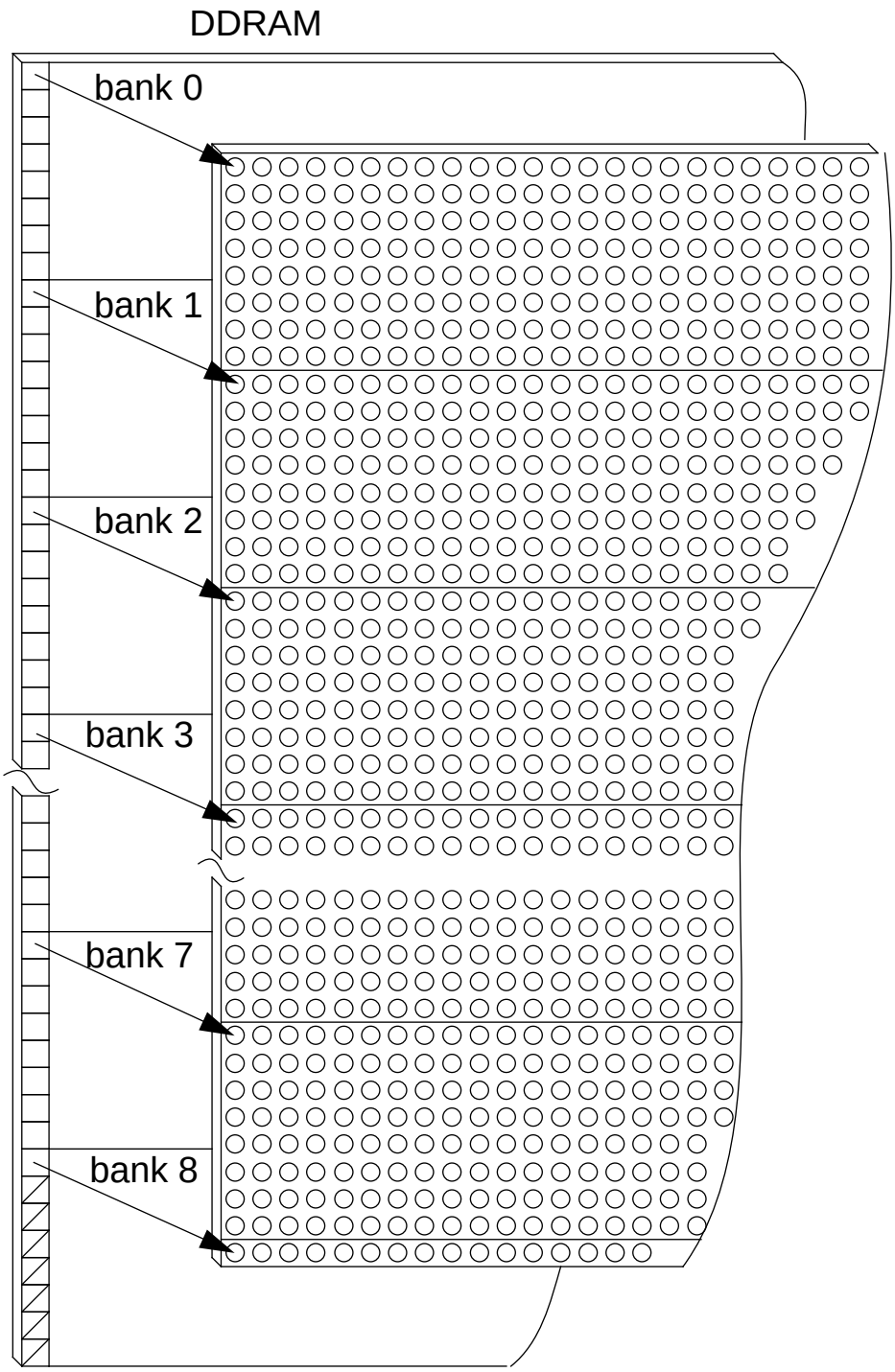


Fig.3 DDRAM to display mapping.

Addressing

The Display data RAM of the PCF8549 is accessed as indicated in Figs 3, 4, 4, 6 and 7. The display RAM has a matrix of 65 × 102 bits. The columns are addressed by the address pointer. The address ranges are:
X 0 to 101 (1100101b) and Y 0 to 8 (1000b). Addresses outside these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments (see Fig.7) after each byte. After the last Y address (Y = 8) Y wraps around to 0 and X increments to address the next column. In horizontal addressing mode (V = 0) the X address increments (see Fig.6) after each byte. After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row. After the very last address (X = 101 and Y = 8) the address pointers wrap around to address (X = 0 and Y = 0).

The MX bit allows a horizontal mirroring: When MX = 1, the X address space is mirrored: The address X = 0 is then located at the right side (column 101) of the display (see Fig.4). When MX = 0 the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.4).

If the RM-bit (read-modify-write mode) is set, the address is only incremented after a write, otherwise the address is incremented after both read and write access to the display data RAM.

DISPLAY DATA RAM STRUCTURE

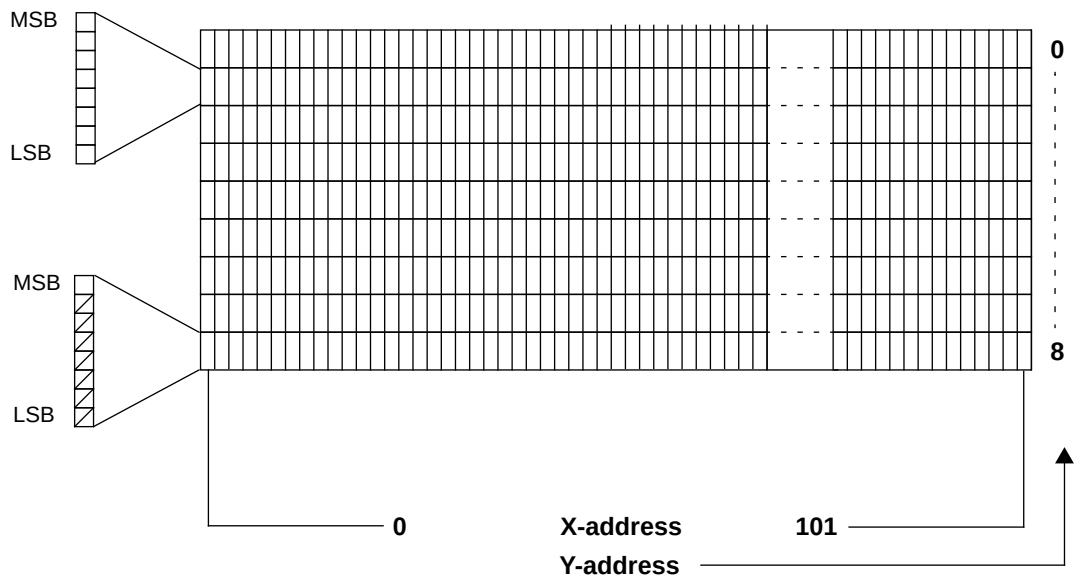


Fig.4 RAM format, addressing (MX = 0).

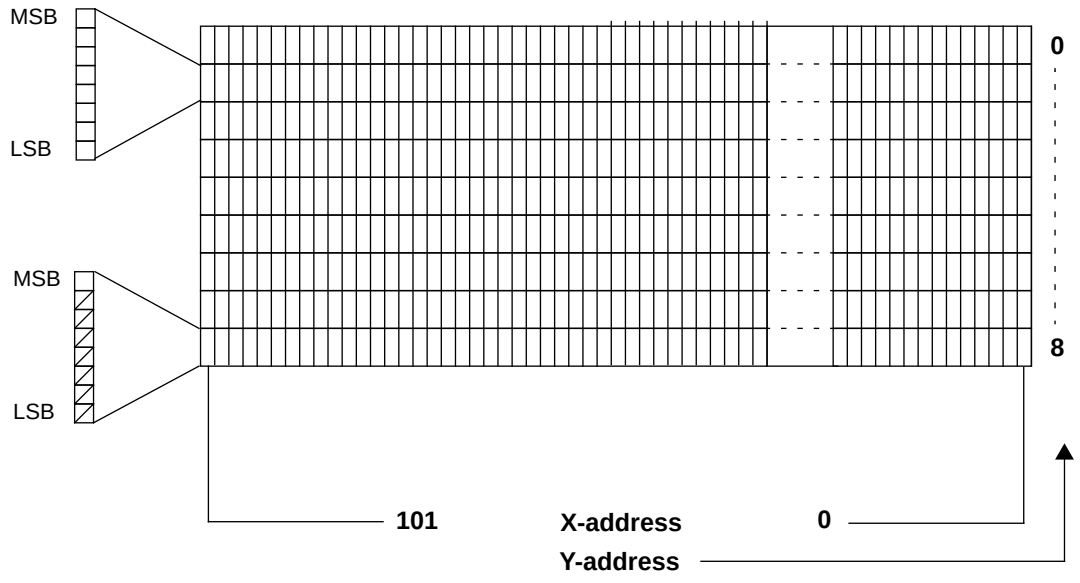


Fig.5 RAM format, addressing (MX = 1).

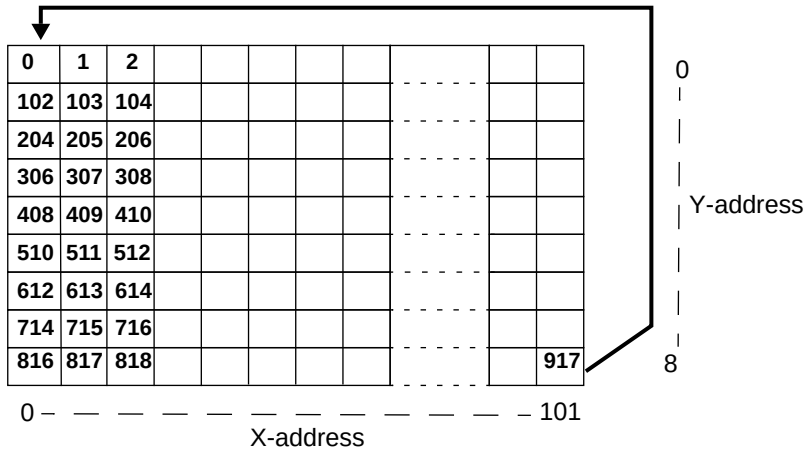


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

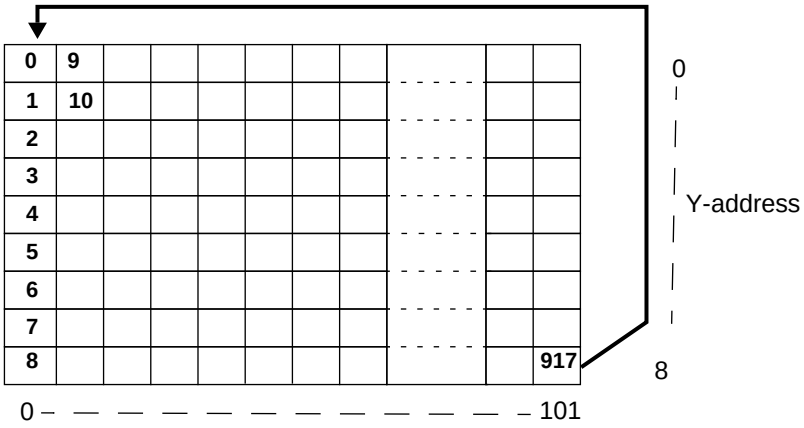


Fig.7 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

RAM access

If the D/$\overline{C}$ bit is 1 the RAM can be accessed in both read and write access mode, depending on the R/$\overline{W}$ bit. The data is written to the RAM during the acknowledge cycle.

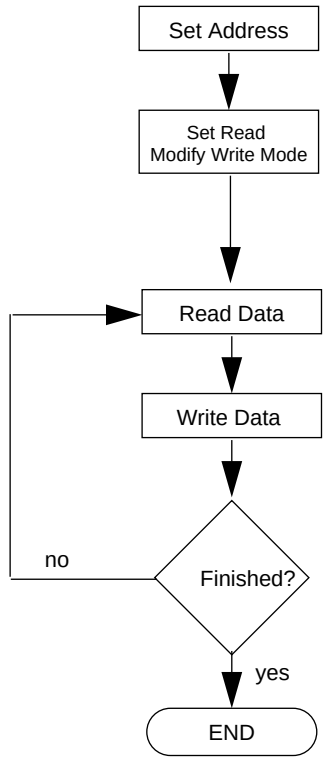


Fig.8 Read modify write access.

I²C-BUS INTERFACE

Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER (see Fig.9)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

START AND STOP CONDITIONS (see Fig.10)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

SYSTEM CONFIGURATION (see Fig.11)

- Transmitter: The device which sends the data to the bus
- Receiver: The device which receives the data from the bus
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: The device addressed by a master
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronisation: Procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE (see Fig.12)

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

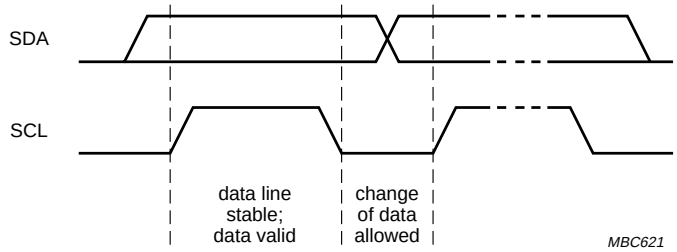


Fig.9 Bit transfer.

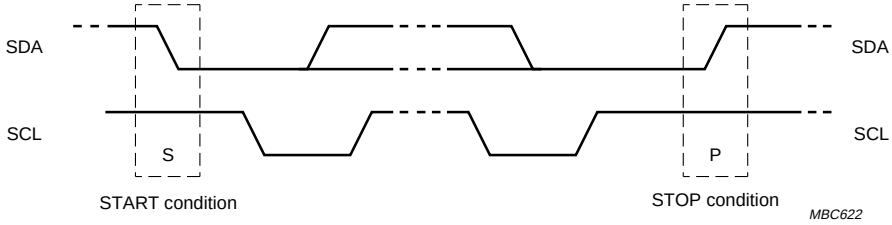


Fig.10 Definition of start and stop conditions.

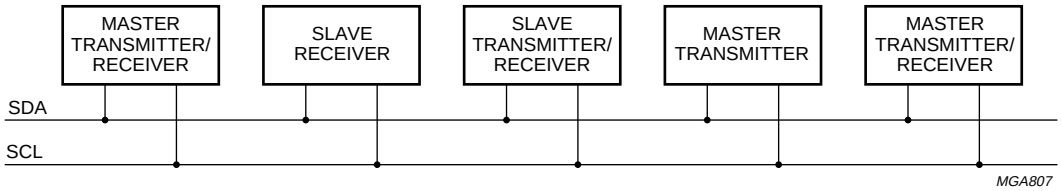


Fig.11 System configuration.

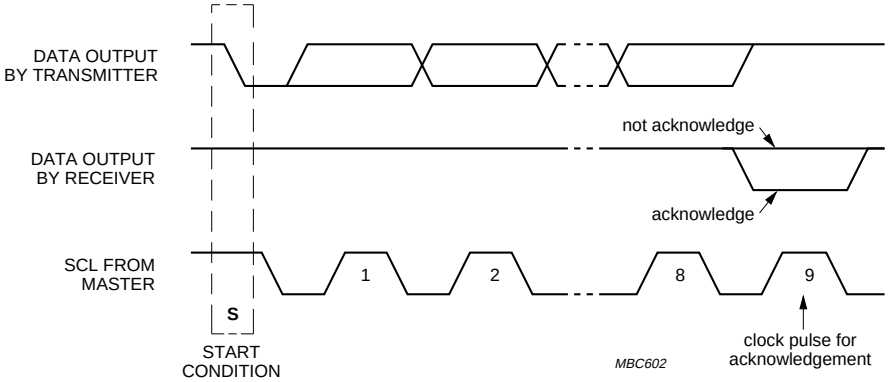


Fig.12 Acknowledgement on the I^2C-bus.

I²C-bus protocol

The PCF8549 supports both read and write access. The R/$\overline{W}$ bit is part of the slave address.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8549. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (V_{SS1}) or 1 (V_{DD1}).

The I²C-bus protocol is illustrated in Fig.13.

The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.13 and Table 1).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D/$\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data.The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to ‘1’, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8549 device. If the D/$\overline{C}$ bit of the last control byte was set to ‘0’, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a stop condition (P).

If the R/$\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the D/$\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

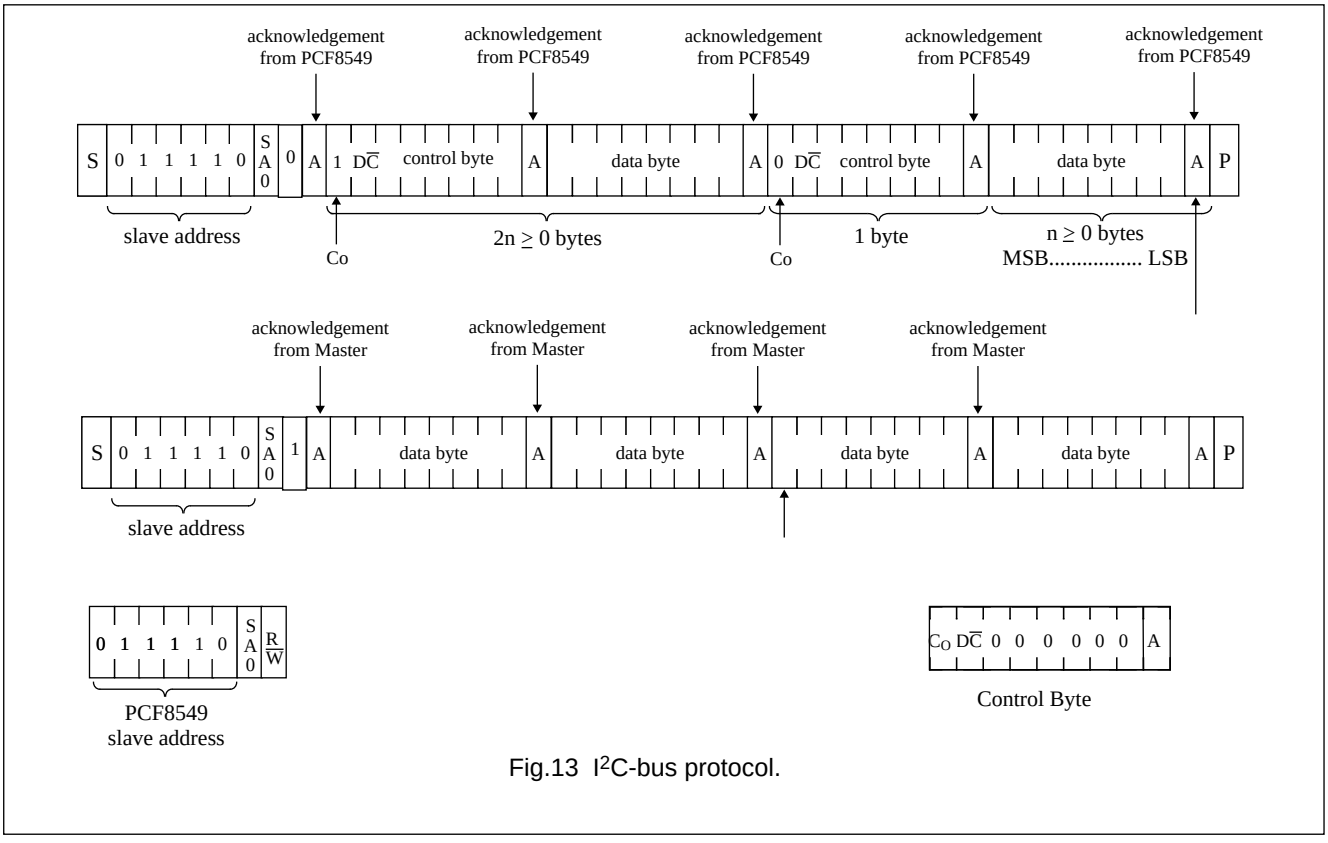


Fig.13 I²C-bus protocol.

INSTRUCTIONS

The instruction format is divided into two modes: If D/$\overline{C}$ is set low, the status byte can be read or commands can be sent to the chip, depending on the R/$\overline{W}$ signal. If D/$\overline{C}$ is set high, the DDRAM will be accessed. Every instruction can be sent in any order to the PCF8549.

Table 1 Instruction set

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								DESCRIPTION
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H = 0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Function Set	0	0	0	0	1	MX	MY	PD	V	H	power down control; entry mode; Extended Instruction Set control (H)
Read Status Byte	0	1	PD	X	X	D	E	MX	MY	X	reads status byte
Write Data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to RAM
Read Data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	reads data from RAM
H = 0											
Set Read Modify Write	0	0	0	0	0	0	0	0	1	RM	sets the read-modify-write mode
Reserved	0	0	0	0	0	0	0	1	X	X	do not use
Display Control	0	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	0	1	X	X	X	X	do not use
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y-address of RAM: $0 \leq Y \leq 8$
Set X address of RAM.	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X-address of RAM: $0 \leq X \leq 101$
H = 1											
Reserved	0	0	0	0	0	0	0	0	0	1	do not use
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Temperature Control	0	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
Reserved	0	0	0	0	0	0	1	X	X	X	do not use
Bias System	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Set Bias System(BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	do not use (reserved for test...)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations for symbols in Table 1

BIT		0	1	RESET STATE
PD		chip is active	chip is in power down mode	1
V		horizontal addressing	vertical addressing	0
H		use basic instruction set	use extended instruction set	0
MX		normal X-addressing	X-address is mirrored	0
MY		display is not vertically mirrored	display is vertically mirrored	0
RM		read-modify-write mode is disabled	read-modify-write mode is enabled	0
D and E	00	display blank		D = 0 E = 0
	10	normal mode		
	01	all display segments on		
	11	inverse video mode		
TC[1 : 0]	00	V_{LCD} temperature coefficient 0		TC[1 : 0] = 00
	01	V_{LCD} temperature coefficient 1		
	10	V_{LCD} temperature coefficient 2		
	11	V_{LCD} temperature coefficient 3		
BS[2 : 0]		bias system		BS[2 : 0] = 000

External reset ($\overline{RES}$)

After power-on a reset pulse has to be applied immediately to the chip, as it is in an undefined state. A reset of the chip can be achieved with the external reset pin. After the reset the LCD driver is set to the following status:

- Power down mode (PD = 1)
- All LCD-outputs at V_{SS} (display off)
- Read-modify-write mode is disabled (RM = 0)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Normal display (MX = MY = 0)
- Display blank (E = D = 0)
- Address counter X[6 : 0] = 0 and Y[3 : 0] = 0
- Temperature coefficient (TC[1 : 0] = 0)
- Bias system (BS[2 : 0] = 0)
- Read-modify-write mode disabled (RM = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{OP}[6 : 0] = 0)
- After power-on, RAM data are undefined; The reset signal does not change the content of the RAM.

Set read-modify-write

When RM = 0, the read-modify-write mode is disabled. The X/Y-address counter is incremented after every read or write access to the display data RAM.

When RM = 1, the read-modify-write mode is enabled. In this mode the X/Y-address is incremented only after a write access to the display data RAM. The X/Y-address will not be incremented after a read access to the RAM.

Function Set

PD (POWER DOWN)

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off
- Oscillator off (external clock possible)
- V_{LCD} can be disconnected
- Parallel bus, command, etc. function
- RAM contents not cleared; RAM data can be written.

V

When V = 0, the horizontal addressing is selected. The data is written into the RAM as shown in Fig.6. When V = 1, the vertical addressing is selected. The data is written into the RAM as shown in Fig.7.

H

When H = 0 the commands ‘display control’, ‘set Y address’ and ‘set X address’ can be performed, when H = 1 the other commands can be executed. The commands ‘write data’ and ‘function set’ can be executed in both cases.

MX

When MX = 0, the display is written from left to right (X = 0 is on the left side, X = 100 is on the right side of the display). When MX = 1 the display is written from right to left (X = 0 is on the right side, X = 100 is on the left side of the display).

MY

When MY = 1, the display is mirrored vertically.

Display Control

D AND E

The bits D and E select the display mode (see Table 2).

Set Y address of RAM

Y[3 : 0] defines the Y address vector address of the RAM.

Table 3 X-/Y-Address range

Y Y Y Y 3 2 1 0	CONTENT	ALLOWED X-RANGE
0 0 0 0	bank 0 (display RAM)	0 to 101
0 0 0 1	bank 1 (display RAM)	0 to 101
0 0 1 0	bank 2 (display RAM)	0 to 101
0 0 1 1	bank 3 (display RAM)	0 to 101
0 1 0 0	bank 4 (display RAM)	0 to 101
0 1 0 1	bank 5 (display RAM)	0 to 101
0 1 1 0	bank 6 (display RAM)	0 to 101
0 1 1 1	bank 7 (display RAM)	0 to 101
1 0 0 0	bank 8 (display RAM)	0 to 101

In bank 8 only the MSB is accessed.

Set X address of RAM

The X address points to the columns. The range of X is 0 to 101(65 hex).

Temperature Control

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimal contrast. There are 4 different temperature coefficients available in the

PCF8549 (see Fig.14). The coefficients are selected by the two bits TC[1 : 0]. Table 6 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed V_{LCD}.

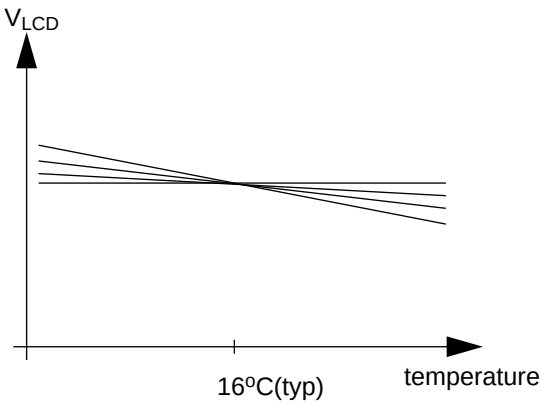


Fig.14 Temperature coefficients.

Bias value:

The bias voltage levels are set in the ratio of R – R – nR – R – R giving a $\frac{1}{n+4}$ bias system. The resulting bias levels are shown in table 5.

Different multiplex rates require different factors n (see Table 4). This is programmed by BS[2 : 0]. For MUX 1 : 65 the optimum bias value n is given by: $n = \sqrt{m} - 3 = \sqrt{65} - 3 = 5.06 = 5$

resulting in $^1/_9$bias.

Table 4 Programming the required Bias system

BS[2]	BS[1]	BS[0]	n	b (RES. COUNT)	MUX RATE
0	0	0	7	11	1 : 100
0	0	1	6	10	1 : 81
0	1	0	5	9	1 : 64
0	1	1	4	8	1 : 49
1	0	0	3	7	1 : 36

BS[2]	BS[1]	BS[0]	n	b (RES. COUNT)	MUX RATE
1	0	1	2	6	1 : 24
1	1	0	1	5	1 : 16
1	1	1	0	4	1 : 9

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES⁄
V1	V_{LCD}
V2	$(b-1)/b \times V_{LCD}$
V3	$(b-2)/b \times V_{LCD}$
V4	$2/b \times V_{LCD}$
V5	$1/b \times V_{LCD}$
V6	V_{SS}

Set V_{OP} value:

The operation voltage V_{LCD} can be set by software. The generated voltage is dependent of the temperature, the programmed temperature coefficient (TC), and the programmed voltage at reference temperature (T_{CUT}).

(1)

$$V_{LCD} = (a + VOP \cdot b) + (T - T_{CUT}) \cdot TC$$

The voltage at reference temperature ($V_{LCD}(T=T_{CUT})$) can be calculated as:

(2)

$$V_{LCD} = (a + VOP \cdot b)$$

The parameters are explained in table 6.

The maximum voltage that can be generated is depending on the $V_{DD2/2\_HV}$ Voltage and the display load current. The relation ship is shown in Fig.16.

The charge pump is turned off if Vop[6 : 0] is set to zero.

For Mux 1 : 65 the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{65}}\right)}} \cdot V_{th} = 6.85 \cdot V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

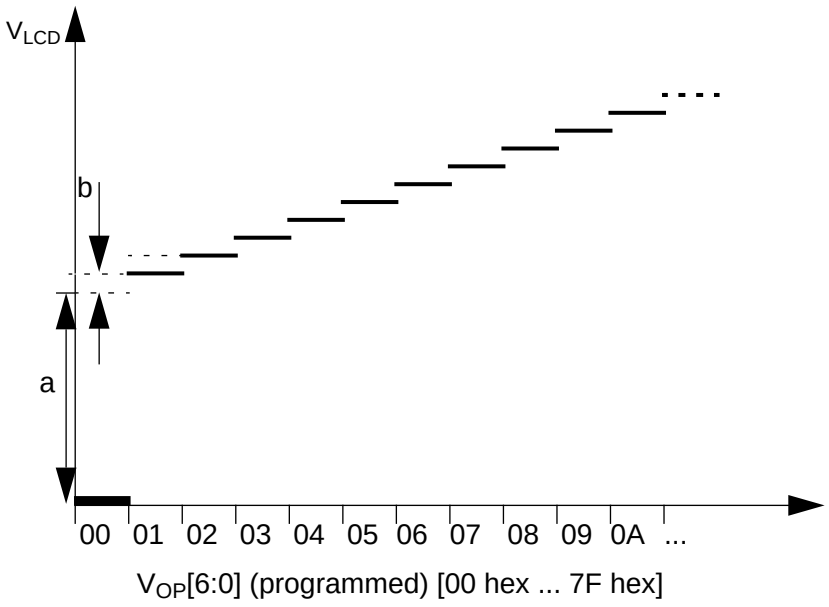


Fig.15 V_{OP} programming of PCF8549.

Table 6 Typical values for parameters for the HV-Generator programming

SYMBOL		VALUE	UNIT
a		7.06	V
b		0.06	V
T_{CUT}		16	^0C
TC	00	$-0.142 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/ºC
	01	$-1.3 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/ºC
	10	$-2.467 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/ºC
	11	$-3.483 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/ºC

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134); all voltages referred to V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	supply voltage range	-0.5	+7	V
V_{LCD}	supply voltage range LCD	-0.5	+17	V
I_{SS}	supply current	-50	50	mA
V_i/V_O	input/output voltage range	-0.5	V_{DD}+0.5	V
V_{OLCD}	LCD output voltage range	-0.5	V_{LCD}+0.5	V
I_i	DC input current	-10	10	mA
I_o	DC output current	-10	10	mA
P_{TOT}	power dissipation per package	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{AMB}	operating ambient temperature. range	-40	+85	℃
T_{STG}	storage temperature range	-65	+150	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. with external LCD supply voltage external supplied **(voltage generator disabled)**. V_{DDmax} (V_{DD2},V_{DD2_HV}) is **5V** if LCD supply voltage is internally generated (voltage generator enabled).

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS Devices”). The PCF8549 withstands the following stress:

- approximately 1.0kV Human Body Model
- approximately 150V Machine Model

DC CHARACTERISTICS

Table 7 V_{DD1} = 1.5 to 6 V; $V_{DD2/2\_HV}$ = 2.4 to 5.0 V; V_{DD2} = V_{DD2_HV}; V_{SS1} = V_{SS2} = V_{SS2_HV} = 0 V; V_{LCD} = 7 to 16 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD1}	Logic supply voltage range		1.5	3	6	V
V_{DD2}, V_{DD2_HV}	HV Generator supply range		2.4		5	V
I_{VDD1}	supply current internal V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0;		30	80	µA
$I_{VDD2/2\_HV}$	supply current internal V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0; (1)(5)		600	1200	µA
I_{VDD1}	supply current external V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0;		30	80	µA
$I_{VDD2/2\_HV}$	supply current external V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0; (2)(5)		0	10	µA
I_{VDD1}	supply current	power-down mode; V_{LCD} = 0V; f_{scl} = 0; display load = 0		0.5	10	µA
I_{LCD}	supply current external V_{LCD}	V_{LCD} = 10 V; f_{SCL}= 0, display load = 0; (2)		50	130	µA
$V_{LCD(tol)}$	V_{LCD} tolerance internal generated	V_{DD} = 2.7V; V_{LCD} = 10V; f_{SCL} = 0; display load = 0;(3)(4)(6)			+/- 500	mV
V_{IL}	LOW level input voltage		V_{SS}		0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}		V_{DD}	V
I_{OL}	LOW level output current (SDA)	V_{OL} = 0.4V; V_{DD1} = 5 V		3.0		mA
I_L	leakage current	V_I = V_{DD1} or V_{SS1}	-1		+1	µA
R_{ROW}	Row output resistance R0 to R64			12	20	kOhm
R_{COL}	Column output resistance C0 to C101			12	20	kOhm

Note

1. When a display is connected the I_{VDD2_HV} increases with 7 x display load current due to 7 stage charge pump.
2. With external V_{LCD}, the display load current does not translate into increased I_{VDD2_HV}.
3. For TC1, TC2 and TC3
4. The maximum possible VLCD voltage that may be generated is dependent on voltage ($V_{DD2/2\_HV}$), temperature and (display) load.
5. V_{DD2} V_{DD2_HV} connected together
6. Difference to the theoretical value given by equation 1

AC CHARACTERISTICS

Table 8 V_{DD1} = 1.5 to 6 V; $V_{DD2/2\_HV}$ = 2.4 to 5.0 V; V_{DD2} = V_{DD2_HV}; V_{SS1} = V_{SS2} = V_{SS2_HV} = 0 V; V_{LCD} = 7 to 16 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency		19	32	64	kHz
f_{EXT}	external clock frequency	(2)	10	32	64	kHz
t_{start}	oscillator start up time	(5)	–	450	1600	us
f_{FRAME}	frame frequency	f_{EXT} = 32 kHz;(1)	–	62	–	Hz
t_{VHRL}	VDD to $\overline{RES}$ Low	(5)			1	ms
t_{PWRES}	reset low pulse width		400	–	–	ns
I^2C timing characteristics						
f_{SCLK}	SCL clock frequency	(6)	DC	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	us
t_{HIGH}	SCL clock high period		0.6	–	–	us
$t_{SU;Data}$	Data set-up time		100	–	–	ns
$t_{HD;Data}$	Data hold time		0	–	0.9	us
t_R	SCL and SDA rise time	(3)	20 + 0.1 Cb	–	300	ns
t_F	SCL and SDA fall time	(3)	20 + 0.1 Cb	–	300	ns
c_b	Capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	setup time for a repeated START condition		0.6	–	–	us
$t_{HD;STA}$	start condition hold time		0.6	–	–	us
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold-time		0	–	–	ns
$t_{SU;STO}$	setup time for STOP condition		0.6	–	–	us
t_{SW}	tolerable spike width on bus	(4)	–	–	50	ns
t_{BUF}	BUS free time between a STOP and START condition		1.3	–	–	us

Note

1. $f_{FRAME} = \frac{f_{EXT}}{520}$
2. Duty cycle of 50 +/-5%.
3. The rise and fall times specified here refer to the driver device (i.e. not PCF8549) and are part of the general fast I^2C-bus specification. When PCF8549 asserts an acknowledge on SDA, the minimum fall time is 10ns. C_b= capacitive load per bus line.
4. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width < $t_{SW(max)}$.
5. Not tested in production
6. Only for VDD1= 2V to 6V

TYPICAL CHARACTERISTICS

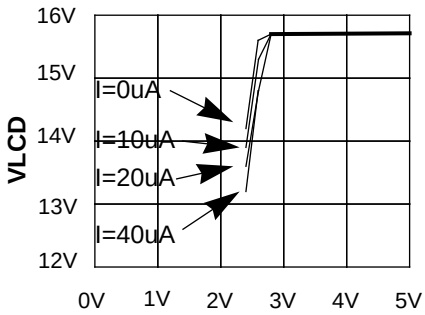


Fig.16 VLCD dependency of VDD2, VDD2_HV and load current. Programmed VLCD=15.8V (@ Room Temperature in special Test mode)

RESET

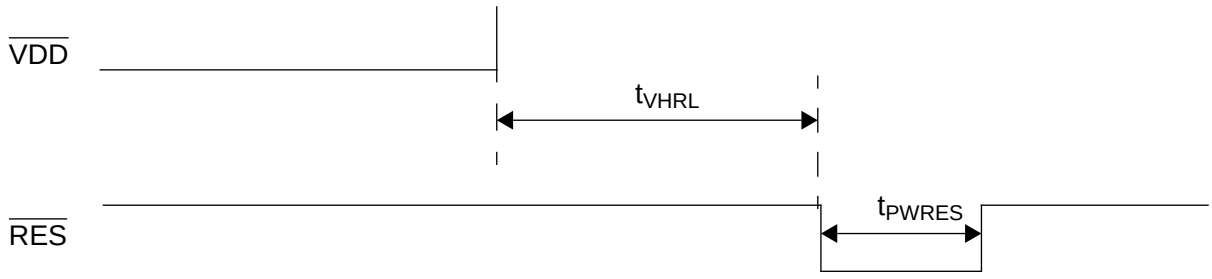
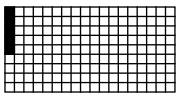
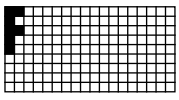
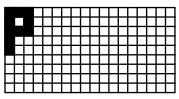
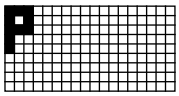
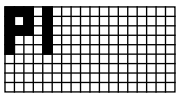
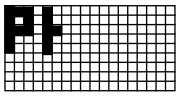
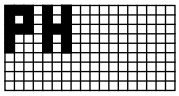
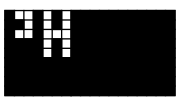


Fig.17 Reset timing.

APPLICATION INFORMATION

Table 9 programming example for PCF8549

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
1	I^2C start									
2	0	1	1	1	1	0	0	0		Slave address for write
3	0	0	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 0.
4	0	0	1	0	0	0	0	1		Function Set PD = 0; V = 0; select extended instruction set (H = 1 mode)
5	0	0	0	1	0	0	1	0		Set Bias System 2. This is the recommended Bias System for a multiplex rate 1:65
6	1	1	1	0	1	0	1	0		set V_{OP} V_{OP} is set to a +16 × b [V]. Please note: The required voltage is depending on the liquid.
7	0	0	1	0	0	0	0	0		Function Set PD = 0; V = 0; select normal instruction set (H = 0 mode)
8	0	0	0	0	1	1	0	0		Display Control set normal mode (D = 1 and E = 0)
9	I^2C start									Restart: To write into the Display RAM the D/$\overline{C}$ must be set to 1; therefore a control byte is needed.
10	0	1	1	1	1	0	0	0		Slave address for write
11	0	1	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 1.
12	1	1	1	1	1	0	0	0		Data Write Y and X are initialized to 0 by default, so they aren't set here
13	1	0	1	0	0	0	0	0		Data Write
14	1	1	1	0	0	0	0	0		Data Write

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
15	0	0	0	0	0	0	0	0		Data Write
16	1	1	1	1	1	0	0	0		Data Write
17	0	0	1	0	0	0	0	0		Data Write
18	1	1	1	1	1	0	0	0		Data Write
19	I^2C start									Restart
20	0	1	1	1	1	0	0	0		Slave address for write
21	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
22	0	0	0	0	1	1	0	1		Display Control Set inverse video mode (D = 1 and E = 1)
23	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
24	1	0	0	0	0	0	0	0		Set X address of RAM set address to ‘0000000’
25	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
26	0	0	0	0	0	0	0	0		Data Write
27	0	0	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 0.
28	1	0	0	0	0	0	0	0		Set X address of RAM Set address to ‘0000000’
29	0	0	0	0	0	0	0	1		Set Read Modify Write Mode

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
30	I^2C start									Restart
31	0	1	1	1	1	0	0	0		Slave address for write
32	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
33	I^2C start									Restart
34	0	1	1	1	1	0	0	1		Slave address for read
35	1	0	0	0	0	0	0	0		Read Data From Address ‘0000000’
36	1	0	0	0	0	0	0	0		Read Data From Address ‘0000000’ again. Master does not send an acknowledge to stop the read access.
37	I^2C start									Restart
38	0	1	1	1	1	0	0	0		Slave address for write
39	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
40	1	1	1	1	1	0	0	0		Write Data
41	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
42	I^2C start									Restart
43	0	1	1	1	1	0	0	1		Slave address for read
44	1	0	0	0	0	0	0	0		Read Status Byte

APPLICATION INFORMATION

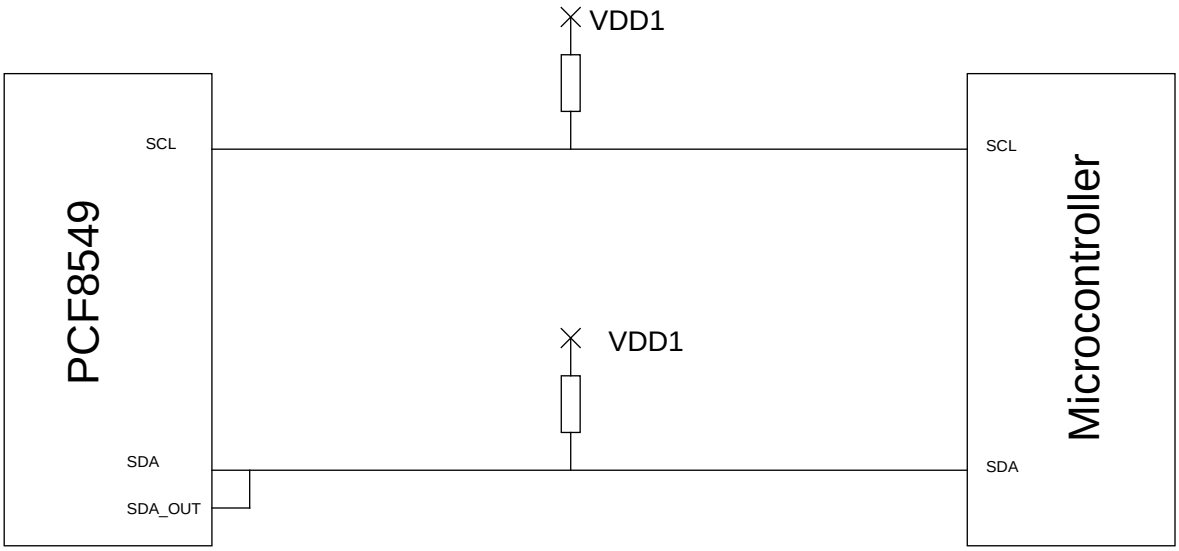


Fig.18 Application diagram: Connecting the I2C Interface

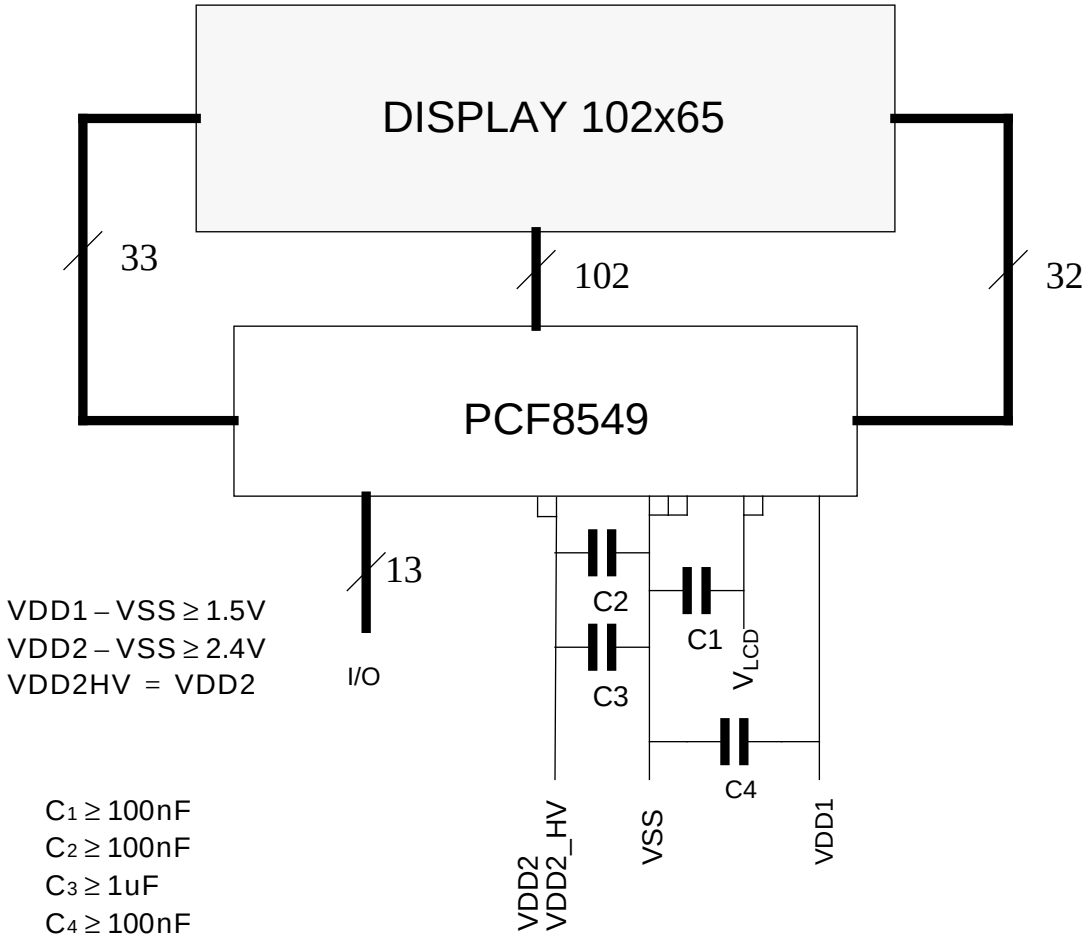


Fig.19 Application diagram: Connecting the power supplies

The pinning of the PCF8549 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 65 × 102 pixels.

CHIP INFORMATION

The PCF8549 is manufactured in n-well CMOS technology.

The substrate is on V_{SS} potential.

BONDING PADS

	VALUE	UNIT
Pad pitch	min. 100	μm
Pad size, alumin.	80 × 100	μm
Passivation.	48 × 78	μm
Bumps	60 (±6) × 90 (±6) × 17.5 (±5)	μm
Wafer thickness	380 (±25)	μm

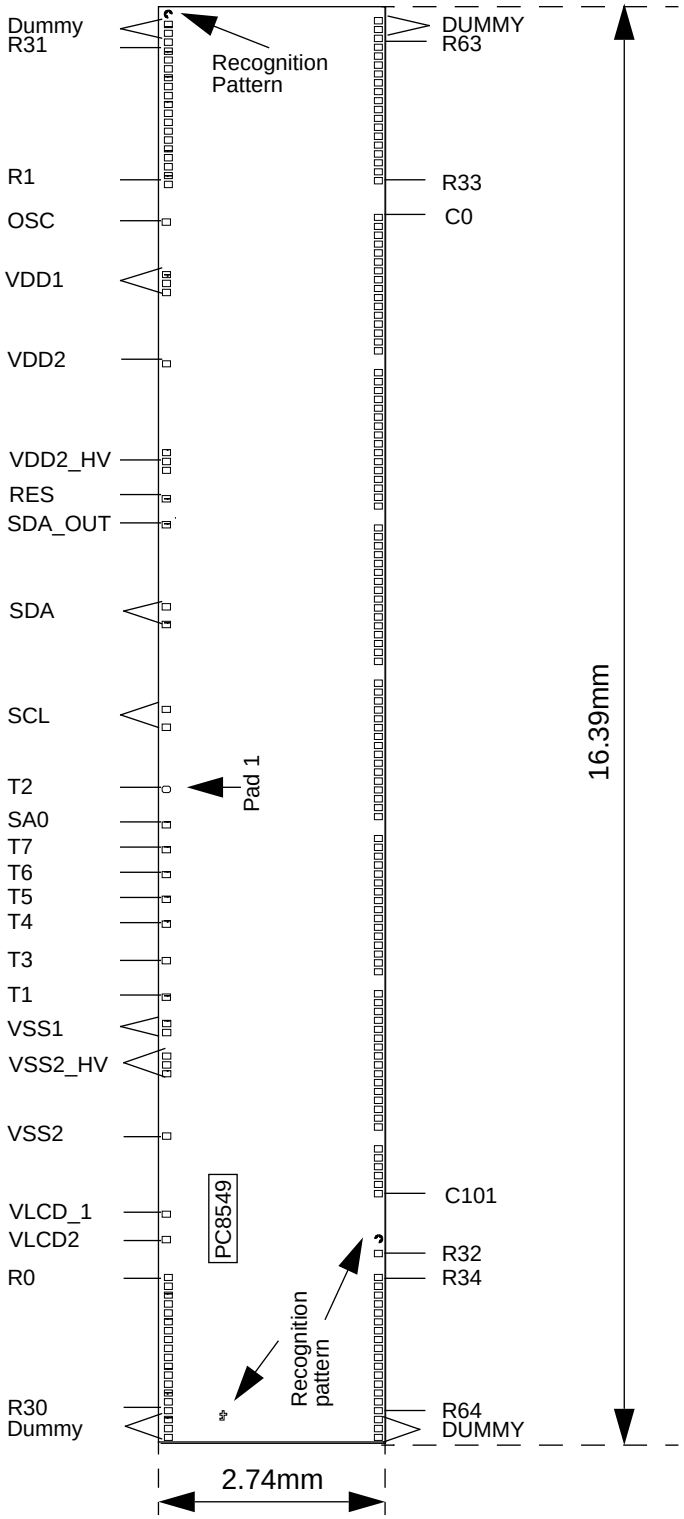

Dummy
R31
Recognition
Pattern
DUMMY
R63
R1
R33
OSC
C0
VDD1
VDD2
VDD2_HV
RES
SDA_OUT
SDA
SCL
T2
Pad 1
SA0
T7
T6
T5
T4
T3
T1
VSS1
VSS2_HV
VSS2
VLCD_1
VLCD2
R0
PC8549
C101
R32
R34
Recognition
pattern
R30
Dummy
R64
DUMMY
16.39mm
2.74mm

Fig.20 Pads.

Table 10 Bonding pad locations (dimensions in um).

Pad	Pad name	X	Y
1	T2	7359.5	2462
2	SA0	6958	2462
3	T7	6679	2462
4	T6	6400	2462
5	T5	6121	2462
6	T4	5841.5	2462
7	T3	5431.5	2462
8	T1	5022	2462
9	VSS1	4724	2458
10	VSS1	4624	2458
11	VSS2_HV	4359	2458
12	VSS2_HV	4259	2458
13	VSS2_HV	4159	2458
14	VSS2	3458.5	2458
15	VLCD1	2580	2462
16	VLCD2	2294	2462
17	ROW<0>	1870	2437
18	ROW<2>	1770	2437
19	ROW<4>	1670	2437
20	ROW<6>	1570	2437
21	ROW<8>	1470	2437
22	ROW<10>	1370	2437
23	ROW<12>	1270	2437
24	ROW<14>	1170	2437
25	ROW<16>	1070	2437
26	ROW<18>	970	2437
27	ROW<20>	870	2437
28	ROW<22>	770	2437
29	ROW<24>	670	2437
30	ROW<26>	570	2437
31	ROW<28>	470	2437
32	ROW<30>	370	2437
33	Dummy 4	270	2437
34	Dummy 5	170	2437
35	Dummy 6	70	2437
36	Dummy 3	70	84
37	Dummy 2	170	84
38	Dummy 1	270	84
39	ROW<64>	370	84
40	ROW<62>	470	84
41	ROW<60>	570	84
42	ROW<58>	670	84
43	ROW<56>	770	84
44	ROW<54>	870	84
45	ROW<52>	970	84
46	ROW<50>	1070	84
47	ROW<48>	1170	84
48	ROW<46>	1270	84
49	ROW<44>	1370	84
50	ROW<42>	1470	84
51	ROW<40>	1570	84
52	ROW<38>	1670	84
53	ROW<36>	1770	84
54	ROW<34>	1870	84
55	ROW<32>	2137	84
56	COL<101>	2812	84
57	COL<100>	2914	84
58	COL<99>	3014	84
59	COL<98>	3114	84
60	COL<97>	3214	84
61	COL<96>	3314	84
62	COL<95>	3560	84
63	COL<94>	3660	84
64	COL<93>	3760	84
65	COL<92>	3860	84
66	COL<91>	3960	84
67	COL<90>	4060	84
68	COL<89>	4160	84
69	COL<88>	4260	84
70	COL<87>	4360	84
71	COL<86>	4460	84
72	COL<85>	4560	84
73	COL<84>	4660	84
74	COL<83>	4760	84
75	COL<82>	4860	84
76	COL<81>	4960	84
77	COL<80>	5060	84
78	COL<79>	5306	84
79	COL<78>	5406	84
80	COL<77>	5506	84

Pad	Pad name	X	Y
81	COL<76>	5606	84
82	COL<75>	5706	84
83	COL<74>	5806	84
84	COL<73>	5906	84
85	COL<72>	6006	84
86	COL<71>	6106	84
87	COL<70>	6206	84
88	COL<69>	6306	84
89	COL<68>	6406	84
90	COL<67>	6506	84
91	COL<66>	6606	84
92	COL<65>	6706	84
93	COL<64>	6806	84
94	COL<63>	7052	84
95	COL<62>	7152	84
96	COL<61>	7252	84
97	COL<60>	7352	84
98	COL<59>	7452	84
99	COL<58>	7552	84
100	COL<57>	7652	84
101	COL<56>	7752	84
102	COL<55>	7852	84
103	COL<54>	7952	84
104	COL<53>	8052	84
105	COL<52>	8152	84
106	COL<51>	8252	84
107	COL<50>	8352	84
108	COL<49>	8452	84
109	COL<48>	8552	84
110	COL<47>	8798	84
111	COL<46>	8898	84
112	COL<45>	8998	84
113	COL<44>	9098	84
114	COL<43>	9198	84
115	COL<42>	9298	84
116	COL<41>	9398	84
117	COL<40>	9498	84
118	COL<39>	9598	84
119	COL<38>	9698	84
120	COL<37>	9798	84

Pad	Pad name	X	Y
121	COL<36>	9898	84
122	COL<35>	9998	84
123	COL<34>	10098	84
124	COL<33>	10198	84
125	COL<32>	10298	84
126	COL<31>	10544	84
127	COL<30>	10644	84
128	COL<29>	10744	84
129	COL<28>	10844	84
130	COL<27>	10944	84
131	COL<26>	11044	84
132	COL<25>	11144	84
133	COL<24>	11244	84
134	COL<23>	11344	84
135	COL<22>	11444	84
136	COL<21>	11544	84
137	COL<20>	11644	84
138	COL<19>	11744	84
139	COL<18>	11844	84
140	COL<17>	11944	84
141	COL<16>	12044	84
142	COL<15>	12290	84
143	COL<14>	12390	84
144	COL<13>	12490	84
145	COL<12>	12590	84
146	COL<11>	12690	84
147	COL<10>	12790	84
148	COL<9>	12890	84
149	COL<8>	12990	84
150	COL<7>	13090	84
151	COL<6>	13190	84
152	COL<5>	13290	84
153	COL<4>	13390	84
154	COL<3>	13490	84
155	COL<2>	13590	84
156	COL<1>	13690	84
157	COL<0>	13790	84
158	ROW<33>	14204	84
159	ROW<35>	14304	84
160	ROW<37>	14404	84

Pad	Pad name	X	Y
161	ROW<39>	14504	84
162	ROW<41>	14604	84
163	ROW<43>	14704	84
164	ROW<45>	14804	84
165	ROW<47>	14904	84
166	ROW<49>	15004	84
167	ROW<51>	15104	84
168	ROW<53>	15204	84
169	ROW<55>	15304	84
170	ROW<57>	15404	84
171	ROW<59>	15504	84
172	ROW<61>	15604	84
173	ROW<63>	15704	84
174	Dummy 7	15804	84
175	Dummy 8	15904	84
176	Dummy 9	16004	84
177	Dummy 12	15961	2437
178	Dummy 11	15861	2437
179	Dummy 10	15761	2437
180	ROW<31>	15661	2437
181	ROW<29>	15561	2437
182	ROW<27>	15461	2437
183	ROW<25>	15361	2437
184	ROW<23>	15261	2437
185	ROW<21>	15161	2437
186	ROW<19>	15061	2437
187	ROW<17>	14961	2437
188	ROW<15>	14861	2437
189	ROW<13>	14761	2437
190	ROW<11>	14661	2437
191	ROW<9>	14561	2437
192	ROW<7>	14461	2437
193	ROW<5>	14361	2437
194	ROW<3>	14261	2437
195	ROW<1>	14161	2437
196	OSC	13738	2462
197	VDD1	13147	2461
198	VDD1	13047	2461
199	VDD1	12947	2461
200	VDD2	12145	2461

Pad	Pad name	X	Y
201	VDD2_HV_IN	11145	2461
202	VDD2_HV_IN	11045	2461
203	VDD2_HV_IN	10945	2461
204	RES_B_IN	10627	2462
205	SDA_OUT	10333.55	2462
206	SDA_IN	9412.4	2462
207	SDA_IN	9212.4	2462
208	SCL_IN	8256.8	2462
209	SCL_IN	8056.8	2462
	Recpat C1	16275	2437
	Recpat C2	2301	80
	Recpat F	304	1824

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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