PRELIMINARY

SMALL SIZED QUARTZ CRYSTAL OSCILLATOR

■GENERAL DESCRIPTION

The **NJU6366** series is a C-MOS fundamental quartz crystal oscillator that consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

The 3-stage divider generates only one frequency selected of f_0,$f_0/2$,$f_0/4$ and $f_0/8$ by internal circuits is output.

The oscillation amplifier is realized very low stand-by current using NAND circuit.

The 3-state output buffer is C-MOS compatible

Furthermore, the package is small-sized MTP-6.

■PACKAGE OUTLINE

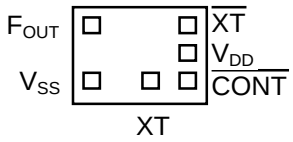

NJU6366XCT NJU6366XF

■FEATURES

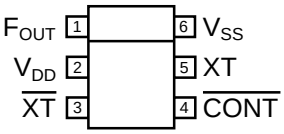
- ●Operating Voltage 2.0 to 5.5V
- ●Maximum Oscillation Frequency 50MHz(T.B.D.)
- ●Low Operating Current
- ●High Fan-out I_{OH}/I_{OL}=4mA @2.5V
- ●3-Stage Divider One of f_0,$f_0/2$,$f_0/4$ and $f_0/8$
- ●Oscillation Stop and Output Stand-by Function
- ●3-State Output Buffer
- ●Oscillation Capacitors Cg and Cg on-chip
- ●Package Outline Thin-Chip/MTP-6
- ●C-MOS Technology

■PAD LOCATION/PIN CONFIGURATION

Thin-Chip



MTP-6



■LINE-UP TABLE

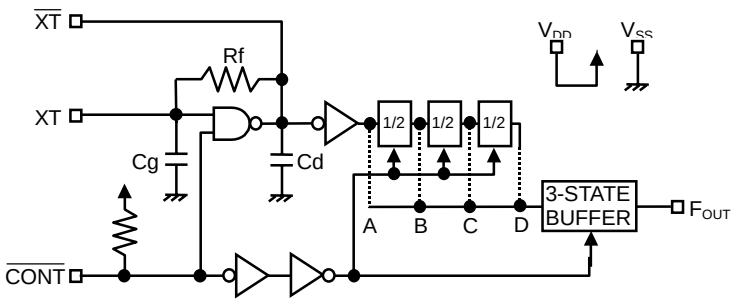
Type No.		F_{OUT}	Internal Connect		Cg/Cd
			Connect	Non Connect	
NJU6366	A	f_0	A Line	B,C,D Line	T.B.D
	B	$f_0/2$	B Line	A,C,D Line	T.B.D
	C	$f_0/4$	C Line	A,B,D Line	T.B.D
	D	$f_0/8$	D Line	A,B,C Line	T.B.D

■COORDINATES

Pad Name	X	Y
F_{OUT}	-207	247
V_{SS}	-207	-247
XT	33	-247
$\overline{CONT}$	207	-247
V_{DD}	207	-17
$\overline{XT}$	207	172

Starting Point:Chip Center Unit[um]
Chip Size:0.67x0.75mm
Thin-Chip Thickness:260±20um
Pad Size:90x90um

■BLOCK DIAGRAM



■TREMINAL DESCRIPTION

SYMBOL	FUNCTION
$\overline{CONT}$	Oscillation and 3-state Output Buffer Control
XT $\overline{XT}$	Quartz Crystal Connecting Terminals
V_{SS}	V_{SS}=0V
F_{OUT}	Frequency Output
V_{DD}	V_{DD}=2.5V/3.0V/5.0V

$\overline{CONT}$	F_{OUT}
H or OPEN	Output either one frequency selected of f_0, $f_0/2$,$f_0/4$ and $f_0/8$ Note1)
L	Oscillation Stop and High impedance Output

Note1) Refer to the line-up table.

■ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.5~+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5~V_{DD}+0.5	V
Output Voltage	V_O	-0.5~V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Output Current	I_O	±25	mA
Power Dissipation Note4)	P_D	200(MTP-6)	mW
Operating Temperature Range	Topr	-40~+85	℃
Storage Temperature Range	Tstg	-55~+125	℃

Note2) If the supply voltage(V_{DD}) is less than 7.0V, the input voltage must not over the V_{DD} level though 7.0V is limit specified.

Note3) Decupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

Note4) The power dissipation is the maximum value at only the package.

■ELECTRICAL CHARACTERISTICS

(Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		2.0		5.5	V

(V_{DD}=2.5V,Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	A version,fosc=16MHz,C_L=15pF			5	mA
		B version,fosc=16MHz,C_L=15pF			T.B.D	
		C version,fosc=16MHz,C_L=15pF			T.B.D	
		D version,fosc=16MHz,C_L=15pF			T.B.D	
Oscillation Stopping Current	I_{STB}	$\overline{CONT}$=V_{SS}, No load		2	5	uA
Stand-by Current	Ist	$\overline{CONT}$=XT=V_{SS}, No load Note5)			1	uA
Input Voltage	V_{IH}		2.0		2.5	V
	V_{IL}		0		0.5	V
Output Current	I_{OH}	V_{OH}=2.2V	4			mA
	I_{OL}	V_{OL}=0.3V	4			mA
Input Current	I_{IN}	$\overline{CONT}$=0.8V_{DD}		T.B.D	T.B.D	uA
		$\overline{CONT}$=0.2V_{DD}		T.B.D	T.B.D	uA
3-state Off Leakage Current	I_{OZ}	$\overline{CONT}$=V_{SS}, F_{OUT}= V_{DD} or V_{SS}			±0.1	uA
Feedback Resistance	Rf			T.B.D		kΩ
Internal Capacitor	Cg/Cd	fosc=16MHz		T.B.D		pF
Maximum Oscillation Frequency	F_{MAX}		T.B.D			MHz
Output Signal Symmetry	SYM	C_L=15pF, @V_{DD}/2	45	50	55	%
Output Signal Rise Time	tr	C_L=15pF,10%~90%		3	6	ns
Output Signal Fall Time	tf	C_L=15pF,90%~10%		3	6	ns
Output Disable time	T_{PLZ}	C_L=15pF,R_{UP}=10kΩ			250	ns
Output Enable Time	T_{PZL}	C_L=15pF,R_{UP}=10kΩ			250	ns

Note5) Excluding input current on $\overline{CONT}$ Terminal.

(V_{DD}=3.0V,Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	A version,fosc=16MHz,C_L=15pF			6	mA
		B version,fosc=16MHz,C_L=15pF			T.B.D	
		C version,fosc=16MHz,C_L=15pF			T.B.D	
		D version,fosc=16MHz,C_L=15pF			T.B.D	
Oscillation Stopping Current	I_{STB}	$\overline{CONT}$=V_{SS}, No load		2	5	uA
Stand-by Current	Ist	$\overline{CONT}$=XT=V_{SS}, No load Note5)			1	uA
Input Voltage	V_{IH}		2.4		3.0	V
	V_{IL}		0		0.6	V
Output Current	I_{OH}	V_{OH}=2.7V	5			mA
	I_{OL}	V_{OL}=0.3V	5			mA
Input Current	I_{IN}	$\overline{CONT}$=0.8V_{DD}		T.B.D	T.B.D	uA
		$\overline{CONT}$=0.2V_{DD}		T.B.D	T.B.D	uA
3-state Off Leakage Current	I_{OZ}	$\overline{CONT}$=V_{SS}, F_{OUT}= V_{DD} or V_{SS}			±0.1	uA
Feedback Resistance	Rf			T.B.D		kΩ
Internal Capacitor	Cg/Cd	fosc=16MHz		T.B.D		pF
Maximum Oscillation Frequency	F_{MAX}		50			MHz
Output Signal Symmetry	SYM	C_L=15pF, @V_{DD}/2	45	50	55	%
Output Signal Rise Time	tr	C_L=15pF,10%~90%		3	6	ns
Output Signal Fall Time	tf	C_L=15pF,90%~10%		3	6	ns
Output Disable time	T_{PLZ}	C_L=15pF,R_{UP}=10kΩ			200	ns
Output Enable Time	T_{PZL}	C_L=15pF,R_{UP}=10kΩ			200	ns

Note5) Excluding input current on $\overline{CONT}$ Terminal.

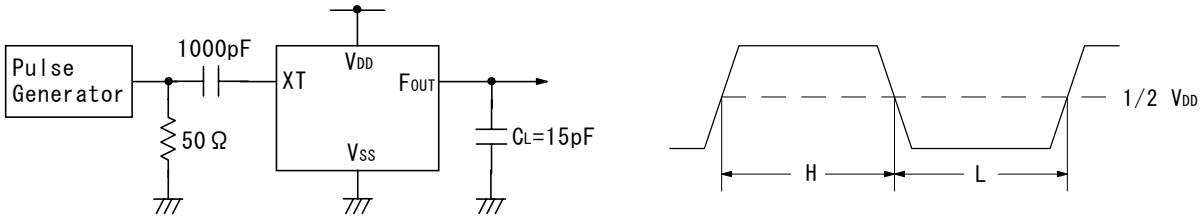
(V_{DD}=5.0V,Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	A version,fosc=16MHz,C_L=15pF			10	mA
		B version,fosc=16MHz,C_L=15pF			T.B.D	
		C version,fosc=16MHz,C_L=15pF			T.B.D	
		D version,fosc=16MHz,C_L=15pF			T.B.D	
Oscillation Stopping Current	I_{STB}	$\overline{CONT}$=V_{SS}, No load		5	10	uA
Stand-by Current	Ist	$\overline{CONT}$=XT=V_{SS}, No load Note5)			1	uA
Input Voltage	V_{IH}		3.5		5.0	V
	V_{IL}		0		1.5	V
Output Current	I_{OH}	V_{OH}=4.5V	8			mA
	I_{OL}	V_{OL}=0.5V	8			mA
Input Current	I_{IN}	$\overline{CONT}$=0.8V_{DD}		T.B.D	T.B.D	uA
		$\overline{CONT}$=0.2V_{DD}		T.B.D	T.B.D	uA
3-state Off Leakage Current	I_{OZ}	$\overline{CONT}$=V_{SS}, F_{OUT}= V_{DD} or V_{SS}			±0.1	uA
Feedback Resistance	Rf			T.B.D		kΩ
Internal Capacitor	Cg/Cd	fosc=16MHz		T.B.D		pF
Maximum Oscillation Frequency	F_{MAX}		50			MHz
Output Signal Symmetry	SYM	C_L=15pF, @V_{DD}/2	45	50	55	%
Output Signal Rise Time	tr	C_L=15pF,10%~90%		3	6	ns
Output Signal Fall Time	tf	C_L=15pF,90%~10%		3	6	ns
Output Disable time	T_{PLZ}	C_L=15pF,R_{UP}=10kΩ			100	ns
Output Enable Time	T_{PZL}	C_L=15pF,R_{UP}=10kΩ			100	ns

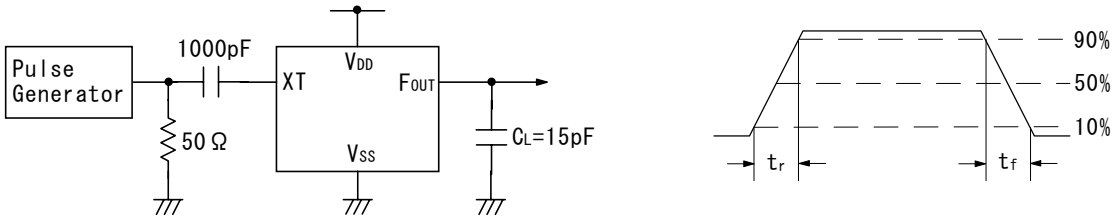
Note5) Excluding input current on $\overline{CONT}$ Terminal.

■MEASURMENT CIRCUITS

(1)Output Signal Symmetry(C_L=15pF)



(2)Output Signal Rise/Fall Time(C_L=15pF)



(3)Output Disable/Enable Time(C_L=15pF,R_{UP}=10kΩ)