AN8124K

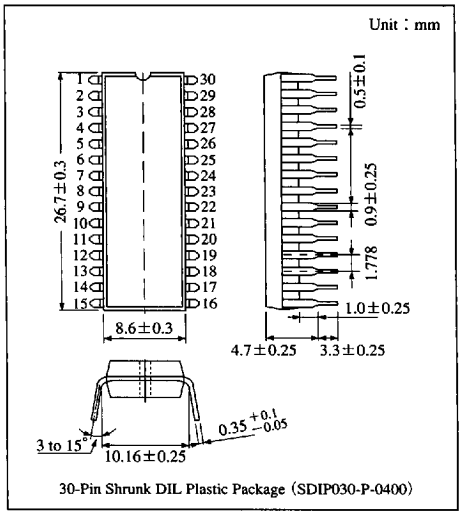
High-speed 8-bit A/D and D/A Converter IC

■ Overview

The AN8124K is a Bi-CMOS LSI containing 8-bit A/D and D/A converter whose maxmum conversion rate is 20MSPS. It operates on 5V single power supply and its I/O level is compatible with TTL and most suitable for digitalizing the video processing, such as VCR and TV.

■ Features

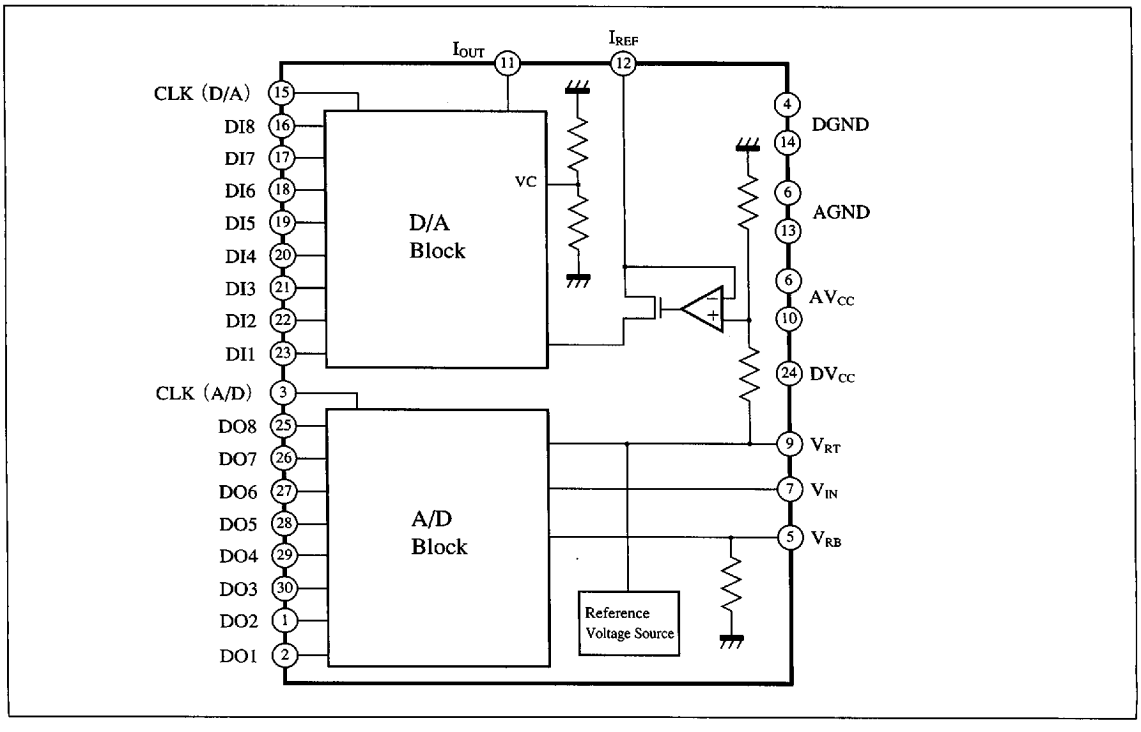
- 8-bit resolution
- Max. conversion rate : 20MSPS
- Power consumption : 250mW
- I/O level is compatible with TTL
- Reference power supply built-in



30-Pin Shrunk DIL Plastic Package (SDIP030-P-0400)

ICs for TV

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	7	V
Supply current	I_{CC}	100	mA
Power dissipation	P_D	700	mW
Operating ambient temperature	T_{opr}	−20 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

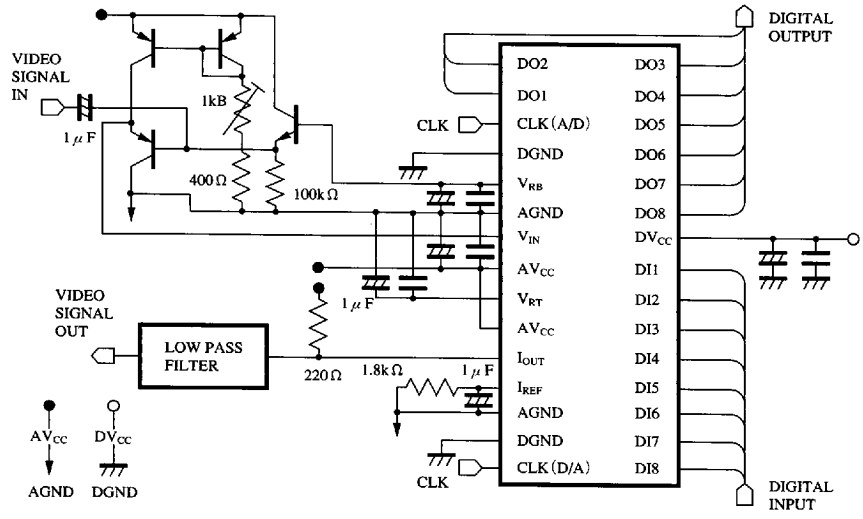
■ Recommended Operating Range (Ta=25℃)

Parameter		Symbol	Range
Digital supply voltage		DV_{CC}	4.75V to 5.25V
Analog supply voltage		AV_{CC}	4.75V to 5.25V
A/D	Analog input voltage	V_{IN}	V_{RB} to V_{RT}
	Clock input voltage	V_{IH}	2.4V to DV_{CC}
		V_{IL}	DGND to 0.8V
	Digital output current	I_{OH}	−1mA
		I_{OL}	1mA
	Clock input pulse width	t_H	25ns to
		t_L	25ns to
D/A	Reference resistance	R_{REF}	1.8kΩ
	Output load resistance	R_O	220Ω
	Digital input voltage	V_{IH}	2.4V to DV_{CC}
		V_{IL}	DGND to 0.8V
	Clock input pulse width	t_{WH}	25ns to
		t_{WL}	25ns to

■ Electrical Characteristics (Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit	Note
Supply current	I_{CC}	f_{CLK}=15MHz R_{REF}=1.8kΩ	—	50	80	mA	—
Reference resistor current	I_{RT}	$V_{RT}-V_{RB}$=2V	—	9	20	mA	—
Reference resistor current	I_{RB}	$V_{RT}-V_{RB}$=2V	−20	−9	—	mA	—
Input bias current	I_{IN}	V_{IN}=2.5V	—	40	120	μA	—
Clock input current	I_{IH}	V_{IH}=2.4V	—	—	30	μA	—
Clock input current	I_{IL}	V_{IL}=0.4V	−30	—	—	μA	—
Digital output voltage	V_{OH}	I_{OH}=−2mA	V_{CC}−0.8	—	—	V	—
Digital output voltage	V_{OL}	I_{OL}=2mA	—	—	0.4	V	—
Resolution	RES		—	8	—	bit	A/D
Maximum conversion rate	F_C		20	—	—	MSPS	A/D
Linearity error	E_L	V_{RT}=3.5V V_{RB}=1.5V	—	±0.5	±1	LSB	A/D
Differential linearity error	E_D	V_{RT}=3.5V V_{RB}=1.5V	—	±0.5	±1	LSB	A/D
Resolution	RES		—	8	—	bit	D/A
Maximum conversion rate	F_C	R_{OUT}=220Ω R_{REF}=1.8kΩ	20	—	—	MSPS	D/A
Linearity error	E_L	R_{OUT}=220Ω R_{REF}=1.8kΩ	—	—	±0.5	LSB	D/A
Differential linearity error	E_D	R_{OUT}=220Ω R_{REF}=1.8kΩ	—	—	±0.5	LSB	D/A
Full-scale current	I_{FS}	R_{OUT}=220Ω R_{REF}=1.8kΩ	—	4.8	—	mA	D/A
Hold time	t_H		20	—	—	ns	D/A
Setup time	t_S		20	—	—	ns	D/A
Setting time	t_{ST}	R_{OUT}=220Ω R_{REF}=1.8Ω	—	—	50	ns	D/A

Application Circuit



Pin Descriptions

Pin No.	Pin name	Typ. waveform	Description	I/O impedance	Equivalent circuit
24	Digital power supply	—	Digital power pin.	—	—
4, 14	Digital GND	—	Digital GND pin.	—	—
8, 10	Analog power supply	—	Analog power pin.	—	—
6, 13	Analog GND	—	Analog GND pin.	—	—
7	Analog signal input	3.5V / 1.5V	Input pin for analog signal to A/D.	500kΩ	×256
9	Reference voltage high	DC 3.5V	Reference power pin. This voltage determines the upper limit of input of an analog signal to A/D.	250Ω	250Ω
5	Reference voltage low	DC 1.5V	Reference power pin. This voltage determines the lower limit of input of an analog signal to A/D.	250Ω	
3	A/D clock input	Refer to the timing chart.	A/D clock pin. Sampling is made at the rising edge of clock pulse.	—	
1, 2 25 to 30	A/D digital output	Same as above.	A/D digital output pin.	—	
12	A/D full-scale current adjustment	DC	D/A full-scale current setting pin. Connect the resistor between this pin and analog GND.	—	
11	D/A current output	5V / 4V	D/A analog output pin. Connect the load resistor (75Ω) between this pin and analog power supply, and current is converted to voltage.	—	
15	D/A clock input	Refer to the timing chart.	D/A clock pin. Data is latched at clock rising edge.	—	
16 to 23	D/A digital data input	Same as above.	D/A digital data input pin.	—	

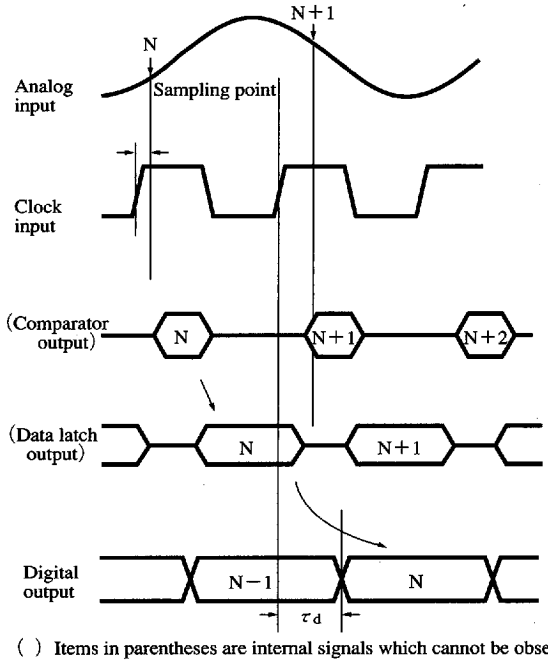
■ Supplementary Explanation

• Reference Value for Design in Electrical Characteristics (Ta=25℃)

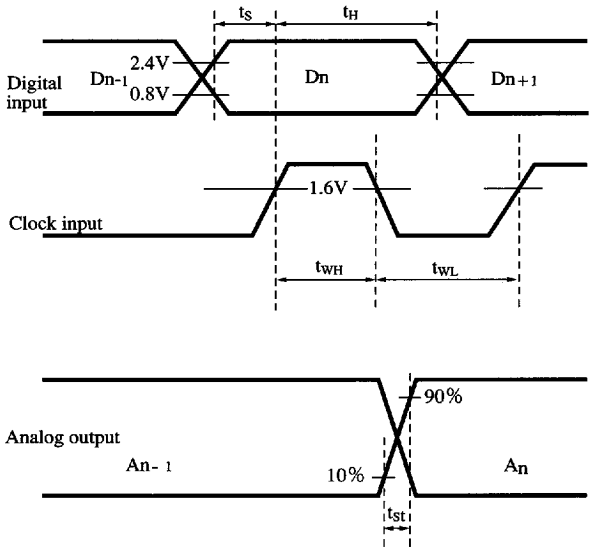
Parameter	Symbol	Condition	min	typ	max	Unit	Note
Equivalent input impedance	R_{IN}	V_{IN}=2.5V	—	500	—	kΩ	A/D
Input capacitance	C_{IN}	V_{IN}=2.5V	—	40	—	pF	A/D
Digital output delay	τ_d		—	25	—	ns	A/D
Differential gain	DG		—	1	—	%	D/A
Differential phase	DP		—	0.5	—	deg	D/A
S/N	S/N	f_{IN}=4MHz, f_S=20MHz	35	40	—	dB	D/A

Note) The value in the above characteristics is not a guaranteed value, but reference one on design.

• A/D Sampling Timing Chart



• D/A Timing Chart



( ) Items in parentheses are internal signals which cannot be observed from the outside.

■ Supplementary Explanation (cont.)

• Output Code Table

Step	Input signal voltage	Digital output
	$2.000V_{FS}$ 8.000mV STEP	M L 12345678
000	1.50000V	00000000
001	1.50800V	00000001
·	·	·
·	·	·
127	2.51600V	01111111
128	2.52400V	10000000
129	2.53200V	10000001
·	·	·
·	·	·
254	3.53200V	11111110
255	3.54800V	11111111

• Output Voltage Table

Step	Digital input	Output voltage
	Binary	V_{OUT}(V)
000	00000000	4.00000
001	00000001	4.00391
·	·	·
·	·	·
127	01111111	4.49609
128	10000000	4.50000
129	10000001	4.50391
·	·	·
·	·	·
254	11111110	4.99608
255	11111111	5.00000