AN4030

MA31750 - Use Of NMA31750 Samples

Application Note

Replaces July 2000 version, AN4030-8.0

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The following Applications Note presents information which will be of use to design engineers who are evaluating the N iteration of the MA31750 microprocessor. In particular, it defines the aspects of the current device operation which do not fully meet the requirements of the specification. This note covers all of the known problems found to date with the N iteration parts.

1. LONG LOADS AND STORES IN 1750B MODE

When using the long load instructions in 1750B mode, the status word does not update the flags bits according to the data just loaded. If a conditional branch or jump is to be determined on the data long loaded, then an explicit compare must be executed before the branch or jump instruction.

During long load and store instructions, the status word is written between each memory access. In the status word written during the loads / stores the PS bits mimic the AS bits. This can be a problem if there is an MMU present in the system as it may cause illegal memory accesses due to access locks and keys no longer matching.

2. EXTENDED MULTIPLICATION IN 1750B MODE

In 1750B mode, when using EFM / EFMR to multiply 2 numbers, both with an exponent of 0x80, the normalisation method incorrectly determines that an overflow has occurred. The result is forced to the largest positive value (7FFF FF7F FFFF) if the signs of the multiplicands were the same, and to the largest negative number (8000 007F 0000) if the signs of the multiplicands were different. In both cases, the overflow flag is set. A workaround within the overflow interrupt service routine would be to check the exponent of the multiplicand that has not been overwritten. If the exponent value is 0x80, then an overflow result must be erroneous and appropriate action can be taken if required. This problem does not occur in 1750A mode.

3. UNSIGNED SUBTRACT IN 1750B

If a negative flag is set as the result of an unsigned subtract, the carry flag will also be set. This may be incorrect.

4. FAULT MASK WRITES IN 1750B MODE

The fault mask is permanantly stuck at $FFFF_H$. The fault mask write XIO is legal in 1750B mode, but has no effect on the contents of the mask register.

5. BUS TIMEOUTS AND THE FAULT REGISTER

When RDYN stays high during an external memory or IO access (ie. DSN is low), then a timeout fault (either bit 5 or bit 8), will be logged in the fault register. Internally, the CPU sets a timeout flag. This timeout flag is only cleared by servicing the machine error interrupt or by executing the CLIR XIO instruction. Normally, when a fault is activated, the ME interrupt is serviced immediately and the timeout flag is cleared. However, if the ME interrupt is masked, any further external cycles will be flagged as having a timeout fault. This could erroneously set either bit 5 or bit 8 in the fault register. This is also a problem in console mode when console has priority over interrupts.

6. DE-GRANTING THE PROCESSOR

It is strongly recommended that users should reference Application Note 11 for the MA31750, if the CPU is ever to be de-granted.

7. SELECTING MULTIPLE BPU DEVICES

When multiple BPUs are present in a system (in1750B) the configuration register must have BPU0 set high otherwise the XIO MPEN is disabled. This means that 2MWords of BPU protection cannot be selected.

8. EXTERNAL CYCLES WITH NO ACTIVE DATA STROBES

During an external machine cycle, AS can go active whilst DSN / RDN / WRN remain inactive. This is caused by the occurrance of aborted cycles. Cycles can be aborted causing the following effects:

a: If MPROEN and / or EXADEN are held low for 2 falling edges of TCLK, the current machine cycle aborts without producing any data strobes.

b: If PEN is active when AS falls, the following cycle (if it is external) will produce an active AS with no data strobes (if the ME interrupt is unmasked). This AS can be extended by MPROEN and / or EXADEN being low.

c: If a fixed point overflow occurs, the CPU begins to fetch the next instruction. It then aborts this fetch to go back and execute the overflow routine. This aborted fetch is a fixed machine cycle of 2 CLKs. The AS is active for a fixed length of 1.5 CLK cycles. This cannot be extended by MPROEN, EXADEN or RDYN. This has implications when using an MMU and BPU in the system at 16MHz, as a cache miss for both the MMU and BPU would mean that MPROEN could be invalid when the CPU samples it on AS falling. If the system is restricted to the use of either an MMU or a BPU, there is enough time available to ensure that MPROEN is valid before it is sampled. Alternatively, if the system speed is slowed to approximately 10MHz, both an MMU and a BPU can be used. A further implication of external cycles with no data strobes is that wait state generators must not be started on the AS rising edge, but on DSN active. (An additional reason for this is that the NMA31750 inserts CLK cycles between AS rising and DSN falling if MPROEN or EXADEN are active or if an interrupt occurs).

9. EARLY WAIT STATES AFTER ABORT

If the Machine Error interrupt is masked, and an early wait timeout occurs, the current cycle is aborted. If the subsequent cycle is external, early wait states cannot be added.

10. BUS FAULT TIMEOUT SERVICING

If a bus fault timeout occurs, due to RDYN held high for 2 falling edges of TCLK, and the machine error interrupt is unmasked, the processor will service the ME interrupt service routine. This ISR is erroneously aborted and restarted by the microprocessor which causes the CPU to enter a continuous loop. This can only be halted by an active RESETN signal.

11. EXTENDED FLOATING POINT ADDS AND SUBTRACTS

If the answer produced as the result of an extended floating point add or subtract is a small positive number, which is contained within the 8 least significant bits before normalisation, then the answer will be incorrectly set to zero. The macros are available to replace the extended floating point adds and subtracts. These are given in the MA31750, AN16.

12. EXTENDED FLOATING POINT COMPARES

If 2 numbers are compared and the result is a small positive number contained in the 16 LSB's, then the status flag will incorrectly indicate zero rather than positive. A macro is available to replace the extended floating point compare instructions. This is given in MA31750, AN16.

13. FLOATING SUBTRACTS

If the subtraction 0x800001XX - 0x800000XX is done, the MA31750 gives the eroneous result of zero. (XX represents any exponent. (Both numbers have the same exponent).

14. PARITY CHECKING

The NMA31750 has a slow path within its data parity checking circuit which will affect the device when running at speeds over 120MHz, at high temperatures and low voltages. This slow path can result in 2 types of error:

Case (a)

If a parity error has occurred on a cycle when DPARN is low, and DPARN is then raised, the following external cycle will be logged as having a parity error.

Case (b)

If a genuine parity error has occurred a machine error interrupt will be flagged but no parity error interrupt will be flagged but no parity error is set in the fault register.

If parity checking is required at high speeds over the military temperature and voltage range, either a valid parity bit should be generated at all times, or DPARN low should be extended to cover an extra external cycle to prevent Case (a) from occuring. Case (b) cannot be avoided unless clock speeds are reduced.

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