REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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SHEET	15	16	17	18	19															

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Thomas M. Hess

CHECKED BY Thomas M. Hess

APPROVED BY Monica L. Poelking

DRAWING APPROVAL DATE
94-09-07

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 8-BIT TTL/BTL REGISTERED TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-94574**

SHEET 1 OF 19

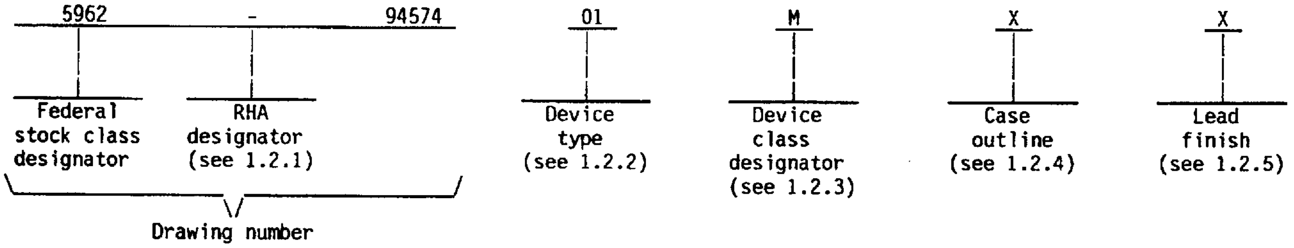
DESC FORM 193
JUL 94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FB2033	8-bit TTL/BTL registered transceiver

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP1-F56	56	flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input voltage range	
(V_I, except B port)	-1.2 V to 7 V
(V_I, B port)	-1.2 V to 3.5 V
Input current range, (except B port)	-40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state	-0.5 V to 3.5 V
Voltage range applied to any output in the high state (A port)	-0.5 V to V_{CC}
Current applied to any single output in the low state	
A port	48 mA
B port	200 mA
Maximum power dissipation, P_D	
(T_A = 55°C, still air)	1.7 W
(T_A = 25°C)	1.1 W
Storage temperature range	-65°C to 150°C

1.4 Recommended operating conditions. 2/

Supply voltage (V_{CC}, BG V_{CC})	$4.75\ V \le V_{CC} \le 5.25$
Supply Voltage (bias V_{CC})	$4.5\ V \le V_{CC} \le 5.5\ V$
Input transition rise or fall rate ($\Delta t/\Delta v$) except B port	10 ns/V
High level input voltage (V_{IH})	
B port.	$1.62\ V \le V_{IH} \le 2.3\ V$
except B port	2 V min
Low level input voltage (V_{IL})	
B port.	$0.75\ V \le V_{IL} \le 1.47\ V$
except B port	0.8 V max
High level ouput current (I_{OH})	
AO port	-3.0 mA max
Low level output current (I_{OL})	
AO port	24 mA max
B port	100 mA max
Ambient operating temperature	-55°C to 125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unused or floating pins (input or I/O) must be held high or low.
3/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block shall be as specified on figure 2.

3.2.4 Truth table. The truth table shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 127 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_A \leq +125°C$ unless otherwise specified $4.75\ V \leq V_{CC} \leq 5.25$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IK}	$V_{CC} = 4.75$ V, $I_I = -18$ mA	1, 2, 3	All		-1.2	V
Output voltage high AO port	V_{OH}	$V_{CC} = 4.75$ V to 5.25 V $I_{OH} = -10$ µA	1, 2, 3	All		V_{CC} - 1.0	V
Output voltage high AO port	V_{OH}	$V_{CC} = 4.75$ V, $I_{OH} = -3$ mA $V_{CC} = 4.75$ V, $I_{OH} = -32$ mA	1, 2, 3	All	2.5 2.0	3.4 -	V
Output voltage low AO port	V_{OL}	$V_{CC} = 4.75$, $I_{OL} = 20$ mA $V_{CC} = 4.75$, $I_{OL} = 55$ mA	1, 2, 3	All		0.5 0.8	V
Output voltage low B port	V_{OL}	$V_{CC} = 4.75$, $I_{OL} = 100$ mA $V_{CC} = 4.75$, $I_{OL} = 4$ mA	1, 2, 3	All	0.75 0.5	1.1	V
Input current Except B port	I_I	$V_{CC} = 0$ V, $V_I = 5.25$ V	1, 2, 3	All		100	µA
Input current high except B port 2/	I_{IH}	$V_{CC} = 5.25$ V, $V_I = 2.7$ V	1, 2, 3	All		50	µA
Input current high B port	I_{IH}	$V_{CC} = 0$ to 5.25 V $V_I = 2.1$ V	1, 2, 3	All		100	µA
Input current low except B port	I_{IL}	$V_{CC} = 5.25$ V, $V_I = 0.5$ V	1, 2, 3	All		-50	µA
Input current low B port 2/	I_{IL}	$V_{CC} = 5.25$ V $V_I = 0.75$ V	1, 2, 3	All		-100	µA
Output current high B port	I_{OH}	$V_{CC} = 0$ to 5.25 V, $V_I = 2.1$ V	1, 2, 3	All		100	µA
Output current high tristate, AO port	I_{OZH}	$V_{CC} = 5.25$ V $V_O = 2.7$ V	1, 2, 3	All		50	µA
Output current high tristate, AO port	I_{OZL}	$V_{CC} = 5.25$ V, $V_O = 0.5$ V	1, 2, 3	All		-50	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified 4.75 V ≤ V_{CC} ≤ 5.25 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output short circuit current, A0 port 3/	I_{OS}	V_{CC} = 5.25 V, V_O = 0 V	1, 2, 3	All	-40	-150	mA
Power supply current All outputs on	I_{CC}	V_{CC} = 5.25 V, I_O = 0 A	1, 2, 3	All		90	mA
Input Capacitance All port and control inputs	C_I	V_I = V_{CC} or GND See 4.4.1c	4	All		9.5	pF
Output capacitance A0 port	C_O	V_O = V_{CC} or GND See 4.4.1c	4	All		9.0	pF
Input/Output capacitance B port	$C_{I/O}$	V_{CC} = 0 to 4.75 V	4	All		8	pF
		V_{CC} = 4.75 V to 5.25 V				8	
Functional test		See 4.4.1b	7, 8	All			
Clock frequency	f_{clock}	V_{CC} = 5 V, T_A = 25°C See figure 3	9	All	0	150	MHz
		V_{CC} = 4.75 V to 5.25 V See figure 3	10, 11				
Pulse duration, CLKAB/LEAB or CLKBA/LEBA	t_W	See figure 3, V_{CC} = 5.0 V	9	All	3.9		ns
		V_{CC} = 4.75 V, 5.25 V	10, 11		4.3		
Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	t_{SU}	See figure 3, V_{CC} = 5.0 V	9	All	2.9		ns
		V_{CC} = 4.75 V 5.25 V	10, 11		3.3		
Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	t_H	See figure 3, V_{CC} = 5.0 V	9	All	1.0		ns
		V_{CC} = 4.75 V 5.25 V	10, 11		1.3		
Maximum frequency	f_{Max}	See figure 3, V_{CC} = 5.0 V	9	All	150		MHz
		V_{CC} = 4.75 V 5.25 V	10, 11				
Propagation delay AI (thru mode) to $\overline{B}$	t_{PLH}	See figure 3, V_{CC} = 5.0 V	9	All	1.7	4.6	ns
		V_{CC} = 4.75 V 5.25 V	10, 11		1.2	7.5	
Propagation delay AI (thru mode) to $\overline{B}$	t_{PHL}	See figure 3, V_{CC} = 5.0 V	9	All	1.3	4.3	ns
		V_{CC} = 4.75 V 5.25 V	10, 11		1.0	5.5	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	**SIZE A**		**5962-94574**
		REVISION LEVEL	SHEET 7

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_A \leq +125°C$ unless otherwise specified $4.75\ V \leq V_{CC} \leq 5.25$ 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay $\overline{B}$ (thru mode) to AO	t_{PLH}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.5	5.9	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.4	7.6	
Propagation delay $\overline{B}$ (thru mode) to AO	t_{PHL}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.7	5.7	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.6	7.8	
Propagation delay AI (transparent) to $\overline{B}$	t_{PLH}	See figure 3	$V_{CC} = 5.0\ V$	9	All	1.7	4.6	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.2	8.7	
Propagation delay AI (transparent) to $\overline{B}$	t_{PHL}	See figure 3	$V_{CC} = 5.0\ V$	9	All	1.3	4.3	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.0	5.9	
Propagation delay $\overline{B}$ (transparent) to AO	t_{PLH}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.5	5.8	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.5	7.8	
Propagation delay $\overline{B}$ (transparent) to AO	t_{PHL}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.7	5.7	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.6	8.0	
Propagation delay OEB to $\overline{B}$	t_{PLH}	See figure 3	$V_{CC} = 5.0\ V$	9	All	1.6	4.7	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.1	6.6	
Propagation delay OEB to $\overline{B}$	t_{PHL}	See figure 3	$V_{CC} = 5.0\ V$	9	All	1.2	4.1	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		0.4	5.4	
Propagation delay $\overline{OEB}$ to B	t_{PLH}	See figure 3	$V_{CC} = 5.0\ V$	9	All	1.3	4.3	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.2	6.6	
Propagation delay $\overline{OEB}$ to B	t_{PHL}	See figure 3	$V_{CC} = 5.0\ V$	9	All	1.2	4.4	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		0.8	5.5	
Propagation delay OEA to AO	t_{PZH}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.0	5.1	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.2	6.6	
Propagation delay OEA to AO	t_{PZL}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.7	6.1	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.3	7.7	
Propagation delay OEA to AO	t_{PHZ}	See figure 3	$V_{CC} = 5.0\ V$	9	All	2.1	5.8	ns
			$V_{CC} = 4.75\ V$ $5.25\ V$	10, 11		1.1	6.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified 4.75 V ≤ V_{CC} ≤ 5.25 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay OEA to A0	t_{PLZ}	See figure 3	V_{CC} = 5.0 V	9	All	1.6	4.7	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.0	6.0	
Propagation delay CLKAB/LEAB to B	t_{PLH}	See figure 3	V_{CC} = 5.0 V	9	All	2.1	5.8	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.6	8.7	
Propagation delay CLKAB/LEAB to B	t_{PHL}	See figure 3	V_{CC} = 5.0 V	9	All	2.0	5.6	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.1	6.6	
Propagation delay CLKBA/LEBA to A0	t_{PLH}	See figure 3	V_{CC} = 5.0 V	9	All	2.0	5.4	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.4	6.7	
Propagation delay CLKBA/LEBA to A0	t_{PHL}	See figure 3	V_{CC} = 5.0 V	9	All	2.2	5.6	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.5	6.5	
Propagation delay OMODE to B	t_{PLH}	See figure 3	V_{CC} = 5.0 V	9	All	2.3	6.1	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.6	8.1	
Propagation delay OMODE to B	t_{PHL}	See figure 3	V_{CC} = 5.0 V	9	All	1.4	6.0	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.0	6.5	
Propagation delay IMODE to A0	t_{PLH}	See figure 3	V_{CC} = 5.0 V	9	All	1.8	5.9	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.3	7.3	
Propagation delay IMODE to A0	t_{PHL}	See figure 3	V_{CC} = 5.0 V	9	All	2.3	5.4	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.4	6.4	
Propagation delay LOOPBACK to A0	t_{PLH}	See figure 3	V_{CC} = 5.0 V	9	All	2.4	7.1	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.6	8.3	
Propagation delay LOOPBACK to A0	t_{PHL}	See figure 3	V_{CC} = 5.0 V	9	All	3.1	6.9	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.8	7.5	
Propagation delay A1 to A0	t_{PLH}	See figure 3	V_{CC} = 5.0 V	9	All	1.9	5.7	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.4	7.1	
Propagation delay A1 to A0	t_{PHL}	See figure 3	V_{CC} = 5.0 V	9	All	2.6	5.8	ns
			V_{CC} = 4.75 V 5.25 V	10, 11		1.6	7.3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified 4.75 V ≤ V_{CC} ≤ 5.25 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{B}$-port input pulse rejection 4/	t_{PR}	See figure 3	9, 10, 11	All	1		ns
Live Insertion Parameters							
Output voltage $\overline{B}$ port	V_O	V_{CC} = 0 V V_I (BIAS V_{CC}) = 4.5 to 5.5 V	1, 2, 3	All	1.62	2.1	V
Input current BIAS V_{CC}	I_{CC} (BIAS)	V_I(BIAS V_{CC}) = 4.5 to 5.5 V V_{CC} = 0 to 4.5 V, V_B = 0 to 2 V	1, 2, 3	All		400	µA
Input current BIAS V_{CC}	I_{CC} (BIAS)	V_I(BIAS V_{CC}) = 4.5 to 5.5 V V_{CC} = 4.5 to 5.5 V, V_B = 0 to 2 V	1, 2, 3	All		10	µA
Output current $\overline{B}$ port	I_O	V_{CC} = 0 V V_I(BIAS V_{CC}) = 4.5 to 5.5 V V_B = 1 V	1, 2, 3	All	-30		µA
Output current $\overline{B}$ port	I_O	V_{CC} = 0 to 5.5 V $\overline{OEB}$ = 0 to 0.8 V	1, 2, 3	All		170	µA
Output current $\overline{B}$ port	I_O	V_{CC} = 0 to 2.2 V $\overline{OEB}$ = 0 to 5.0 V	1, 2, 3	All		100	µA
Miscellaneous characteristics							
Peak bus voltage during turnoff of 100 mA into 40 nH ($\overline{B}$ port) 4/	V_{OHP}		1, 2, 3	All		4	V
Minimum bus voltage during turnoff of 100 mA into 40 nH ($\overline{B}$ port) 4/	V_{OHV}		1, 2, 3	All	1.62		V
Minimum bus voltage during high to low switch ($\overline{B}$ port)	V_{OLV}	I_{OL} = -50 mA	1, 2, 3	All	0.3		V

1/ All testing shall be performed using worst case test conditions unless otherwise specified.
2/ For I/O ports, the parameter I_{IH} and I_{IL} include the off-state output current.
3/ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
4/ Parameter is based on characterization data but not tested.

Case X

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	NC	16	AI5	31	OMODE1	46	$\overline{B3}$
2	IMODE1	17	AO5	32	V_{CC}	47	GND
3	CLKAB/LEAB	18	AI6	33	OEB	48	$\overline{B2}$
4	V_{CC}	19	AO6	34	$\overline{OEB}$	49	GND
5	GND	20	AI7	35	GND	50	$\overline{B1}$
6	AI1	21	GND	36	$\overline{B8}$	51	BIAS V_{CC}
7	AO1	22	AO7	37	GND	52	BG GND
8	AI2	23	AI8	38	$\overline{B7}$	53	OEA
9	GND	24	AO8	39	GND	54	BG V_{CC}
10	AO2	25	GND	40	$\overline{B6}$	55	IMODE0
11	AI3	26	V_{CC}	41	GND	56	NC
12	AO3	27	CLKBA/LEBA	42	$\overline{B5}$		
13	AI4	28	NC	43	GND		
14	AO4	29	NC	44	$\overline{B4}$		
15	LOOPBACK	30	OMODE0	45	GND		

FIGURE 1. Terminal connections.

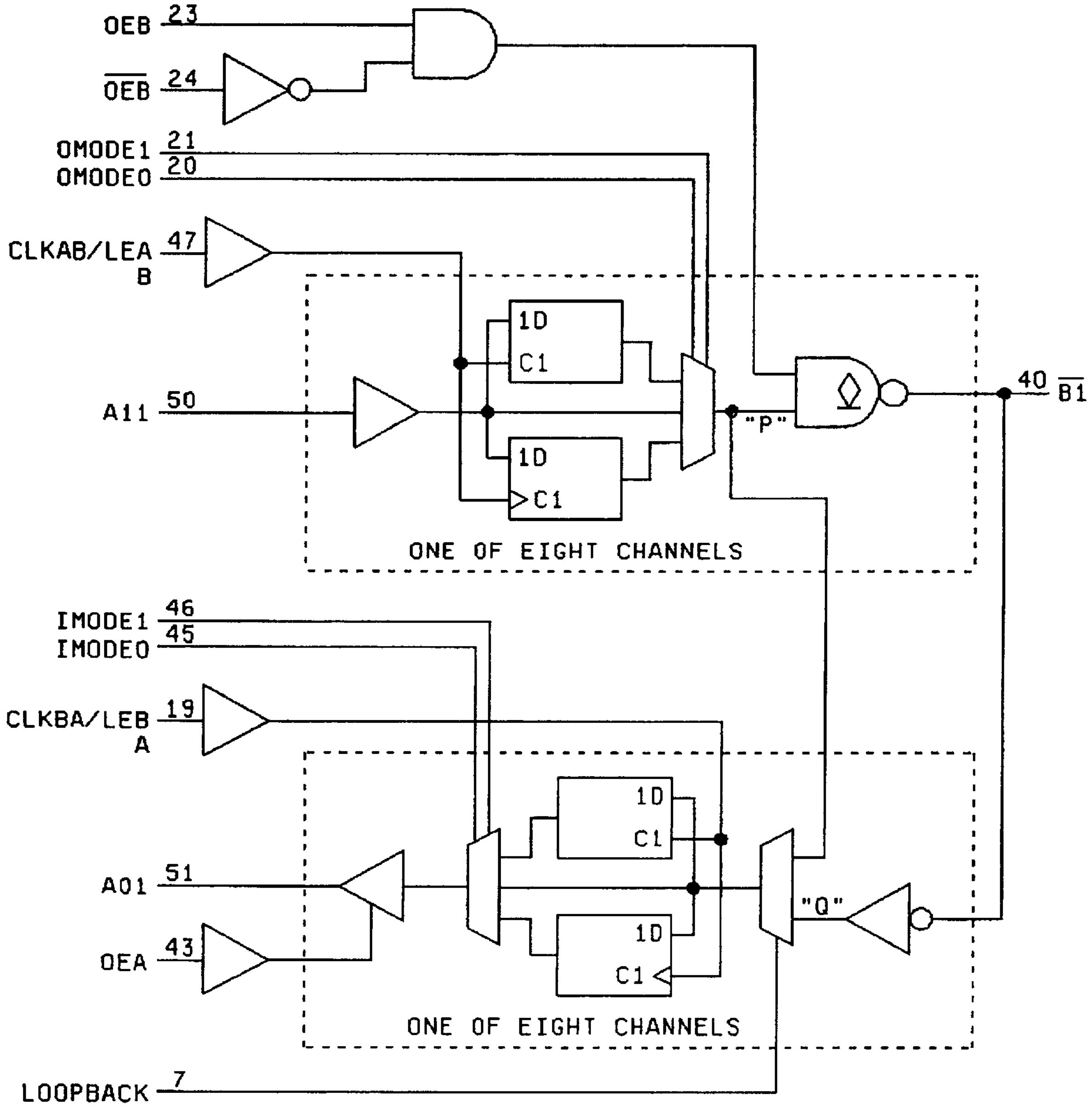


FIGURE 2. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-94574
		REVISION LEVEL	SHEET 12

ENABLE/DISABLE

Inputs			Outputs	
OEA	OEB	$\overline{OEB}$	AO	$\overline{B}$
L	X	X	Z	
H	X	X	Active (H or L)	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active (H or L)
X	H	H		Inactive (H)

Buffer

Input	Output
L	H
H	L

Latch

Inputs		Outputs
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

Loopback

Loopback	Q 1/
L	$\overline{B}$ Port
H	Point P 2/

Select

Inputs		Selected Logic Element
MODE 1	MODE 0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

notes:

1/ Q is the input to the B to A logic element.

2/ P is the output of the A to B logic element (see functional block diagram).

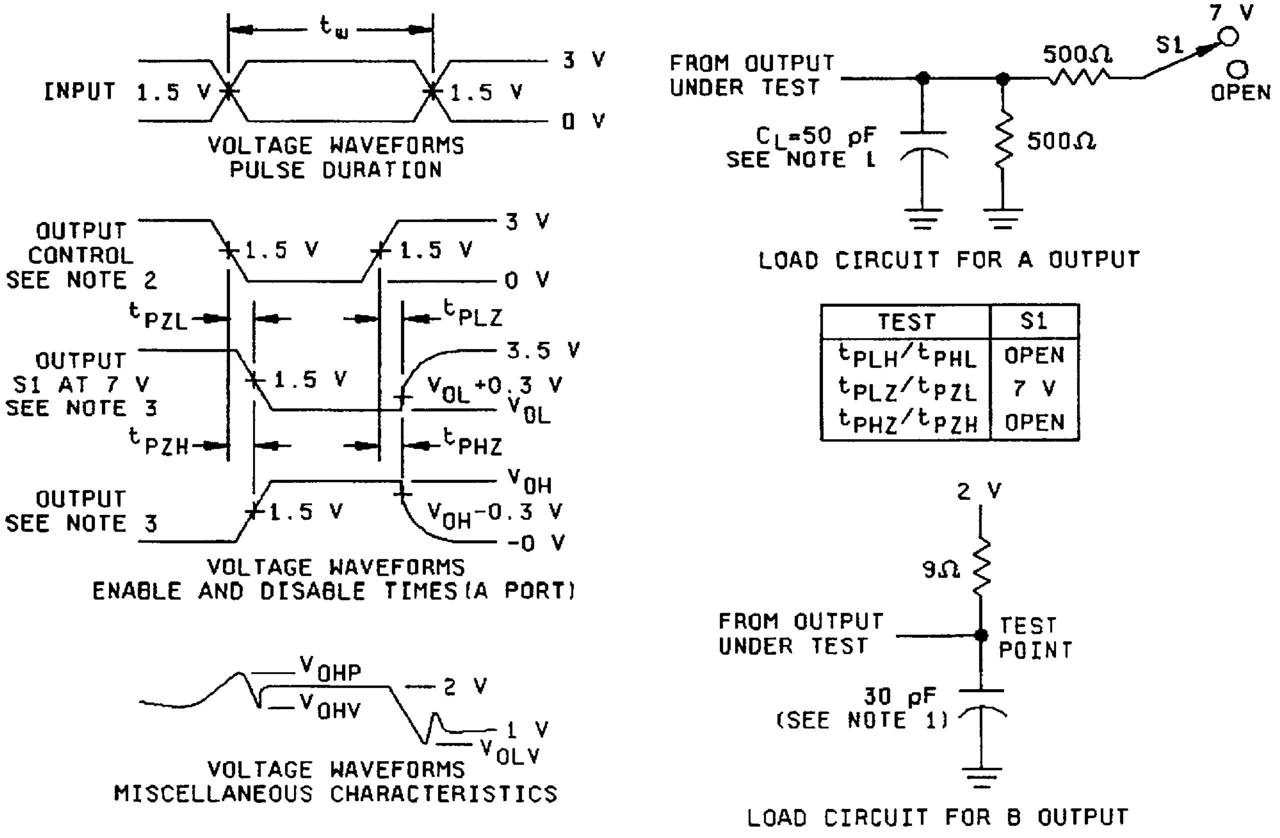
Figure 3. Truth table.

Flip-Flop

Inputs		Outputs
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

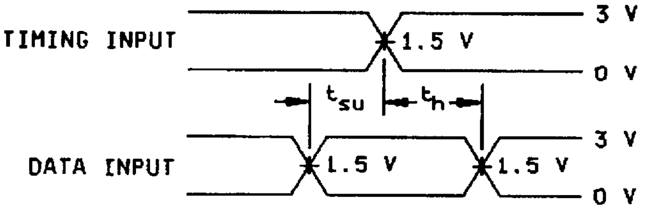
Inputs								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L L	L X	X H	X X	X X	X X	X X	X X	Isolation
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H H	L X	X H	X X	X X	L L	L L	L L	$\overline{B}$ to AO, buffer mode
H H	L X	X H	X X	X X	L L	H H	L L	$\overline{B}$ to AO, flip flop mode
H H	L X	X H	X X	X X	H H	X X	L L	$\overline{B}$ to AO latch mode
H H	L X	X H	X X	X X	L L	L L	H H	AI to AO buffer mode
H H	L X	X H	X X	X X	L L	H H	H H	AI to AO flip-flop mode
H H	L X	X H	X X	X X	H H	X X	H H	AI to AO, latch mode
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

Figure 3. Truth table - Continued.

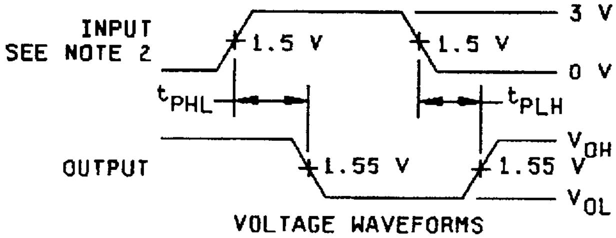


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	OPEN

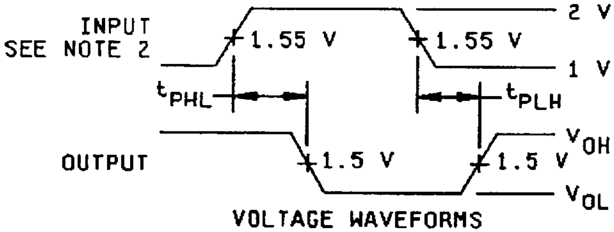
FIGURE 4. Timing waveforms.



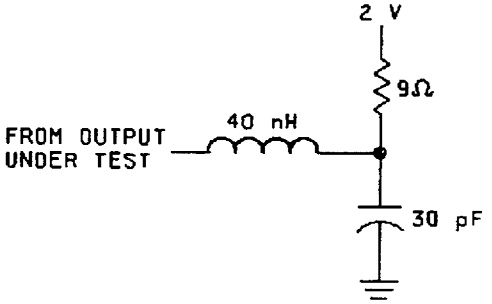
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES(A TO B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES(B TO A)



LOAD CIRCUIT V_{OHP}, V_{OHV}

FIGURE 4. Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		5962-94574
		REVISION LEVEL	SHEET 16

DESC FORM 193A
JUL 94

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality fo the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 7, 8 1/ 9, 10, 11	1, 2, 3, 7 2/ 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8 9, 10, 11	1, 2, 3, 4, 7, 8 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.