Preliminary

82-common X 128RGB-Segment, in 256-Color STN LCD DRIVER

■ GENERAL DESCRIPTION

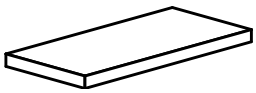
The **NJU6821** is a STN LCD driver with 82-common x 128RGB-segment in 256-color. It consists of 384(128xRGB)-segment, 82-common drivers, and serial and parallel MPU interface circuits, internal power supply circuits, gradation palettes and 81,920-bit for graphic and 2,048-bit for icon display data RAM.

Each segment driver outputs 8-(for R and G) and 4-(for B) gradation level out of 32-gradation level of gradation palette.

Since the **NJU6821** provides a low operating voltage of 1.7V and low operating current, it is ideally suited for battery-powered handheld applications.

In addition, it is possible to drive up to 164 x 128 pixels LCD panel when use two of **NJU6821** as a master and slave LSIs.

■ PACKAGE OUTLINE



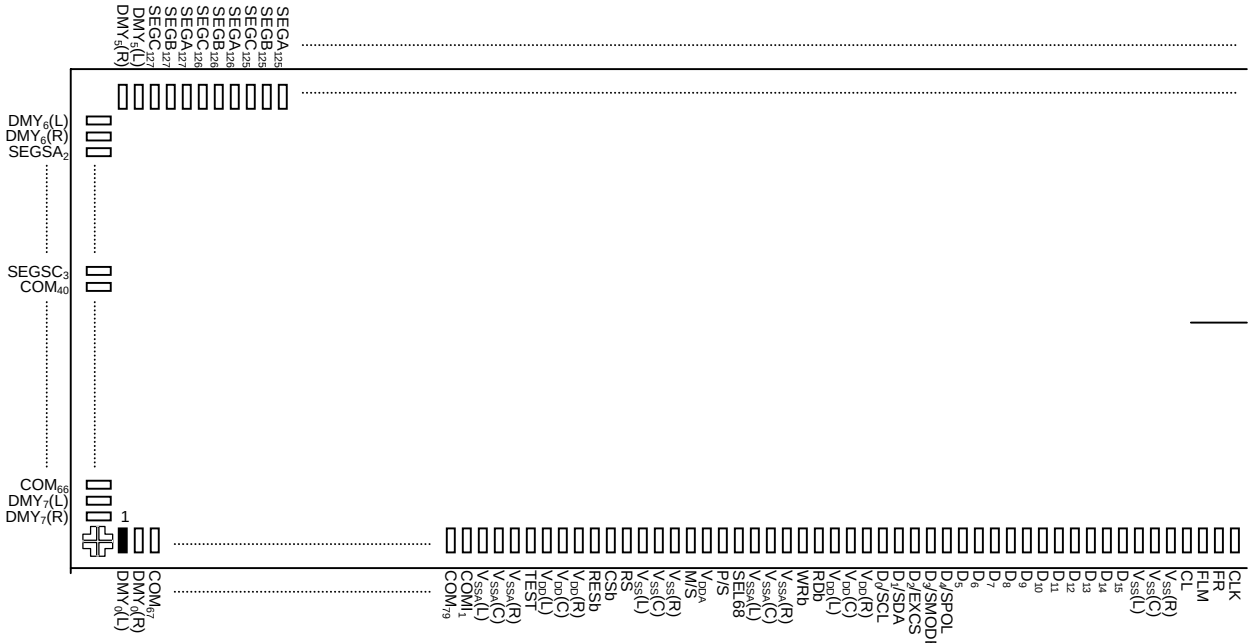
NJU6821CJ

■ FEATURES

- 256-color STN LCD driver
- LCD drivers 80 and 2-icon commons, 128RGB-segments, 4RGB-icon segments
- Display data RAM (DDRAM) 81,920-bit for graphic display
  2,048-bit for icon display
- Color display mode 8-(R and G) or 4-(B) gradation level out of 32-gradation level of gradation palette
- Black & white display mode 82 x 384 pixels in B&W
- 8/16bit Parallel interface directly- connective to 68/80 series MPU
- Programmable 8- or 16-bit data bus length for display data
- 3-/4-line Serial interface
- Programmable duty and bias ratios
- Programmable internal voltage booster (Maximum 7-times)
- Programmable contrast control using 128-step EVR
- Various instructions
  Display data read/write, Display ON/OFF, Reverse display ON/OFF, All pixels ON/OFF, column address, row address, N-line inversion, Initial display line, Initial COM line, Read-modify-write, Gradation mode control, Increment control, Data bus length, Discharge ON/OFF, Duty cycle ratio, LCD bias ratio, Boost level, EVR control, Power save ON/OFF, etc
- Low operating current
- Low logic supply voltage 1.7V to 3.3V
- LCD driving supply voltage 5.0V to 18.0V
- C-MOS process
- Package Bumped chip / TCP

2002/11/22

■ PAD LOCATION

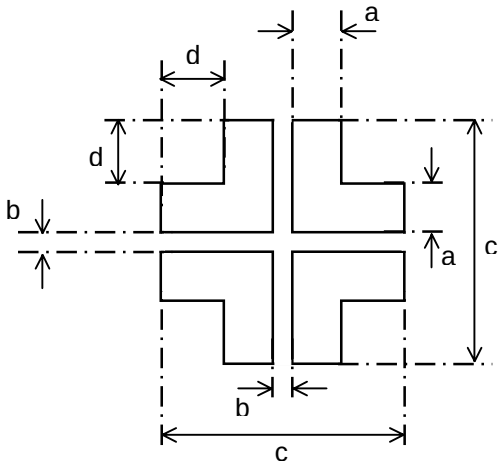


Note1) The PADs of (L), (R) and (C) are shorted mutually in the LSI.
Note2) The DMY PADs are electrically open.

Chip Center	:X= 0µm, Y= 0µm
Chip Size	:19.91mm x 2.55mm
Chip Thickness	:625µm ± 25µm
Bump Size	:100µm x 32µm
Bump Pitch	:50µm(Min)
Bump Height	:14.0~22.5µm (Typical 18µm) <tolerance : ±3µm >
Bump Material	:Au

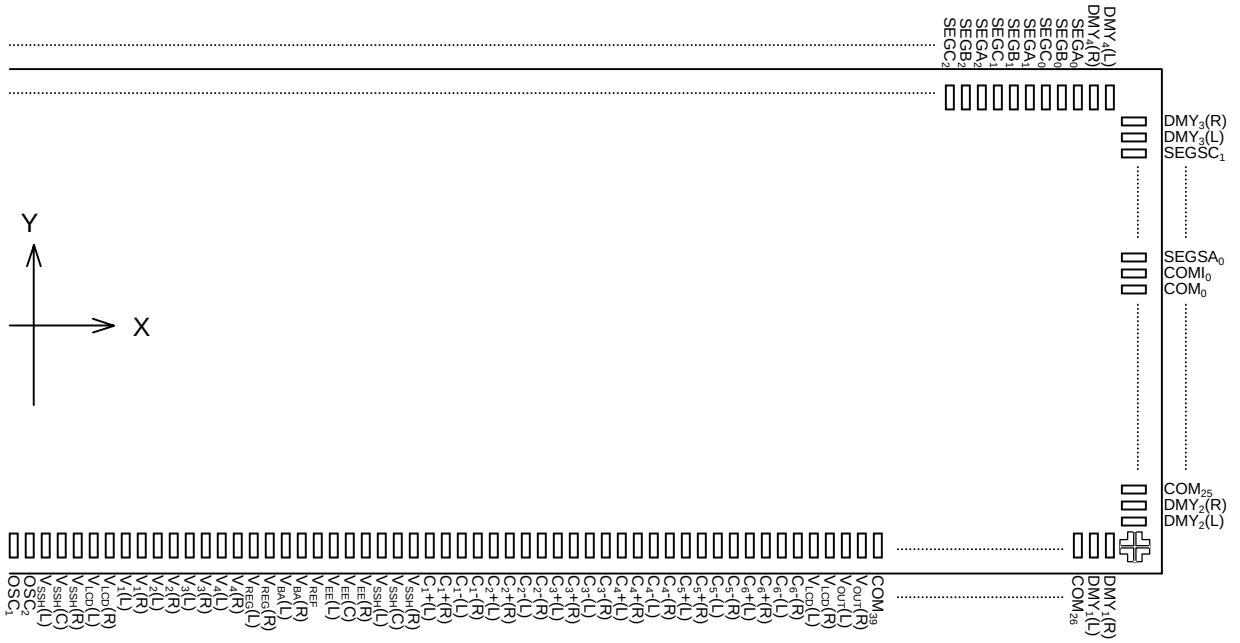
Alignment marks

a: 30µm
b: 6µm
c: 120µm
d: 27µm



Alignment mark coordinates

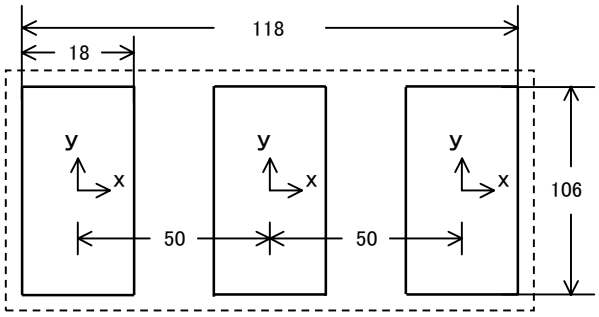
X=-9732µm, Y=-1052µm
X= 9732µm, Y=-1052µm



PAD size

V_{SSA}, V_{SS}, V_{DD}, V_{SSH}, V_{EE}, V_{OUT} PADs types

17to19, 21to23, 29to31, 37to39, 43to45, 77to79, 91to93, 109to111, 112to114, 140to142



■ PAD COORDINATES 1

Chip Size 19910μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
1	DMY_0(L)	-9625	-1068	52	D_{10}	-2550	-1068	103	C_4+(L)	6120	-1068
2	DMY_0(R)	-9575	-1068	53	D_{11}	-2380	-1068	104	C_4+(R)	6290	-1068
3	COM_{67}	-9525	-1068	54	D_{12}	-2210	-1068	105	C_4-(L)	6460	-1068
4	COM_{68}	-9475	-1068	55	D_{13}	-2040	-1068	106	C_4-(R)	6630	-1068
5	COM_{69}	-9425	-1068	56	D_{14}	-1870	-1068	107	C_5+(L)	6800	-1068
6	COM_{70}	-9375	-1068	57	D_{15}	-1700	-1068	108	C_5+(R)	6970	-1068
7	COM_{71}	-9325	-1068	58	V_{SS}(L)	-1472	-1068	109	C_5-(L)	7140	-1068
8	COM_{72}	-9275	-1068	59	V_{SS}(C)	-1340	-1068	110	C_5-(R)	7310	-1068
9	COM_{73}	-9225	-1068	60	V_{SS}(R)	-1190	-1068	111	C_6+(L)	7480	-1068
10	COM_{74}	-9175	-1068	61	CL	-1020	-1068	112	C_6+(R)	7650	-1068
11	COM_{75}	-9125	-1068	62	FLM	-850	-1068	113	C_6-(L)	7820	-1068
12	COM_{76}	-9075	-1068	63	FR	-680	-1068	114	C_6-(R)	7990	-1068
13	COM_{77}	-9025	-1068	64	CLK	-510	-1068	115	V_{LCD}(L)	8160	-1068
14	COM_{78}	-8975	-1068	65	OSC_1	-340	-1068	116	V_{LCD}(R)	8330	-1068
15	COM_{79}	-8925	-1068	66	OSC_2	-107	-1068	117	V_{OUT}(L)	8500	-1068
16	$COMI_1$	-8875	-1068	67	V_{SSH}(L)	74	-1068	118	V_{OUT}(R)	8670	-1068
17	V_{SSA}(L)	-8670	-1068	68	V_{SSH}(C)	196	-1068	119	COM_{39}	8875	-1068
18	V_{SSA}(C)	-8500	-1068	69	V_{SSH}(R)	318	-1068	120	COM_{38}	8925	-1068
19	V_{SSA}(R)	-8330	-1068	70	V_{LCD}(L)	510	-1068	121	COM_{37}	8975	-1068
20	TEST	-8171	-1068	71	V_{LCD}(R)	680	-1068	122	COM_{36}	9025	-1068
21	V_{DD}(L)	-7990	-1068	72	V_1(L)	850	-1068	123	COM_{35}	9075	-1068
22	V_{DD}(C)	-7820	-1068	73	V_1(R)	1020	-1068	124	COM_{34}	9125	-1068
23	V_{DD}(R)	-7650	-1068	74	V_2(L)	1190	-1068	125	COM_{33}	9175	-1068
24	RESb	-7480	-1068	75	V_2(R)	1360	-1068	126	COM_{32}	9225	-1068
25	CSb	-7310	-1068	76	V_3(L)	1530	-1068	127	COM_{31}	9275	-1068
26	RS	-7140	-1068	77	V_3(R)	1700	-1068	128	COM_{30}	9325	-1068
27	V_{SS}(L)	-6970	-1068	78	V_4(L)	1870	-1068	129	COM_{29}	9375	-1068
28	V_{SS}(C)	-6800	-1068	79	V_4(R)	2040	-1068	130	COM_{28}	9425	-1068
29	V_{SS}(R)	-6630	-1068	80	V_{REG}(L)	2210	-1068	131	COM_{27}	9475	-1068
30	M/S	-6448	-1068	81	V_{REG}(R)	2380	-1068	132	COM_{26}	9525	-1068
31	V_{DDA}	-6290	-1068	82	V_{BA}(L)	2550	-1068	133	DMY_1(L)	9575	-1068
32	P/S	-6120	-1068	83	V_{BA}(R)	2693	-1068	134	DMY_1(R)	9625	-1068
33	SEL68	-5950	-1068	84	V_{REF}	2879	-1068	135	DMY_2(L)	9726	-900
34	V_{SSA}(L)	-5780	-1068	85	V_{EE}(L)	3060	-1068	136	DMY_2(R)	9726	-850
35	V_{SSA}(C)	-5610	-1068	86	V_{EE}(C)	3230	-1068	137	COM_{25}	9726	-800
36	V_{SSA}(R)	-5440	-1068	87	V_{EE}(R)	3400	-1068	138	COM_{24}	9726	-750
37	WRb	-5270	-1068	88	V_{SSH}(L)	3570	-1068	139	COM_{23}	9726	-700
38	RDb	-5111	-1068	89	V_{SSH}(C)	3740	-1068	140	COM_{22}	9726	-650
39	V_{DD}(L)	-4930	-1068	90	V_{SSH}(R)	3910	-1068	141	COM_{21}	9726	-600
40	V_{DD}(C)	-4760	-1068	91	C_1+(L)	4102	-1068	142	COM_{20}	9726	-550
41	V_{DD}(R)	-4590	-1068	92	C_1+(R)	4250	-1068	143	COM_{19}	9726	-500
42	D_0/SCL	-4420	-1068	93	C_1-(L)	4420	-1068	144	COM_{18}	9726	-450
43	D_1/SDA	-4250	-1068	94	C_1-(R)	4590	-1068	145	COM_{17}	9726	-400
44	D_2/EXCS	-3995	-1068	95	C_2+(L)	4760	-1068	146	COM_{16}	9726	-350
45	D_3/SMODE	-3740	-1068	96	C_2+(R)	4930	-1068	147	COM_{15}	9726	-300
46	D_4/SPOL	-3570	-1068	97	C_2-(L)	5100	-1068	148	COM_{14}	9726	-250
47	D_5	-3400	-1068	98	C_2-(R)	5270	-1068	149	COM_{13}	9726	-200
48	D_6	-3230	-1068	99	C_3+(L)	5440	-1068	150	COM_{12}	9726	-150
49	D_7	-3060	-1068	100	C_3+(R)	5610	-1068	151	COM_{11}	9726	-100
50	D_8	-2890	-1068	101	C_3-(L)	5780	-1068	152	COM_{10}	9726	-50
51	D_9	-2720	-1068	102	C_3-(R)	5950	-1068	153	COM_9	9726	0

■ PAD COORDINATES 2

Chip Size 19910µm x 2550µm (Chip Center 0µm x 0µm)

PAD No.	Terminal	X(µm)	Y(µm)	PAD No.	Terminal	X (µm)	Y (µm)	PAD No.	Terminal	X (µm)	Y (µm)
154	COM_8	9726	50	205	$SEGB_{10}$	8025	1068	256	$SEGB_{27}$	5475	1068
155	COM_7	9726	100	206	$SEGC_{10}$	7975	1068	257	$SEGC_{27}$	5425	1068
156	COM_6	9726	150	207	$SEGA_{11}$	7925	1068	258	$SEGA_{28}$	5375	1068
157	COM_5	9726	200	208	$SEGB_{11}$	7875	1068	259	$SEGB_{28}$	5325	1068
158	COM_4	9726	250	209	$SEGC_{11}$	7825	1068	260	$SEGC_{28}$	5275	1068
159	COM_3	9726	300	210	$SEGA_{12}$	7775	1068	261	$SEGA_{29}$	5225	1068
160	COM_2	9726	350	211	$SEGB_{12}$	7725	1068	262	$SEGB_{29}$	5175	1068
161	COM_1	9726	400	212	$SEGC_{12}$	7675	1068	263	$SEGC_{29}$	5125	1068
162	COM_0	9726	450	213	$SEGA_{13}$	7625	1068	264	$SEGA_{30}$	5075	1068
163	$COMI_0$	9726	500	214	$SEGB_{13}$	7575	1068	265	$SEGB_{30}$	5025	1068
164	$SEGSA_0$	9726	550	215	$SEGC_{13}$	7525	1068	266	$SEGC_{30}$	4975	1068
165	$SEGSB_0$	9726	600	216	$SEGA_{14}$	7475	1068	267	$SEGA_{31}$	4925	1068
166	$SEGSC_0$	9726	650	217	$SEGB_{14}$	7425	1068	268	$SEGB_{31}$	4875	1068
167	$SEGSA_1$	9726	700	218	$SEGC_{14}$	7375	1068	269	$SEGC_{31}$	4825	1068
168	$SEGSB_1$	9726	750	219	$SEGA_{15}$	7325	1068	270	$SEGA_{32}$	4775	1068
169	$SEGSC_1$	9726	800	220	$SEGB_{15}$	7275	1068	271	$SEGB_{32}$	4725	1068
170	DMY_3(L)	9726	850	221	$SEGC_{15}$	7225	1068	272	$SEGC_{32}$	4675	1068
171	DMY_3(R)	9726	900	222	$SEGA_{16}$	7175	1068	273	$SEGA_{33}$	4625	1068
172	DMY_4(L)	9675	1068	223	$SEGB_{16}$	7125	1068	274	$SEGB_{33}$	4575	1068
173	DMY_4(R)	9625	1068	224	$SEGC_{16}$	7075	1068	275	$SEGC_{33}$	4525	1068
174	$SEGA_0$	9575	1068	225	$SEGA_{17}$	7025	1068	276	$SEGA_{34}$	4475	1068
175	$SEGB_0$	9525	1068	226	$SEGB_{17}$	6975	1068	277	$SEGB_{34}$	4425	1068
176	$SEGC_0$	9475	1068	227	$SEGC_{17}$	6925	1068	278	$SEGC_{34}$	4375	1068
177	$SEGA_1$	9425	1068	228	$SEGA_{18}$	6875	1068	279	$SEGA_{35}$	4325	1068
178	$SEGB_1$	9375	1068	229	$SEGB_{18}$	6825	1068	280	$SEGB_{35}$	4275	1068
179	$SEGC_1$	9325	1068	230	$SEGC_{18}$	6775	1068	281	$SEGC_{35}$	4225	1068
180	$SEGA_2$	9275	1068	231	$SEGA_{19}$	6725	1068	282	$SEGA_{36}$	4175	1068
181	$SEGB_2$	9225	1068	232	$SEGB_{19}$	6675	1068	283	$SEGB_{36}$	4125	1068
182	$SEGC_2$	9175	1068	233	$SEGC_{19}$	6625	1068	284	$SEGC_{36}$	4075	1068
183	$SEGA_3$	9125	1068	234	$SEGA_{20}$	6575	1068	285	$SEGA_{37}$	4025	1068
184	$SEGB_3$	9075	1068	235	$SEGB_{20}$	6525	1068	286	$SEGB_{37}$	3975	1068
185	$SEGC_3$	9025	1068	236	$SEGC_{20}$	6475	1068	287	$SEGC_{37}$	3925	1068
186	$SEGA_4$	8975	1068	237	$SEGA_{21}$	6425	1068	288	$SEGA_{38}$	3875	1068
187	$SEGB_4$	8925	1068	238	$SEGB_{21}$	6375	1068	289	$SEGB_{38}$	3825	1068
188	$SEGC_4$	8875	1068	239	$SEGC_{21}$	6325	1068	290	$SEGC_{38}$	3775	1068
189	$SEGA_5$	8825	1068	240	$SEGA_{22}$	6275	1068	291	$SEGA_{39}$	3725	1068
190	$SEGB_5$	8775	1068	241	$SEGB_{22}$	6225	1068	292	$SEGB_{39}$	3675	1068
191	$SEGC_5$	8725	1068	242	$SEGC_{22}$	6175	1068	293	$SEGC_{39}$	3625	1068
192	$SEGA_6$	8675	1068	243	$SEGA_{23}$	6125	1068	294	$SEGA_{40}$	3575	1068
193	$SEGB_6$	8625	1068	244	$SEGB_{23}$	6075	1068	295	$SEGB_{40}$	3525	1068
194	$SEGC_6$	8575	1068	245	$SEGC_{23}$	6025	1068	296	$SEGC_{40}$	3475	1068
195	$SEGA_7$	8525	1068	246	$SEGA_{24}$	5975	1068	297	$SEGA_{41}$	3425	1068
196	$SEGB_7$	8475	1068	247	$SEGB_{24}$	5925	1068	298	$SEGB_{41}$	3375	1068
197	$SEGC_7$	8425	1068	248	$SEGC_{24}$	5875	1068	299	$SEGC_{41}$	3325	1068
198	$SEGA_8$	8375	1068	249	$SEGA_{25}$	5825	1068	300	$SEGA_{42}$	3275	1068
199	$SEGB_8$	8325	1068	250	$SEGB_{25}$	5775	1068	301	$SEGB_{42}$	3225	1068
200	$SEGC_8$	8275	1068	251	$SEGC_{25}$	5725	1068	302	$SEGC_{42}$	3175	1068
201	$SEGA_9$	8225	1068	252	$SEGA_{26}$	5675	1068	303	$SEGA_{43}$	3125	1068
202	$SEGB_9$	8175	1068	253	$SEGB_{26}$	5625	1068	304	$SEGB_{43}$	3075	1068
203	$SEGC_9$	8125	1068	254	$SEGC_{26}$	5575	1068	305	$SEGC_{43}$	3025	1068
204	$SEGA_{10}$	8075	1068	255	$SEGA_{27}$	5525	1068	306	$SEGA_{44}$	2975	1068

■ PAD COORDINATES 3

Chip Size 19910µm x 2550µm (Chip Center 0µm x 0µm)

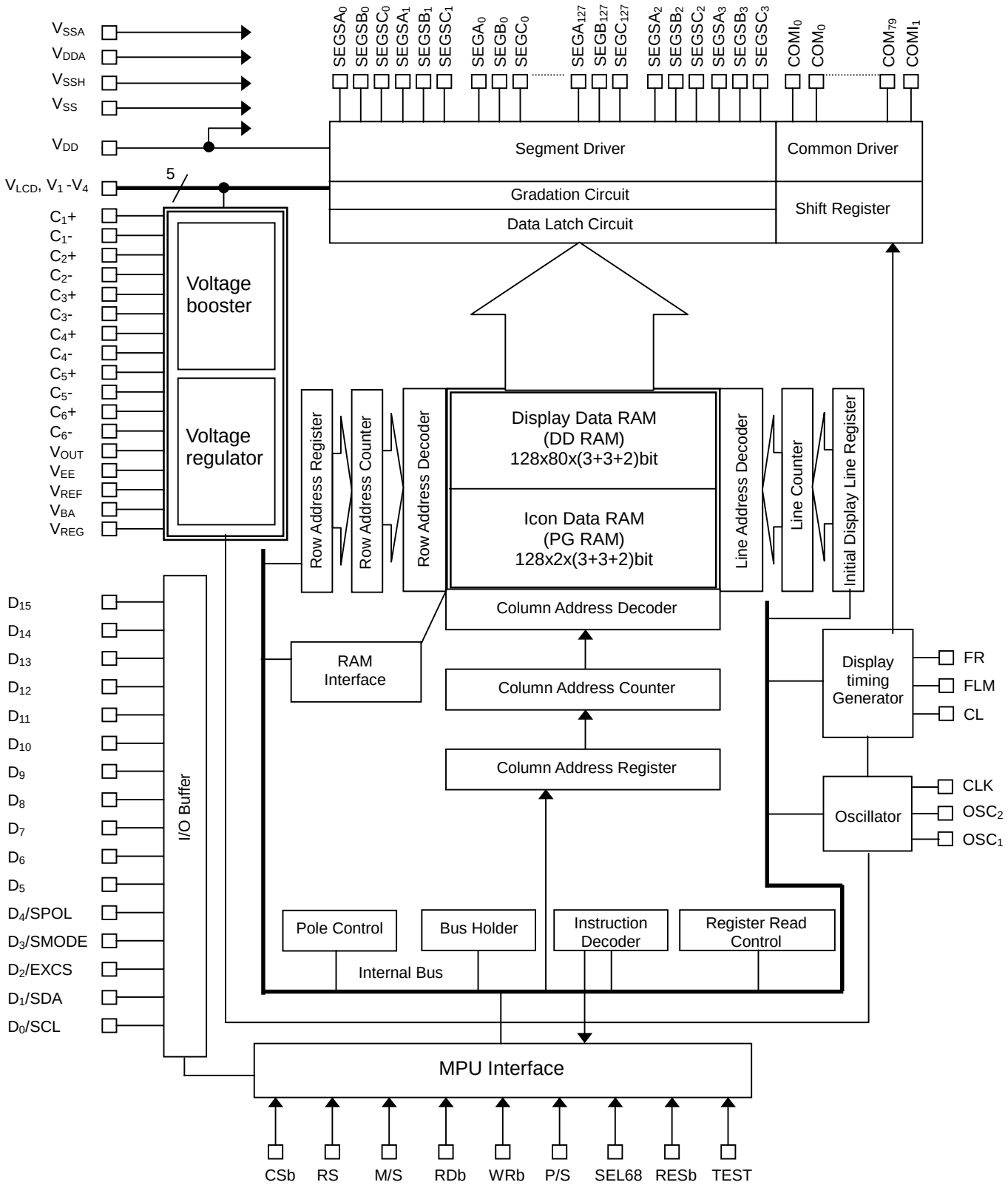
PAD No.	Terminal	X(µm)	Y(µm)	PAD No.	Terminal	X (µm)	Y (µm)	PAD No.	Terminal	X (µm)	Y (µm)
307	$SEGB_{44}$	2925	1068	358	$SEGB_{61}$	375	1068	409	$SEGB_{78}$	-2175	1068
308	$SEGC_{44}$	2875	1068	359	$SEGC_{61}$	325	1068	410	$SEGC_{78}$	-2225	1068
309	$SEGA_{45}$	2825	1068	360	$SEGA_{62}$	275	1068	411	$SEGA_{79}$	-2275	1068
310	$SEGB_{45}$	2775	1068	361	$SEGB_{62}$	225	1068	412	$SEGB_{79}$	-2325	1068
311	$SEGC_{45}$	2725	1068	362	$SEGC_{62}$	175	1068	413	$SEGC_{79}$	-2375	1068
312	$SEGA_{46}$	2675	1068	363	$SEGA_{63}$	125	1068	414	$SEGA_{80}$	-2425	1068
313	$SEGB_{46}$	2625	1068	364	$SEGB_{63}$	75	1068	415	$SEGB_{80}$	-2475	1068
314	$SEGC_{46}$	2575	1068	365	$SEGC_{63}$	25	1068	416	$SEGC_{80}$	-2525	1068
315	$SEGA_{47}$	2525	1068	366	$SEGA_{64}$	-25	1068	417	$SEGA_{81}$	-2575	1068
316	$SEGB_{47}$	2475	1068	367	$SEGB_{64}$	-75	1068	418	$SEGB_{81}$	-2625	1068
317	$SEGC_{47}$	2425	1068	368	$SEGC_{64}$	-125	1068	419	$SEGC_{81}$	-2675	1068
318	$SEGA_{48}$	2375	1068	369	$SEGA_{65}$	-175	1068	420	$SEGA_{82}$	-2725	1068
319	$SEGB_{48}$	2325	1068	370	$SEGB_{65}$	-225	1068	421	$SEGB_{82}$	-2775	1068
320	$SEGC_{48}$	2275	1068	371	$SEGC_{65}$	-275	1068	422	$SEGC_{82}$	-2825	1068
321	$SEGA_{49}$	2225	1068	372	$SEGA_{66}$	-325	1068	423	$SEGA_{83}$	-2875	1068
322	$SEGB_{49}$	2175	1068	373	$SEGB_{66}$	-375	1068	424	$SEGB_{83}$	-2925	1068
323	$SEGC_{49}$	2125	1068	374	$SEGC_{66}$	-425	1068	425	$SEGC_{83}$	-2975	1068
324	$SEGA_{50}$	2075	1068	375	$SEGA_{67}$	-475	1068	426	$SEGA_{84}$	-3025	1068
325	$SEGB_{50}$	2025	1068	376	$SEGB_{67}$	-525	1068	427	$SEGB_{84}$	-3075	1068
326	$SEGC_{50}$	1975	1068	377	$SEGC_{67}$	-575	1068	428	$SEGC_{84}$	-3125	1068
327	$SEGA_{51}$	1925	1068	378	$SEGA_{68}$	-625	1068	429	$SEGA_{85}$	-3175	1068
328	$SEGB_{51}$	1875	1068	379	$SEGB_{68}$	-675	1068	430	$SEGB_{85}$	-3225	1068
329	$SEGC_{51}$	1825	1068	380	$SEGC_{68}$	-725	1068	431	$SEGC_{85}$	-3275	1068
330	$SEGA_{52}$	1775	1068	381	$SEGA_{69}$	-775	1068	432	$SEGA_{86}$	-3325	1068
331	$SEGB_{52}$	1725	1068	382	$SEGB_{69}$	-825	1068	433	$SEGB_{86}$	-3375	1068
332	$SEGC_{52}$	1675	1068	383	$SEGC_{69}$	-875	1068	434	$SEGC_{86}$	-3425	1068
333	$SEGA_{53}$	1625	1068	384	$SEGA_{70}$	-925	1068	435	$SEGA_{87}$	-3475	1068
334	$SEGB_{53}$	1575	1068	385	$SEGB_{70}$	-975	1068	436	$SEGB_{87}$	-3525	1068
335	$SEGC_{53}$	1525	1068	386	$SEGC_{70}$	-1025	1068	437	$SEGC_{87}$	-3575	1068
336	$SEGA_{54}$	1475	1068	387	$SEGA_{71}$	-1075	1068	438	$SEGA_{88}$	-3625	1068
337	$SEGB_{54}$	1425	1068	388	$SEGB_{71}$	-1125	1068	439	$SEGB_{88}$	-3675	1068
338	$SEGC_{54}$	1375	1068	389	$SEGC_{71}$	-1175	1068	440	$SEGC_{88}$	-3725	1068
339	$SEGA_{55}$	1325	1068	390	$SEGA_{72}$	-1225	1068	441	$SEGA_{89}$	-3775	1068
340	$SEGB_{55}$	1275	1068	391	$SEGB_{72}$	-1275	1068	442	$SEGB_{89}$	-3825	1068
341	$SEGC_{55}$	1225	1068	392	$SEGC_{72}$	-1325	1068	443	$SEGC_{89}$	-3875	1068
342	$SEGA_{56}$	1175	1068	393	$SEGA_{73}$	-1375	1068	444	$SEGA_{90}$	-3925	1068
343	$SEGB_{56}$	1125	1068	394	$SEGB_{73}$	-1425	1068	445	$SEGB_{90}$	-3975	1068
344	$SEGC_{56}$	1075	1068	395	$SEGC_{73}$	-1475	1068	446	$SEGC_{90}$	-4025	1068
345	$SEGA_{57}$	1025	1068	396	$SEGA_{74}$	-1525	1068	447	$SEGA_{91}$	-4075	1068
346	$SEGB_{57}$	975	1068	397	$SEGB_{74}$	-1575	1068	448	$SEGB_{91}$	-4125	1068
347	$SEGC_{57}$	925	1068	398	$SEGC_{74}$	-1625	1068	449	$SEGC_{91}$	-4175	1068
348	$SEGA_{58}$	875	1068	399	$SEGA_{75}$	-1675	1068	450	$SEGA_{92}$	-4225	1068
349	$SEGB_{58}$	825	1068	400	$SEGB_{75}$	-1725	1068	451	$SEGB_{92}$	-4275	1068
350	$SEGC_{58}$	775	1068	401	$SEGC_{75}$	-1775	1068	452	$SEGC_{92}$	-4325	1068
351	$SEGA_{59}$	725	1068	402	$SEGA_{76}$	-1825	1068	453	$SEGA_{93}$	-4375	1068
352	$SEGB_{59}$	675	1068	403	$SEGB_{76}$	-1875	1068	454	$SEGB_{93}$	-4425	1068
353	$SEGC_{59}$	625	1068	404	$SEGC_{76}$	-1925	1068	455	$SEGC_{93}$	-4475	1068
354	$SEGA_{60}$	575	1068	405	$SEGA_{77}$	-1975	1068	456	$SEGA_{94}$	-4525	1068
355	$SEGB_{60}$	525	1068	406	$SEGB_{77}$	-2025	1068	457	$SEGB_{94}$	-4575	1068
356	$SEGC_{60}$	475	1068	407	$SEGC_{77}$	-2075	1068	458	$SEGC_{94}$	-4625	1068
357	$SEGA_{61}$	425	1068	408	$SEGA_{78}$	-2125	1068	459	$SEGA_{95}$	-4675	1068

■ PAD COORDINATES 4

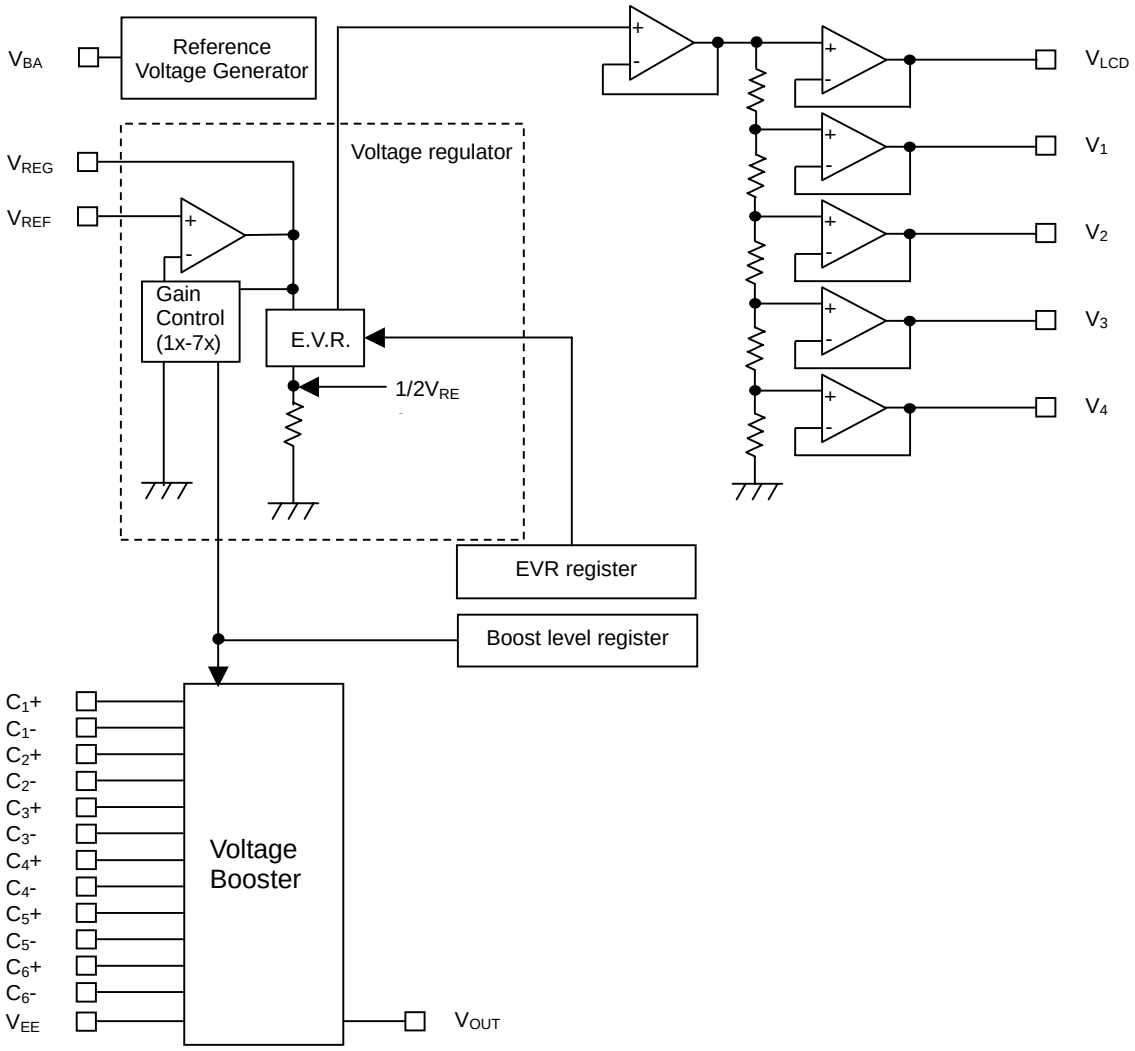
Chip Size 19910μm x 2550μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X (μm)	Y (μm)	PAD No.	Terminal	X (μm)	Y (μm)
460	$SEGB_{95}$	-4725	1068	511	$SEGB_{112}$	-7275	1068	562	$SEGSA_2$	-9726	800
461	$SEGC_{95}$	-4775	1068	512	$SEGC_{112}$	-7325	1068	563	$SEGSB_2$	-9726	750
462	$SEGA_{96}$	-4825	1068	513	$SEGA_{113}$	-7375	1068	564	$SEGSC_2$	-9726	700
463	$SEGB_{96}$	-4875	1068	514	$SEGB_{113}$	-7425	1068	565	$SEGSA_3$	-9726	650
464	$SEGC_{96}$	-4925	1068	515	$SEGC_{113}$	-7475	1068	566	$SEGSB_3$	-9726	600
465	$SEGA_{97}$	-4975	1068	516	$SEGA_{114}$	-7525	1068	567	$SEGSC_3$	-9726	550
466	$SEGB_{97}$	-5025	1068	517	$SEGB_{114}$	-7575	1068	568	COM_{40}	-9726	500
467	$SEGC_{97}$	-5075	1068	518	$SEGC_{114}$	-7625	1068	569	COM_{41}	-9726	450
468	$SEGA_{98}$	-5125	1068	519	$SEGA_{115}$	-7675	1068	570	COM_{42}	-9726	400
469	$SEGB_{98}$	-5175	1068	520	$SEGB_{115}$	-7725	1068	571	COM_{43}	-9726	350
470	$SEGC_{98}$	-5225	1068	521	$SEGC_{115}$	-7775	1068	572	COM_{44}	-9726	300
471	$SEGA_{99}$	-5275	1068	522	$SEGA_{116}$	-7825	1068	573	COM_{45}	-9726	250
472	$SEGB_{99}$	-5325	1068	523	$SEGB_{116}$	-7875	1068	574	COM_{46}	-9726	200
473	$SEGC_{99}$	-5375	1068	524	$SEGC_{116}$	-7925	1068	575	COM_{47}	-9726	150
474	$SEGA_{100}$	-5425	1068	525	$SEGA_{117}$	-7975	1068	576	COM_{48}	-9726	100
475	$SEGB_{100}$	-5475	1068	526	$SEGB_{117}$	-8025	1068	577	COM_{49}	-9726	50
476	$SEGC_{100}$	-5525	1068	527	$SEGC_{117}$	-8075	1068	578	COM_{50}	-9726	0
477	$SEGA_{101}$	-5575	1068	528	$SEGA_{118}$	-8125	1068	579	COM_{51}	-9726	-50
478	$SEGB_{101}$	-5625	1068	529	$SEGB_{118}$	-8175	1068	580	COM_{52}	-9726	-100
479	$SEGC_{101}$	-5675	1068	530	$SEGC_{118}$	-8225	1068	581	COM_{53}	-9726	-150
480	$SEGA_{102}$	-5725	1068	531	$SEGA_{119}$	-8275	1068	582	COM_{54}	-9726	-200
481	$SEGB_{102}$	-5775	1068	532	$SEGB_{119}$	-8325	1068	583	COM_{55}	-9726	-250
482	$SEGC_{102}$	-5825	1068	533	$SEGC_{119}$	-8375	1068	584	COM_{56}	-9726	-300
483	$SEGA_{103}$	-5875	1068	534	$SEGA_{120}$	-8425	1068	585	COM_{57}	-9726	-350
484	$SEGB_{103}$	-5925	1068	535	$SEGB_{120}$	-8475	1068	586	COM_{58}	-9726	-400
485	$SEGC_{103}$	-5975	1068	536	$SEGC_{120}$	-8525	1068	587	COM_{59}	-9726	-450
486	$SEGA_{104}$	-6025	1068	537	$SEGA_{121}$	-8575	1068	588	COM_{60}	-9726	-500
487	$SEGB_{104}$	-6075	1068	538	$SEGB_{121}$	-8625	1068	589	COM_{61}	-9726	-550
488	$SEGC_{104}$	-6125	1068	539	$SEGC_{121}$	-8675	1068	590	COM_{62}	-9726	-600
489	$SEGA_{105}$	-6175	1068	540	$SEGA_{122}$	-8725	1068	591	COM_{63}	-9726	-650
490	$SEGB_{105}$	-6225	1068	541	$SEGB_{122}$	-8775	1068	592	COM_{64}	-9726	-700
491	$SEGC_{105}$	-6275	1068	542	$SEGC_{122}$	-8825	1068	593	COM_{65}	-9726	-750
492	$SEGA_{106}$	-6325	1068	543	$SEGA_{123}$	-8875	1068	594	COM_{66}	-9726	-800
493	$SEGB_{106}$	-6375	1068	544	$SEGB_{123}$	-8925	1068	595	DMY_7(L)	-9726	-850
494	$SEGC_{106}$	-6425	1068	545	$SEGC_{123}$	-8975	1068	596	DMY_7(R)	-9726	-900
495	$SEGA_{107}$	-6475	1068	546	$SEGA_{124}$	-9025	1068				
496	$SEGB_{107}$	-6525	1068	547	$SEGB_{124}$	-9075	1068				
497	$SEGC_{107}$	-6575	1068	548	$SEGC_{124}$	-9125	1068				
498	$SEGA_{108}$	-6625	1068	549	$SEGA_{125}$	-9175	1068				
499	$SEGB_{108}$	-6675	1068	550	$SEGB_{125}$	-9225	1068				
500	$SEGC_{108}$	-6725	1068	551	$SEGC_{125}$	-9275	1068				
501	$SEGA_{109}$	-6775	1068	552	$SEGA_{126}$	-9325	1068				
502	$SEGB_{109}$	-6825	1068	553	$SEGB_{126}$	-9375	1068				
503	$SEGC_{109}$	-6875	1068	554	$SEGC_{126}$	-9425	1068				
504	$SEGA_{110}$	-6925	1068	555	$SEGA_{127}$	-9475	1068				
505	$SEGB_{110}$	-6975	1068	556	$SEGB_{127}$	-9525	1068				
506	$SEGC_{110}$	-7025	1068	557	$SEGC_{127}$	-9575	1068				
507	$SEGA_{111}$	-7075	1068	558	DMY_5(L)	-9625	1068				
508	$SEGB_{111}$	-7125	1068	559	DMY_5(R)	-9675	1068				
509	$SEGC_{111}$	-7175	1068	560	DMY_6(L)	-9726	900				
510	$SEGA_{112}$	-7225	1068	561	DMY_6(R)	-9726	850				

■ BLOCK DIAGRAM



■ POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function
21,22,23, 39,40,41	V_{DD}	Power	Power supply for logic circuits
27,28,29, 58,59,60	V_{SS}	Power	GND for logic circuits
67,68,69, 88,89,90	V_{SSH}	Power	GND for high voltage circuits
31	V_{DDA}	Power	This terminal is internally connected to the V_{DD} level. •This terminal is used to fix the selection terminals to the V_{DD} level. Note) Do not use this terminal for a main power supply.
17,18,19, 34,35,36	V_{SSA}	Power	This terminal is internally connected to the V_{SS} level. •This terminal is used to fix the selection terminals to the V_{SS} level. Note) Do not use this terminal for a main GND.
70,71,115,116 72,73 74,75 76,77 78,79	V_{LCD} V_1 V_2 V_3 V_4	Power/O	LCD driving voltages •When the internal voltage booster is not used, external LCD driving voltages (V_1 to V_4 and V_{LCD}) must be supplied on these terminals. And the external voltages must be maintained in the following relation. $V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}$ • When the internal voltage booster is used, the LCD driving voltages (V_1 to V_4 and V_{LCD}) are enabled by the "Power control" instruction in the master mode operation. The capacitors between the V_{SS} and these terminals are necessary.
91,92 93,94	C_1+ C_1-	O	Capacitor connection terminals for the voltage booster
95,96 97,98	C_2+ C_2-	O	Capacitor connection terminals for the voltage booster
99,100 101,102	C_3+ C_3-	O	Capacitor connection terminals or the voltage booster
103,104 105,106	C_4+ C_4-	O	Capacitor connection terminals for the voltage booster
107,108 109,110	C_5+ C_5-	O	Capacitor connection terminals for the voltage booster
111,112 113,114	C_6+ C_6-	O	Capacitor connection terminals for the voltage booster
82,83	V_{BA}	O	Output of the reference-voltage generator
84	V_{REF}	I	Input of the voltage regulator
85,86,87	V_{EE}	Power	Input of the voltage booster •This terminal is normally connected to the V_{DD} level.
117,118	V_{OUT}	Power/O	Output of the voltage booster Input for high voltage circuits in using external power supply
80,81	V_{REG}	O	Output of the voltage regulator
24	RESb	I	Reset Active "0"

■ TERMINAL DESCRIPTION 2

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>42</td><td>D_0/SCL</td><td>I/O</td><td rowspan="6">Parallel interface:
D_7 to D_0 : 8-bit bi-directional bus
•In the parallel interface mode (P/S=“1”), these terminals connect to 8-bit bi-directional MPU bus.

Serial interface:
SDA : serial data
SCL : serial clock
EXCS : extension chip-selection
SMODE : 3-/4-line serial interface mode selection
SPOL : RS polarity selection
(in the 3-line serial interface mode)

•In the 3-/4-line serial interface mode (P/S=“0”), the D_0 terminal is assigned to the SCL and the D_1 terminal to the SDA.
•In the 3-line serial interface mode, the D_4 terminal is assigned to the SPOL.
•Serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D_7, D_6…D_0, and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal.
•The SCL signal must be set to “0” after data transmissions or during non-access.</td></tr>
<tr><td>43</td><td>D_1/SDA</td><td>I/O</td></tr>
<tr><td>44</td><td>D_2/EXCS</td><td>I/O</td></tr>
<tr><td>45</td><td>D_3/SMODE</td><td>I/O</td></tr>
<tr><td>46</td><td>D_4/SPOL</td><td>I/O</td></tr>
<tr><td>47,48,49</td><td>D_5,D_6,D_7</td><td>I/O</td></tr>
<tr><td>50,51,52,53
54,55,56,57</td><td>D_8,D_9,D_{10},D_{11},
D_{12},D_{13},D_{14},D_{15}</td><td>I/O</td><td>8-bit bi-directional bus
•In the 16-bit data bus mode, these terminals are assigned to upper 8-bit data bus.
•In the serial interface mode or the 8-bit data bus mode of the parallel interface, these terminals must be fixed to “1” or “0”.</td></tr>
<tr><td>25</td><td>CSb</td><td>I</td><td>Chip select
Active “0”</td></tr>
<tr><td>26</td><td>RS</td><td>I</td><td>Resister select
•This signal distinguishes transferred data as an instruction or display data as follows.

<table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Distinct.</td><td>Instruction</td><td>Display data</td></tr></table></td></tr>
<tr><td>38</td><td>RDb (E)</td><td>I</td><td>80 series MPU interface (P/S=“1”, SEL68=“0”)
RDb signal. Active “0”.

68 series MPU interface (P/S=“1”, SEL68=“1”)
Enable signal. Active “1”.</td></tr>
<tr><td>37</td><td>WRb (R/W)</td><td>I</td><td>80 series MPU interface (P/S=“1”, SEL68=“0”)
WRb signal. Active “0”.

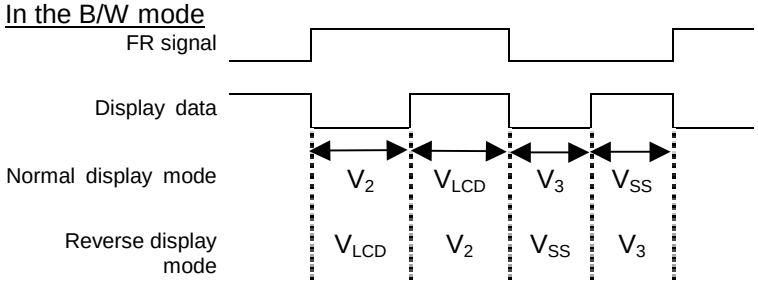
68 series MPU interface (P/S=“1”, SEL68=“1”)
R/W signal.

<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table></td></tr>
</table>

■ TERMINAL DESCRIPTION 3

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>33</td><td>SEL68</td><td>I</td><td>MPU interface type selection
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>Status</td><td>68 series</td><td>80 series</td></tr>
</table></td></tr>
<tr><td>32</td><td>P/S</td><td>I</td><td>Parallel / serial interface mode selection
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Instruction</td><td>Data</td><td>Read/Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>CSb</td><td>RS</td><td>D0~D7</td><td>RDb, WRb</td><td>-</td></tr>
<tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D1)</td><td>Write only</td><td>SCL (D0)</td></tr>
</table>
•Since the D_{15} to D_5 terminals are in the high impedance in the serial interface mode (P/S=“0”), they must be fixed to “1” or “0”. The RDb and WRb terminals also must be “1” or “0”.</td></tr>
<tr><td>20</td><td>TEST</td><td>I</td><td>Maker test terminal
This terminal should be fixed to “0”.</td></tr>
<tr><td>61</td><td>CL</td><td>I/O</td><td>LCD line clock
•This signal is used to count up the line counter and latch the display data into the data latch circuit.
•At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data output onto the segment drivers.
<table>
<tr><td>M/S</td><td>Status</td><td>CL</td></tr>
<tr><td>H</td><td>Master</td><td>Output</td></tr>
<tr><td>L</td><td>Slave</td><td>Input</td></tr>
</table></td></tr>
<tr><td>62</td><td>FLM</td><td>I/O</td><td>LCD frame maker signal
•This signal is used to indicate the start of a new display frame. It presets an initial display line address into the line counter when the FLM signal becomes “1”.
<table>
<tr><td>M/S</td><td>Status</td><td>FLM</td></tr>
<tr><td>H</td><td>Master</td><td>Output</td></tr>
<tr><td>L</td><td>Slave</td><td>Input</td></tr>
</table></td></tr>
<tr><td>63</td><td>FR</td><td>I/O</td><td>LCD alternate signal
•This signal is toggled to alternate the crystal polarization of a LCD panel. It can be programmed so that the FR signal will toggle at every frame or once every N frames in the N-line inversion mode.
<table>
<tr><td>M/S</td><td>Status</td><td>FR</td></tr>
<tr><td>H</td><td>Master</td><td>Output</td></tr>
<tr><td>L</td><td>Slave</td><td>Input</td></tr>
</table></td></tr>
<tr><td>30</td><td>M/S</td><td>I</td><td>Master / slave select
<table>
<tr><td>M/S</td><td>Status</td><td>Oscillator</td><td>Power supply</td></tr>
<tr><td>H</td><td>Master</td><td>Enable</td><td>Enable</td></tr>
<tr><td>L</td><td>Slave</td><td>Disable</td><td>Disable</td></tr>
</table></td></tr>
</table>

■ TERMINAL DESCRIPTION 4

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>174–557</td><td>$SEGA_0$-$SEGA_{127}$,
$SEGB_0$-$SEGB_{127}$,
$SEGC_0$-$SEGC_{127}$</td><td>O</td><td>Segment output
<table><tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and display data.
<u>In the B/W mode</u>
  </td></tr>
<tr><td>164–169,
562–567</td><td>$SEGSA_0$-$SEGSA_3$,
$SEGSB_0$-$SEGSB_3$,
$SEGSC_0$-$SEGSC_3$</td><td>O</td><td>Icon-segment output
•These terminals are assigned at both edge of normal segment output terminals line for out line frame display.</td></tr>
<tr><td>162–137,
132–119,
568–594,
3–15</td><td>COM_0-COM_{79}</td><td>O</td><td>Common output
•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data.
<table><tr><th>Data</th><th>FR</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>V_{SS}</td></tr><tr><td>L</td><td>H</td><td>V_1</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V_4</td></tr></table></td></tr>
<tr><td>163</td><td>$COMI_0$</td><td>O</td><td>Icon common output</td></tr>
<tr><td>16</td><td>$COMI_1$</td><td>O</td><td>Icon common output</td></tr>
<tr><td>65,
66</td><td>OSC_1
OSC_2</td><td>I
O</td><td>OSC
•When the internal oscillator clock is used in the master mode or when the LSI is used in the slave mode, these terminals must be opened. In these cases, the OSC_1 outputs the V_{SS} level.
•When an external oscillator is used, external clock is input to the OSC_1 terminal or an external resistor is connected between the OSC_1 and OSC_2 terminals.</td></tr>
<tr><td>64</td><td>CLK</td><td>I/O</td><td>Display timing synchronous clock
•This signal is used to synchronize the display timing between the master and slave LSIs.
<table><tr><th>M/S</th><th>Mode</th><th>CLK</th></tr><tr><td>H</td><td>Master</td><td>Output</td></tr><tr><td>L</td><td>Slave</td><td>Input</td></tr></table></td></tr>
</table>

(Terminal No. 1,2,133,134,135,136,170,171,172,173,558,559,560,561,595, and 596 are dummy.)

■ FUNCTIONAL DESCRIPTION

(1) MPU Interface

(1-1) Selection of parallel / serial interface mode

The P/S terminal is used to select parallel or serial interface mode as shown in the following table. In the serial interface mode, it is not possible to read out display data from the DDRAM, and status from the internal registers.

Table

P/S	P/S mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

Note 1) " -" : Fix to "1" or "0".

(1-2) Selection of MPU interface type

In the parallel interface mode, the SEL68 terminal is used to select 80- or 68-series MPU interface type, as shown in the following table.

Table

SEL68	MPU type	CSb	RS	RDb	WRb	Data
H	68 series MPU	CSb	RS	E	R/W	D7-D0 (D15-D0)
L	80 series MPU	CSb	RS	RDb	WRb	D7-D0 (D15-D0)

(1-3) Data distinction

In the parallel interface mode, the combination of RS, RDb, and WRb (R/W) signals distinguishes transferred data between the LSI and MPU as instruction or display data, as shown in the following table.

Table

RS	68 series	80 series		Function
	R/W	RDb	WRb	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) Selection of serial interface mode

In the serial interface mode, the SMODE terminal is used to select the 3- or 4-line serial interface mode as shown in the following table.

Table

SMODE	Serial interface mode
H	3-line
L	4-line

(1-5) 4-line serial interface mode

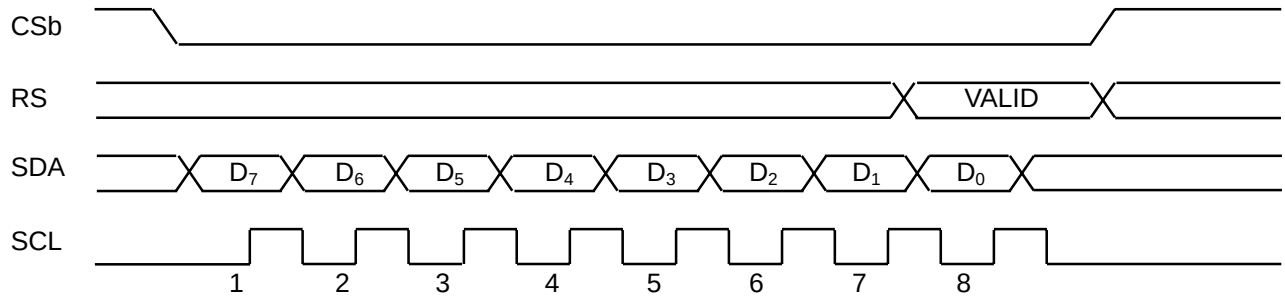
In the serial interface mode, when the chip select is active (CSb="0"), the SDA and the SCL are enabled. When the chip select is not active (CSb="1"), the SDA and the SCL are disabled, and the internal shift register and the counter are being initialized. The 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the D_7, D_6…D_0, and the fetched data is converted into the 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, the transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of the 8-bit data transmissions. The following figure illustrates the interface timing for the 4-line serial interface operation.



4-line serial interface timing

(1-6) 3-line serial interface mode

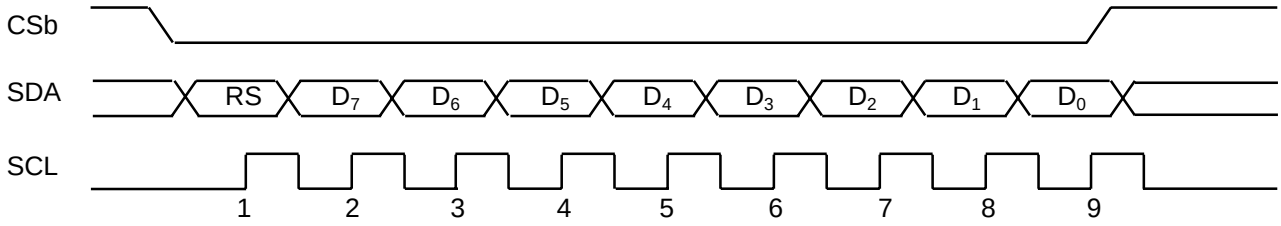
In the serial interface mode, when the chip select is active (CSb="0"), the SDA and SCL are enabled. When the chip select is not active (CSb="1"), the SDA and SCL are disabled and the internal shift register and counter are being initialized. 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, D_7, D_6…D_0, and the fetched data is converted into the 9-bit parallel data at the falling edge of the 9th SCL signal.

In the 3-line serial interface mode, data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of SDA data and the status of the SPOL, as follows.

Table

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

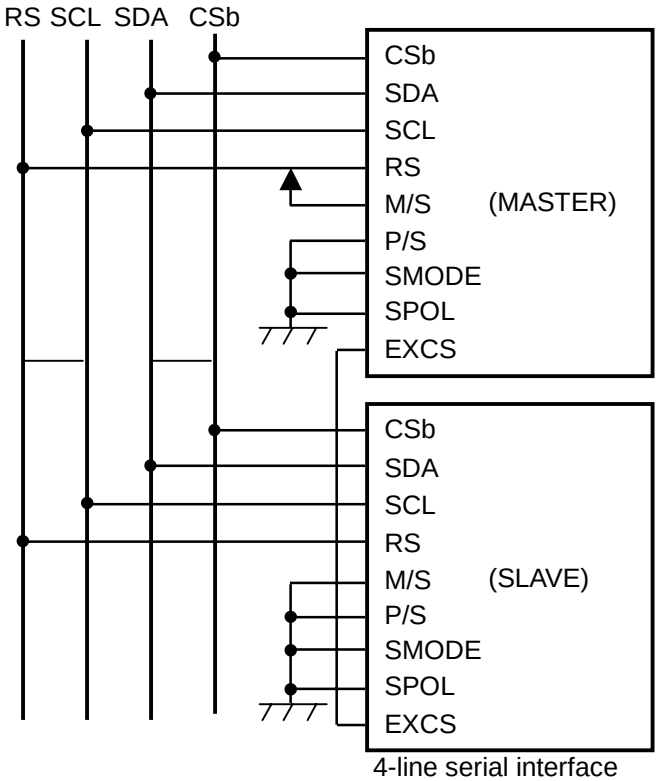
Since the serial interface operation is sensitive to external noises, the SCL must be set to “0” after data transmissions or during non-access. To release a malfunction caused by the external noises, the chip-selected status should be released (CSb=“1”) after each of 9-bit data transmissions. The following figure illustrates the interface timing of the 3-line serial interface operation.



3-line serial interface timing

(1-7) Unification of the CSb signals (in the serial interface mode)

When two of the **NJU6821** is used as a master and slave driver in the 3- or 4-line serial interface mode, both of the CSb signals can be notified using the EXCS terminals in order to simplify the control signals. In this time, the master’s EXCS is assigned to output and slave’s EXCS is assigned to input. The status of the EXCS signal is controlled by the “EXCS control” instruction.
of the master LSI.
During both of the EXCS and CSb are “0”, the slave LSI is enabled to accept instructions from MPU but the master LSI is disabled to accept any instruction except the “EXCS control” instruction. During the EXCS is “1” and CSb is “0”, the master LSI is enabled and the slave LSI is disabled.



4-line serial interface

EXCS: Extension CSb
EXCS=0, CSb=0: Slave LSI is enabled
EXCS=1,CSb=0: Master LSI is enabled

P/S: Parallel/serial interface mode select
P/S=0: Serial interface
P/S=1: Parallel interface

M/S: Master/slave select
M/S=0: Slave operation
M/S=1: Master operation

SMODE: 3-/4-line serial interface mode select
SMODE=0: 4-line serial interface
SMODE=1: 3-line serial interface

SPOL: RS polarity select
SPOL=0, RS=0: Display data
SPOL=0, RS=1: Instruction data
SPOL=1, RS=0: Instruction data
SPOL=1, RS=1: Display data

(In the 3-line serial interface mode)

(2) Access to the DDRAM

When the CSb signal is ”0”, the transferred data from MPU is written into the DDRAM or instruction register in accordance with the condition of the RS signal.

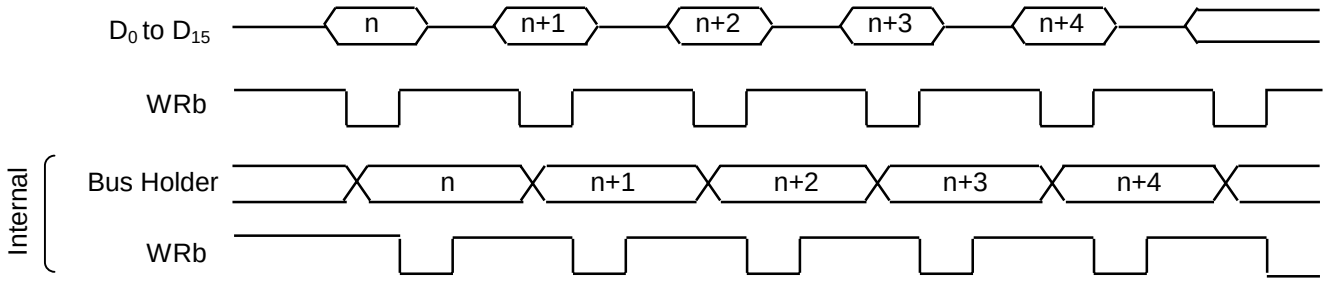
When the RS signal is “1”, the transferred data is distinguished as display data. After the “column address” and “row address” instructions are executed, the display data can be written into the DDRAM by the “display data write” instruction. The display data is written at the rising edge of the WRb signal in the 80 series MPU mode, or at the falling edge of the E signal in the 68 series MPU mode.

Table

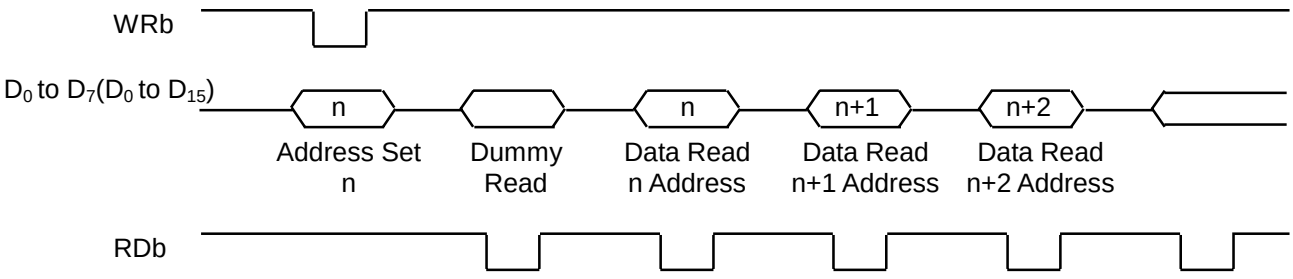
RS	Data distinction
H	Display RAM Data
L	Internal Command Register

In the sequence of the “display data read” operation, the transferred data from MPU is temporarily held in the internal bus-holder and then transferred to the internal data-bus. When the “display data read” operation is executed just after the “column address” and “row address” instructions or “display data write” instruction, unexpected data on the bus-holder is read out at the 1st execution, then the data of designated DDRAM address is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

- Display data write operation



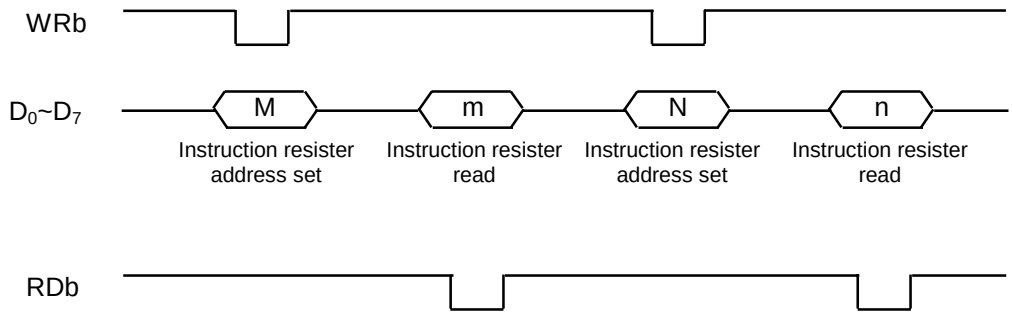
- Display data read operation



Note) In the 16-bit data bus mode, instruction data must be 16-bit as well as the display data.

(3) Access to the instruction register

Each of the instruction resisters is assigned to each address between 0_H and F_H and content of the instruction register can be read out by the combination of the “Instruction resister address” and ”Instruction resister read”.



(4) 8-/16-bit data bus length for display data (in the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the “WLS” of the “Data bus length” instruction.

In the 16-bit data bus mode, instruction data must be 16-bit (D_{15} to D_0) as well as display data. However, for the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table

WLS	Data bus length mode
L	8-bit
H	16-bit

(5) Initial display line register

The initial display line resister specifies the line address, corresponding to the initial COM line, by the “Initial display line” instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the “Initial COM line” instruction.

The line address, established in the initial display line resister, is preset into the line counter whenever the FLM signal becomes “1”. At the rising edge of the CL signal, the line counter is counted-up and addressed 384-bit display data, corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data outputs to the segment drivers.

(6) DDRAM mapping

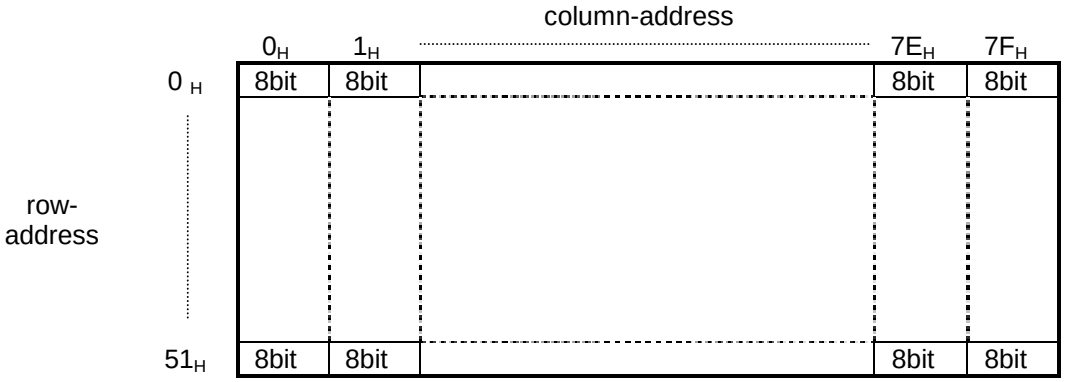
The DDRAM is capable of 1,024-bit (8-bit x 128-segment) for the column address and 82-bit for the row address.

In the gradation mode, each pixel for RGB corresponds to the successive 3-segment drivers that consist of 2-segment drivers for 8-gradation and 1-segment driver for 4-gradation, so that the LSI can drive a 256-color display (8-gradation x 8-gradation x 4-gradation) with up to 128x82 pixels. The 8-gradation level is controlled by 3-bit display data in the DDRAM and 4-gradation level is controlled by 2-bit display data in the DDRAM respectively.

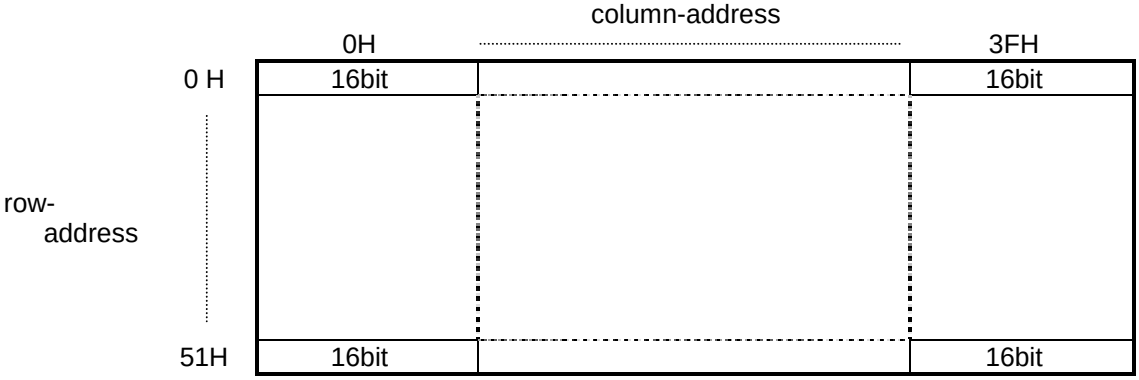
In the B&W mode, only MSB data from each 3-bit and 2-bit RGB display data group in the DDRAM is used. Therefore, 384 x 82 pixels in the B&W display is also available.

The range of the column address varies depending on data bus length. The range between 00_H and 70F is used in the 8-bit data bus length and the range between 00_H and $3F_H$ is in the 16-bit data bus length.

- In the 8-bit data bus length mode



- In the 16-bit data bus length mode



The DDRAM is accessing 8-bit or 16-bit unit addressed by column and row address. In the 16-bit data bus length mode, over 40H address setting is prohibited.
The increment for the column address and row address are set to the auto-increment mode by programming “AXI” and “AYI” registers of the “Increment control” instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters, independent of the line counter. They are used to designate the column address and row address for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address, and output display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

(7) Window addressing mode

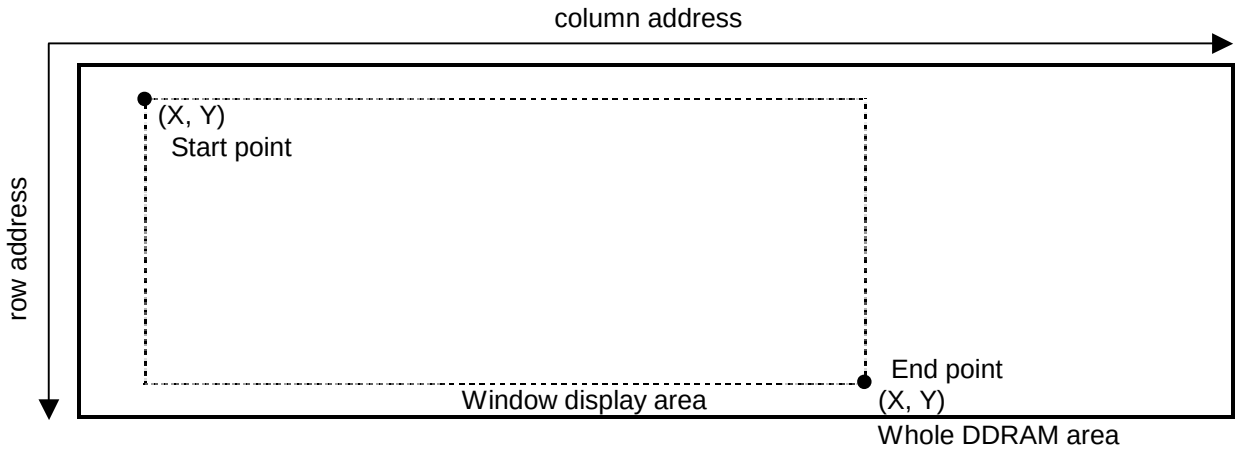
In addition to the above usual DDRAM addressing, it is possible to access some part of DDRAM in using the window addressing mode, in which the start and end points are designated. The start point is determined by the "column address" and "row address" instructions, and the end point is determined by the "Window end column address "and "Window end row address" instructions. The setting example of the window addressing is listed, as follows.

1. Set WIN=1, AXI=1, and AYI=1 by the "Increment control" instruction
2. Set the start point by the "column address" and "row address" instructions
3. Set the end point by the "Window end column address" and "Window end row address" instructions
4. Enable to access to the DDRAM in the window addressing mode

In the window addressing mode (WIN=1, AXI=1, AYI=1), the read-modify-write operation is available by setting "0" to the "AIM" register of the "Increment control" instruction.

And in the window addressing mode, the following start and end point must be maintained to abide a malfunction.

AX (column address of start point) $\leq$ EX (column address of end point) $\leq$ Maximum of column address
AY (row address of start point) $\leq$ EY (row address of end point) $\leq$ Maximum of row address



(8) Reverse display ON/OFF

The "Reverse display ON/OFF" function is used to reverse the display data without changing the contents of the DDRAM.

Table

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Segment direction

The "Segment direction" function is used to reverse the assignment for the segment drivers and column address, and it is possible to reduce the restrictions for the placement of the LSI on the LCD modules.

(10) The relationship among the DDRAM column address, display data and segment drivers

In the color mode, and 16-bit data bus mode

REF	SWAP	column address / bit / segment assign																													
0	0	X=00H														.....	X=3FH															
1	1	X=3FH														.....	X=00H															
		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	.....	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
		palette A			palette B			palette C		palette A			palette B			palette C		.....	palette A			palette B			palette C		palette A			palette B			palette C	
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

REF	SWAP	column address / bit / segment assign																													
0	1	X=00H														.....	X=3FH															
1	0	X=3FH														.....	X=00H															
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	.....	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		palette C			palette B			palette A		palette C			palette B			palette A		.....	palette C			palette B			palette A		palette C			palette B			palette A	
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

In the color mode, and 8-bit data bus mode

REF	SWAP	column address / bit / segment assign																													
0	0	X=00H								X=01H								.....	X=7EH								X=7FH							
1	1	X=7FH								X=7EH								.....	X=01H								X=00H							
		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	.....	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
		palette A			palette B			palette C		palette A			palette B			palette C		.....	palette A			palette B			palette C		palette A			palette B			palette C	
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

REF	SWAP	column address / bit / segment assign																													
0	1	X=00H								X=01H								.....	X=7EH								X=7FH							
1	0	X=7FH								X=7EH								.....	X=01H								X=00H							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	.....	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
		palette C			palette B			palette A		palette C			palette B			palette A		.....	palette C			palette B			palette A		palette C			palette B			palette A	
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

In the B&W mode, and 16-bit data bus mode

REF	SWAP	column address / bit / segment assign																															
0	0	X=00H															.....	X=3FH															
1	1	X=3FH															.....	X=00H															
		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	.....	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

REF	SWAP	column address / bit / segment assign																															
0	1	X=00H															.....	X=3FH															
1	0	X=3FH															.....	X=00H															
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	.....	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

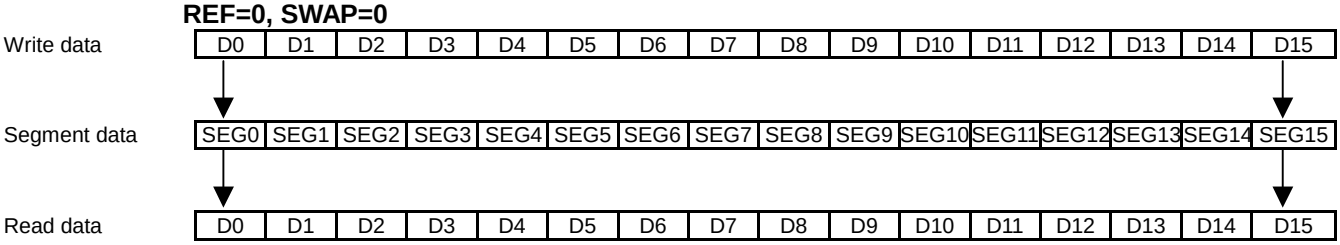
In the B&W mode, and 8-bit data bus mode

REF	SWAP	column address / bit / segment assign																															
0	0	X=00H								X=01H							.....	X=7EH								X=7FH							
1	1	X=7FH								X=7EH							.....	X=01H								X=00H							
		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	.....	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

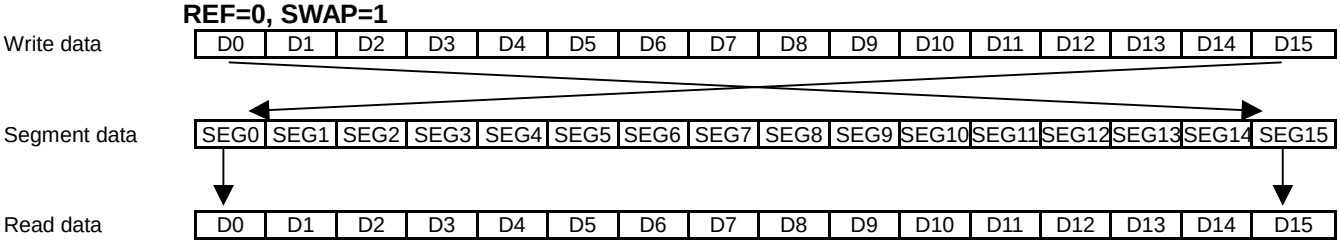
REF	SWAP	column address / bit / segment assign																															
0	1	X=00H								X=01H							.....	X=7EH								X=7FH							
1	0	X=7FH								X=7EH							.....	X=01H								X=00H							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	.....	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
		SEGA0			SEGB0			SEGC0		SEGA1			SEGB1			SEGC1		.....	SEGA126			SEGB126			SEGC126		SEGA127			SEGB127			SEGC127	

- Bit assignments bitween write and read data (in the 16-bit data bus mode)

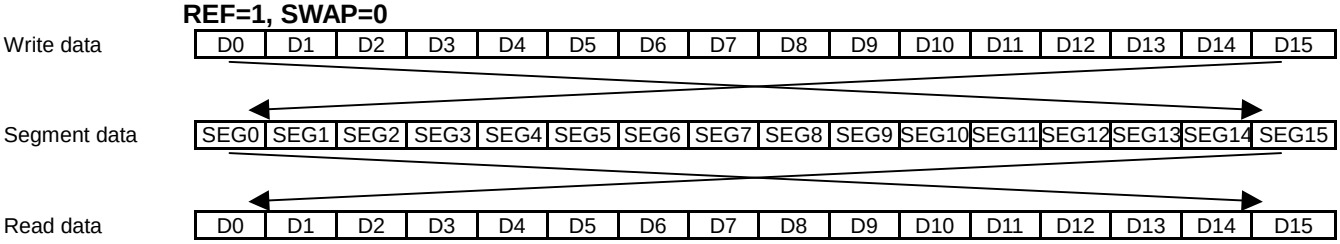
REF=0, SWAP=0



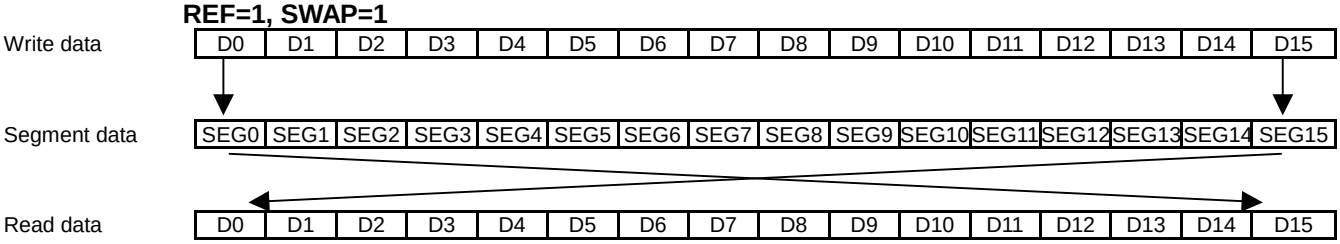
REF=0, SWAP=1



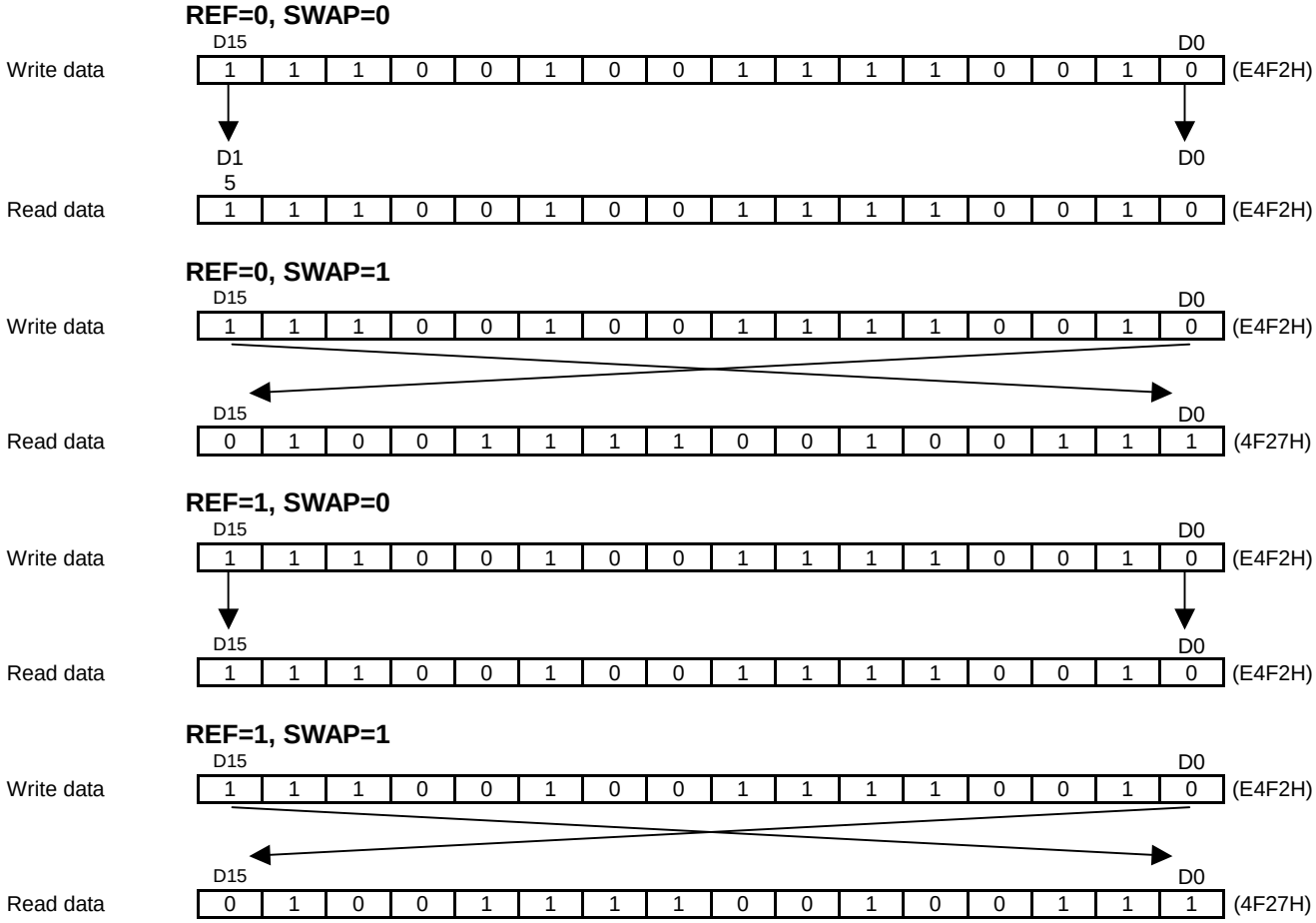
REF=1, SWAP=0



REF=1, SWAP=1

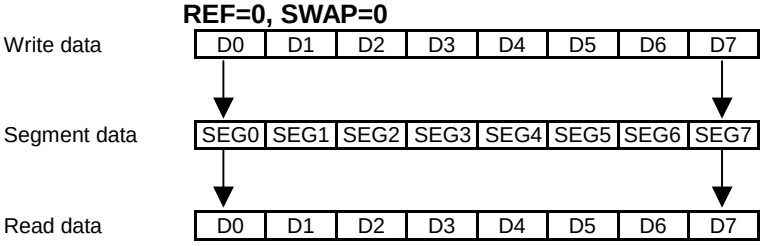


- Examples for write and read data (in the 16-bit data bus mode)

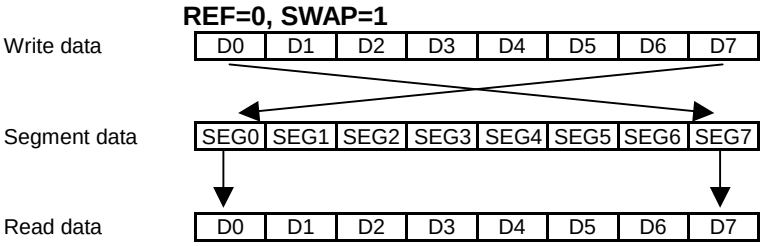


- Bit assignments between write and read data (in the 8-bit data bus mode)

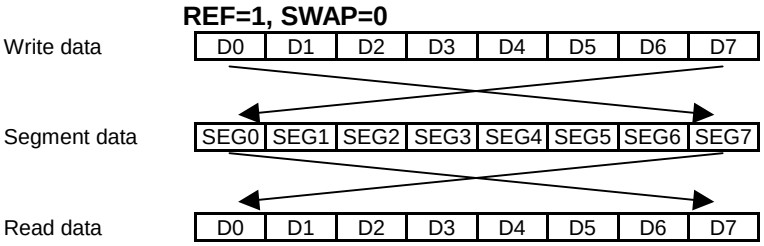
REF=0, SWAP=0



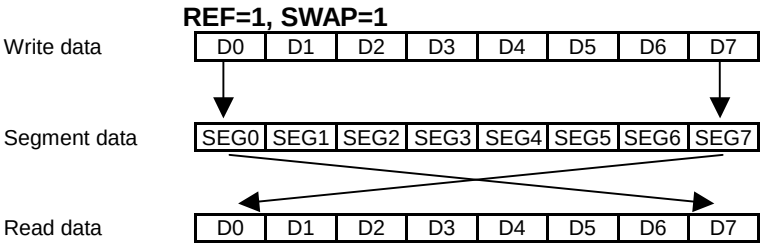
REF=0, SWAP=1



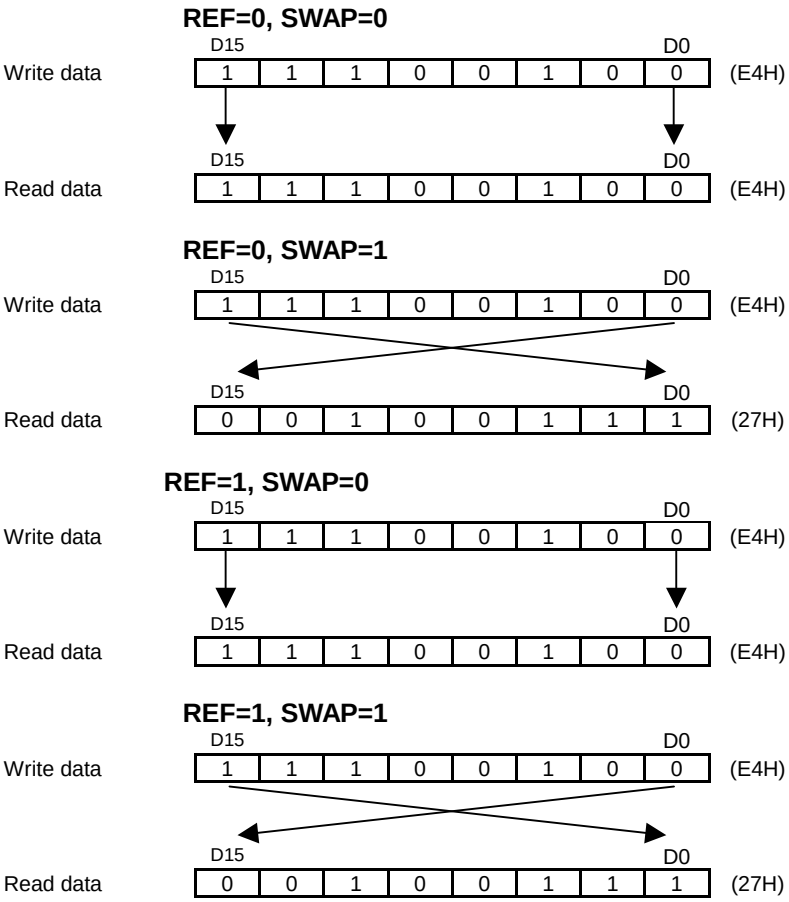
REF=1, SWAP=0



REF=1, SWAP=1



- Examples for write and read data (in the 8-bit data bus mode)



- The relationship among the PGRAM column address, display data and segment drivers

In the color mode, and 16-bit data bus mode

REF	SWAP	column address / bit / segment assign																											
0	0	X=00H														X=01H													
1	1	X=01H														X=00H													
		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
		Palette A			Palette B			Palette C		Palette A			Palette B			Palette C		Palette A			Palette B			Palette C		Palette A			Palette B			Palette C	
		SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3	

REF	SWAP	column address / bit / segment assign																											
0	1	X=00H														X=01H													
1	0	X=01H														X=00H													
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Palette C			Palette B			Palette A		Palette C			Palette B			Palette A		Palette C			Palette B			Palette A		Palette C			Palette B			Palette A	
		SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3	

In the color mode, and 8-bit data bus mode

REF	SWAP	column address / bit / segment assign																											
0	0	X=00H								X=01H								X=02H								X=03H			
1	1	X=03H								X=02H								X=01H								X=00H			
		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
		Palette A			Palette B			Palette C		Palette A			Palette B			Palette C		Palette A			Palette B			Palette C		Palette A			Palette B			Palette C	
		SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3	

REF	SWAP	column address / bit / segment assign																											
0	1	X=00H								X=01H								X=02H								X=03H			
1	0	X=03H								X=02H								X=01H								X=00H			
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
		Palette C			Palette B			Palette A		Palette C			Palette B			Palette A		Palette C			Palette B			Palette A		Palette C			Palette B			Palette A	
		SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3	

In the B&W mode, and 16-bit data bus mode

REF	SWAP	column address / bit / segment assign																													
0	0	X=00H															X=01H														
1	1	X=01H															X=00H														
		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
			SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3

REF	SWAP	column address / bit / segment assign																													
0	1	X=00H															X=01H														
1	0	X=01H															X=00H														
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3	

In the B&W mode, and 8-bit data bus mode

REF	SWAP	column address / bit / segment assign																													
0	0	X=00H								X=01H								X=02H								X=03H					
1	1	X=03H								X=02H								X=01H								X=00H					
		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
			SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3

REF	SWAP	column address / bit / segment assign																													
0	1	X=00H								X=01H								X=02H								X=03H					
1	0	X=03H								X=02H								X=01H								X=00H					
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
		SEGSA0			SEGSB0			SEGSC0		SEGSA1			SEGSB1			SEGSC1		SEGSA2			SEGSB2			SEGSC2		SEGSA3			SEGSB3			SEGSC3	

(11) Gradation palette

In the gradation mode, each of the gradation palettes Aj can select 8-gradation levels out of a palette consisting of 32-gradation levels by setting 5-bit palette value into the “PA” registers in the “Gradation palette Aj” instructions (j=0 to 7). Each of the gradation palettes Bj and Cj can select 8-gradation levels as well as the gradation palette Aj.

The gradation palettes Aj correspond to the SEGAi, the Bj to SEGBj and the Cj to SEGCi (j=0 to 7, i=0 to 127). The display data (0,0,0) corresponds to the gradation palettes Z0, the data (0,0,1) to the Z1, the data (0,1,0) to the Z2…the data (1,1,1) to the Z7 (Z=A, B and C).

(12) Gradation LSB (GLSB)

In the graduation mode, each pixel for RGB corresponds to the successive 3-segment drivers that consist of 2-segment drivers for 8-graduation and 1-segment driver for 4-gradietion. The 8-gradation segment drivers can generate 8-gradation levels controlled by 3-bit display data in the DDRAM. The 4-gradation segment drivers can generate 4-gradation levels by 2-bit in the DDRAM and 1-bit in the GLSB.

All of the selected 8-gradation palettes Zj (Z=A, B and C, j=0 to 7) are available for the 8-gradation segment drivers. However, the only 4-gradation palettes Zj (Z=A, B and C, j= either 0,2,4,6 or 1,3,5,7) are available for the 4-gradation segment drivers, because the GLSB is fixed to either “0” or “1” by setting the “GLSB” register in the “Gradation control” instruction and adopted to all of the 4-gradation segment derivers.

GLSB=0: The LSB of display data is always set to “0”.
Display data: (0,0,0), (0,1,0), (1,0,0), (1,1,0) → Gradation palettes: Z0, Z2, Z4, Z6 (Z=A, B and C)

GLSB=1: The LSB of display data is always set to “1”.
Display data: (0,0,1), (0,1,1), (1,0,1), (1,1,1) → Gradation palettes: Z1, Z3, Z5, Z7 (Z=A, B and C)

(13) Variable or fixed gradation mode

In the gradation mode, either variable or fixed gradation mode is selected by programming the “PWM” register of the “Gradation control” instruction.

PWM=0: Variable gradation mode
(Select 8 gradation levels out of 32-gradation level of the gradation palette)

PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

- Correspondence between display data and gradation palettes (MON="0"; Gradation mode)

(Z=A, B and C, j=0 to 7)

(MSB) Display data (LSB)			Gradation palette Zj
0	0	0	Palette Z0
0	0	1	Palette Z1
0	1	0	Palette Z2
0	1	1	Palette Z3
1	0	0	Palette Z4
1	0	1	Palette Z5
1	1	0	Palette Z6
1	1	1	Palette Z7

Default palette value
0 0 1 0 0
0 0 1 0 1
0 1 0 1 0
0 1 1 1 0
1 0 0 0 1
1 0 1 0 1
1 1 0 1 0
1 1 1 1 1

- Gradation palette table (Variable gradation mode, PWM="0", MON="0")

(Z=A, B and C, j=0 to 7)

Palette value	Gradation level	Gradation palette Zj	Palette value	Gradation level	Gradation palette Zj
0 0 0 0 0	0	Palette Z0 (default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette Z4 (default)
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette Z1 (default)	1 0 1 0 1	21/31	Palette Z5 (default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	Palette Z2 (default)	1 1 0 1 0	26/31	Palette Z6 (default)
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	Palette Z3 (default)	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	Palette Z7 (default)

- Gradation palette table (Fixed gradation mode, PWM="1", MON="0")

8-gradation segment drivers

Display data (MSB)	DDRAM	(LSB)	Gradation level
0	0	0	0
0	0	1	1/7
0	1	0	2/7
0	1	1	3/7
1	0	0	4/7
1	0	1	5/7
1	1	0	6/7
1	1	1	7/7

4-gradation segment drivers

Display data DDRAM		GLSB	Gradation level
0	0	0	0
0	0	1	
0	1	0	2/7
0	1	1	3/7
1	0	0	4/7
1	0	1	5/7
1	1	0	7/7
1	1	1	

- Correspondence between display data and gradation level (B&W mode, MON="1")

8-gradation segment drivers

Display data (MSB)	DDRAM	(LSB)	Gradation level
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

4-gradation segment drivers

Display data DDRAM		GLSB	Gradation level
0	0	*	0
0	1	*	0
1	0	*	1
1	1	*	1

*: Don't care

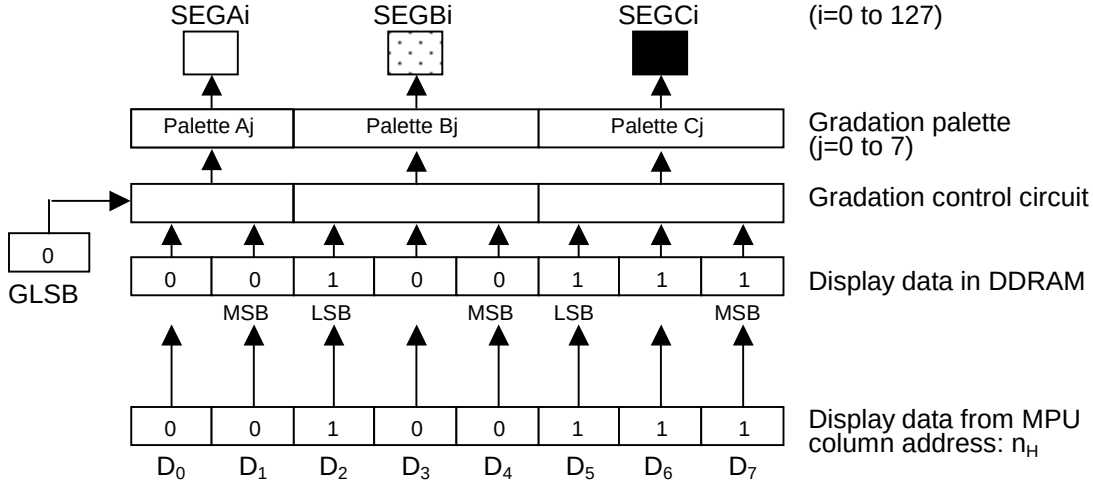
(14) Gradation control and display data

(14-1) Gradation mode

In the graduation mode, each pixel for RGB corresponds to the successive 3 segment drivers that consist of 2 segment drivers for 8-graduation and 1 segment driver for 4-gradietion, so that **NJU6821** can drive a 256-color display (8-gradation x 8-gradation x 4-gradition) with up to 128x82 pixels. The 8-gradation segment drivers can generate 8-gradation levels controlled by using 3-bit of display data in the DDRAM. The 4-gradation segment drivers can generate 4-gradation levels by using 2-bit in the DDRAM and 1-bit in the GLSB.

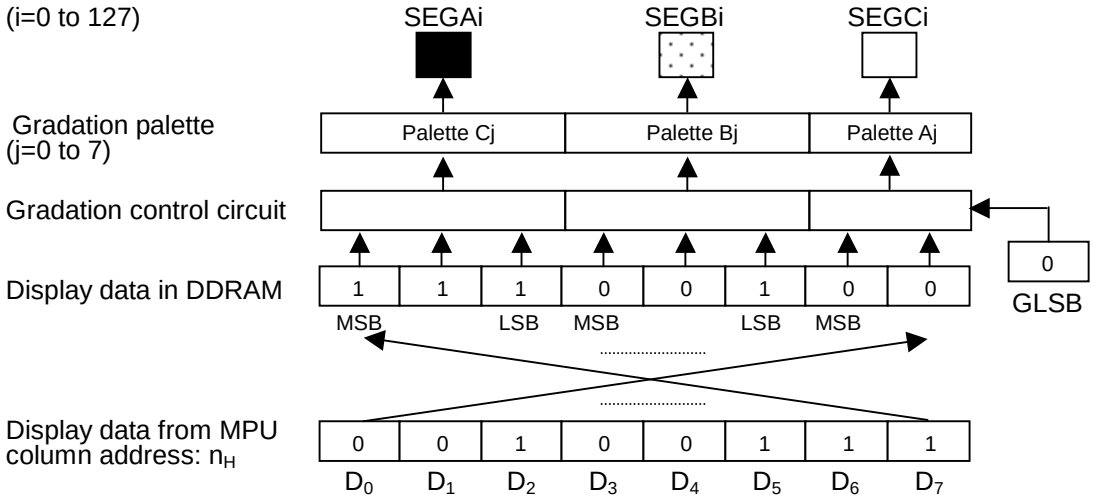
In addition, the LSI can transfer 8-bit display data for 1-pixel the RGB or 16-bit for 2-pixels RGB to the DDRAM at one-time access. The data assignment between gradation palettes and segment drivers varies in accordance with the setting for the “SWAP” and “REF” registers of the "Display control (2)" instruction.

● (REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : $7_H \rightarrow 7F_H$ (REF=”0”)
:$7F_H \rightarrow n_H$ (REF=”1”)

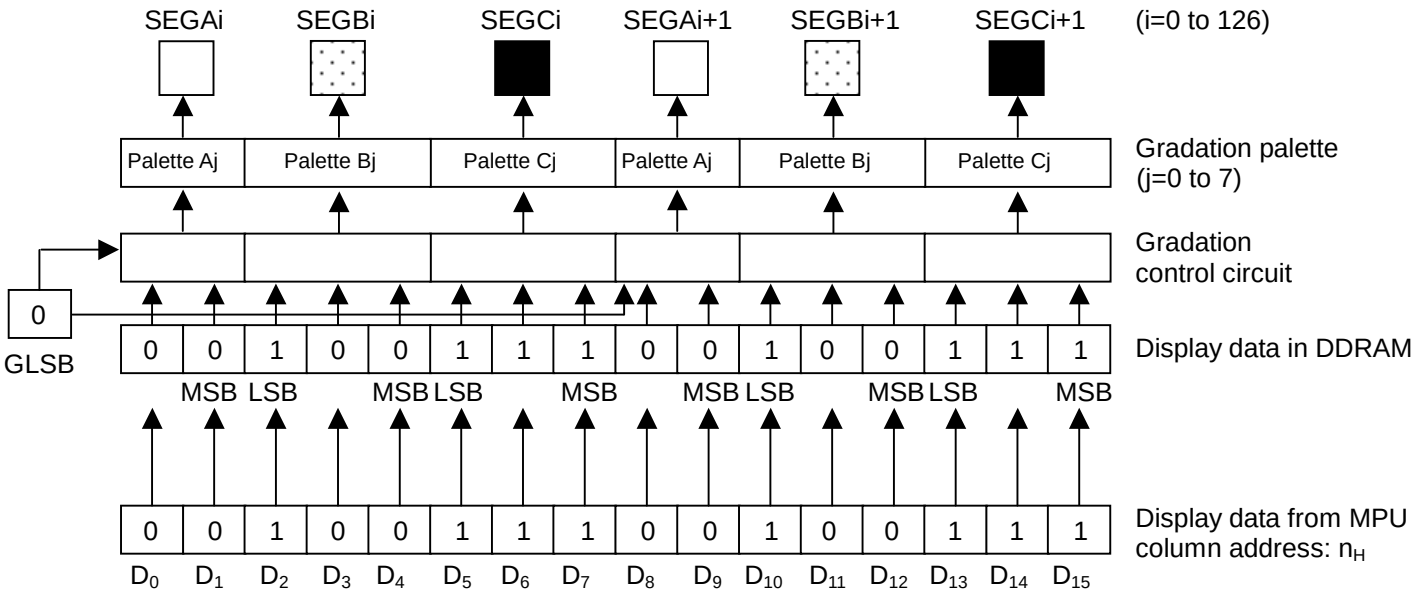
● (REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : nH (REF=”0”)
: $7F_H \rightarrow$ nH (REF=”1”)

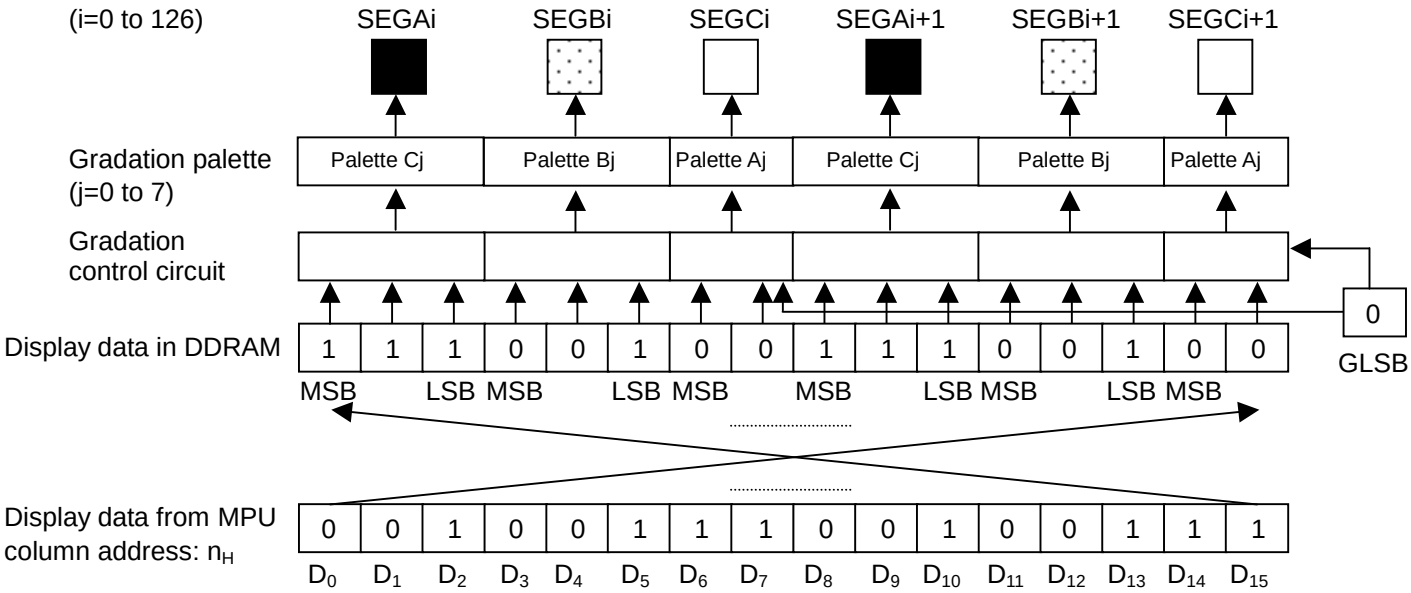
In the 16-bit data bus mode, the data assignments between the gradation palettes and the segment drivers vary in accordance with setting for the “SWAP” and “REF” bit of the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

● (REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF=”0”)
: $3F_H \rightarrow n_H$ (REF=”1”)

● (REF, SWAP)=(0, 0) or (1, 1)



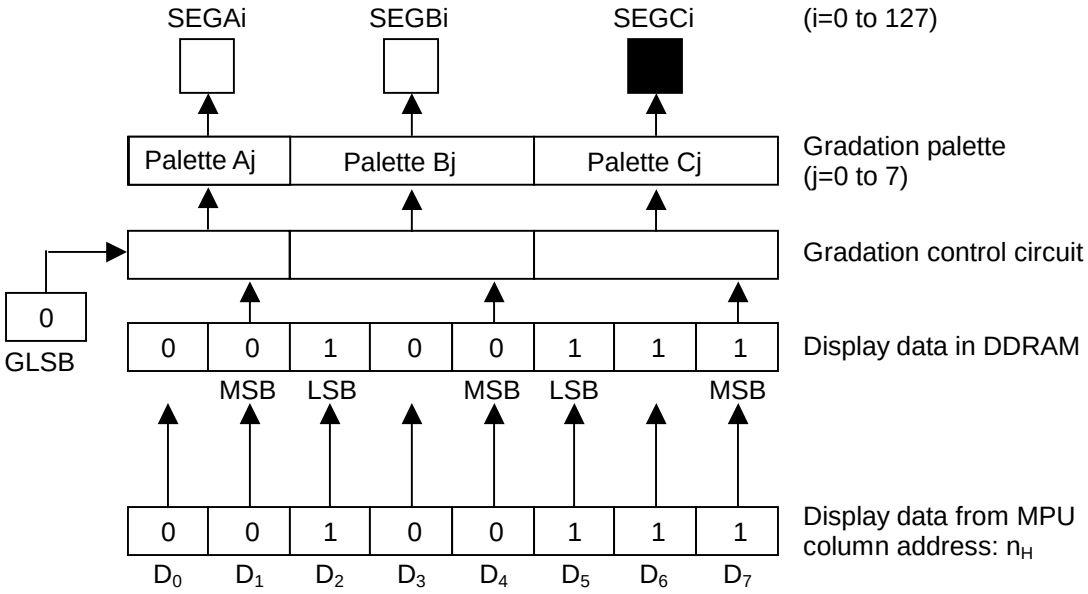
Note) DDRAM column address :n_H (REF=”0”)
:$3F_H \rightarrow$ nH (REF=”1”)

(14-2) B&W mode (MON="1")

In the B&W mode and 8-bit data bus mode, only 3 of MSB of each display data is used for the display. In the 16-bit data bus mode, 6 of MSB of each display data are used.

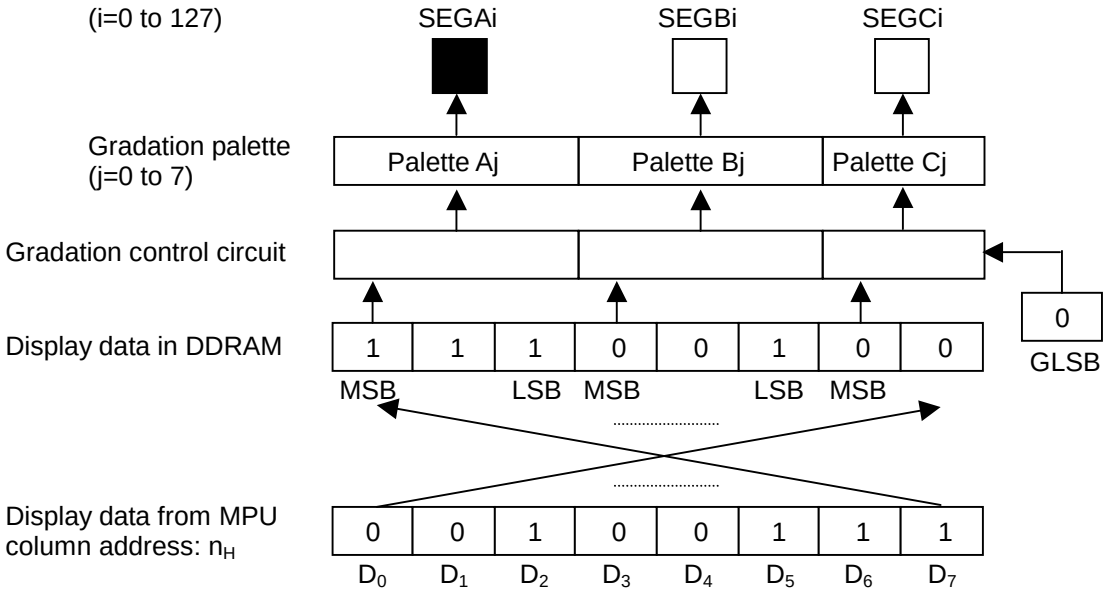
In the 8-bit data bus mode (Similarly 16-bit data bus access)

- (REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF="0")
: $7F_H \rightarrow n_H$ (REF="1")

- (REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : n_H (REF="0")
: $7F_H \rightarrow n_H$ (REF="1")

(15) Display timing generator

The display-timing generator creates the timing pulses such as the CL, the FLM, the FR and the CLK by dividing the oscillation frequency oscillate an external or internal resister mode. The timming pulse terminals and timing generator status is setting by the Master/Slave (M/S) terminal as described in the following table.

The statuses of timing pulse terminal and generator

M/S	Mode	CL	FR	FLM	CLK
L	Slave	Input	Input	Input	Input
H	Master	Output	Output	Output	Output

(16) LCD line clock (CL)

The LCD line clock (CL) is used as a count-up signal for the line counter and a latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to this line address, is latched into the data latch circuit. And at the falling edge of the CL signal, this latched data output on the segment drivers. Read out timing of the display data, from DDRAM to the latch circuits, is completely independent of the accsess timing to the MPU. For this reason, the MPU can access to the LSI regardless of an internal operation.

(17) LCD alternate signal (FR) and LCD synchronous signal (FLM)

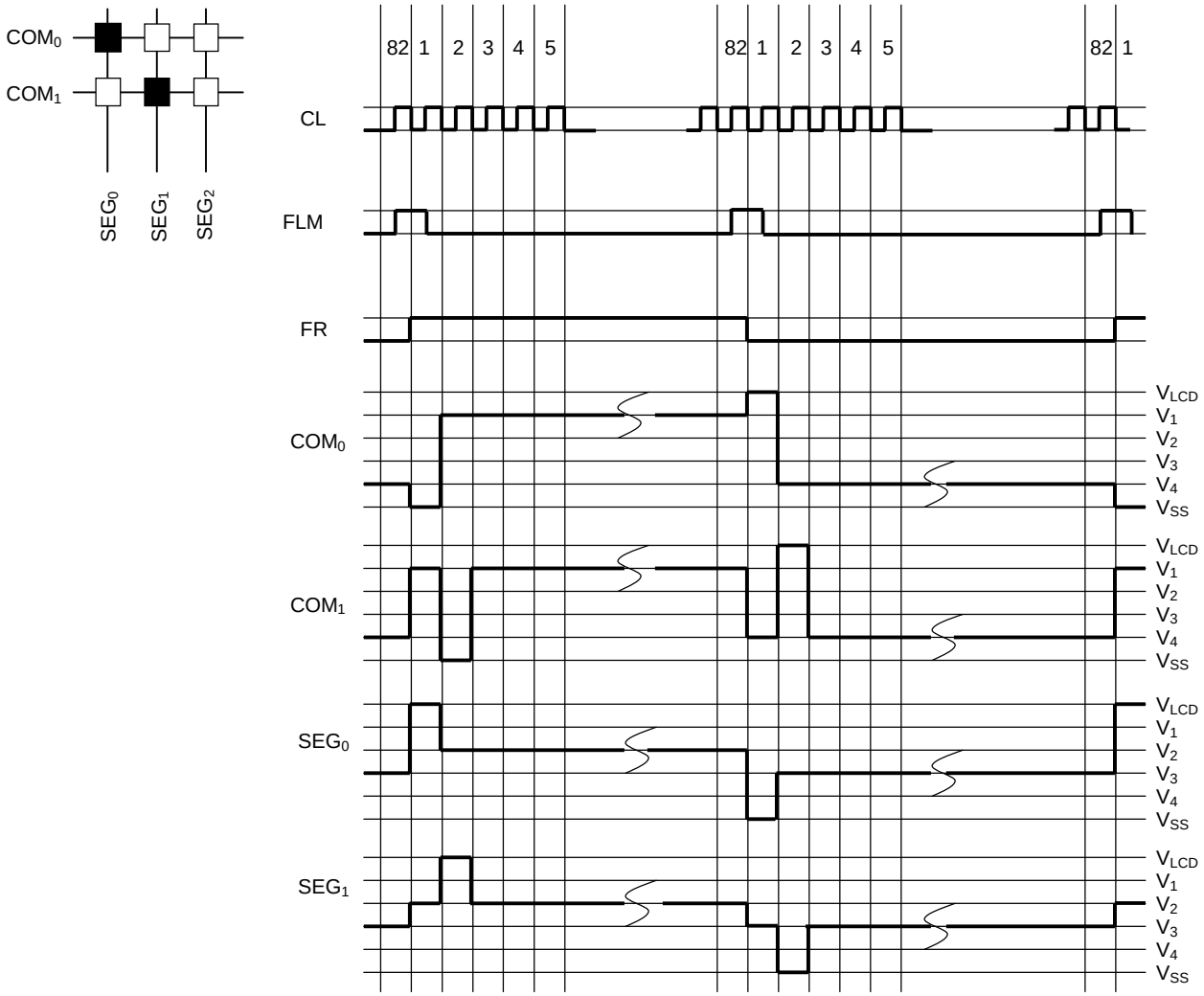
The FR and FLM signals are created from the CL signal. The FR signal is used to alternate the crystal polarization on a LCD panel. It is programmed that the FR signal is toggle on every frame in the default setting or once every N lines in the N-line inversion mode. The FLM signal is used to indicate a start line of a new display frame. It presets an initial display line address of the line counter when the FLM signal becomes ”1”. When two of **NJU6821** is using as a Master and Slave, the CL, the FLM, the FR, and the CLK signals should be supplied from Master **NJU6821** to Slave **NJU6821**.

(18) Data latch circuit

The data latch circuit is used temporarily store the display data that will output to the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The “All pixels ON/OFF”, “Display ON/OFF” and “Reverse display ON/OFF” instructions change the display data in this circuit but do not change the display data of the DDRAM.

- LCD Driving waveforms (In the B&W mode, Reverse display OFF, 1/82 duty)



(19) Common and segment drivers

The LSI includes 384-segment drivers and 82-commom drivers for a graphic display. 2 out of 82-common drivers are assigned to the $COMI_0$ and $COMI_1$ for an icon display. The common drivers generate the LCD driving waveforms composed of the V_{LCD}, V_1, V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate the waveforms composed of the V_{LCD}, V_2, V_3 and V_{SS} in accordance with the FR signal and display data.

(20) Icon segment drivers

The 12-icon-segment drivers: SEGSAk, SEGSBk and SEGSCk (k=0 to 3) are mainly used for an outer-frame display. 6-icon-segment drivers each are positioned in both sides of the segment drivers' block. The icon segment drivers are controlled by the display data entered in the icon segment registers instead of the DDRAM. The dummy segment drivers SEGAk correspond to the gradation palette Aj, the SEGSBk to the palette Bj and the SEGSCk to the palette Cj (k=0 to 3, j=0 to 7). The icon segment registers are capable of 4-byte display data, in which each byte is corresponding to 1-set of the icon segment drivers such as the $SEGSA_0$, $SEGSB_0$ and $SEGSC_0$.

The icon segment registers are enabled by setting "1" into the "DMY" register in the "Icon segment register ON/OFF" instruction and then the "column address" instruction, where the column address such as 00H, 01H, 02H and 03H are available in the 8-bit data bus mode and the column address such as 00H and 01H in the 16-bit mode. The icon segment drivers are independent of the "row address set" instruction.

- 8-bit data bus mode (DMY="1")

  column address
  00H: $SEGSA_0$, $SEGSB_0$, $SEGSC_0$
  01H: $SEGSA_1$, $SEGSB_1$, $SEGSC_1$
  02H: $SEGSA_2$, $SEGSB_2$, $SEGSC_2$
  03H: $SEGSA_3$, $SEGSB_3$, $SEGSC_3$

- 16-bit data bus mode (DMY="1")

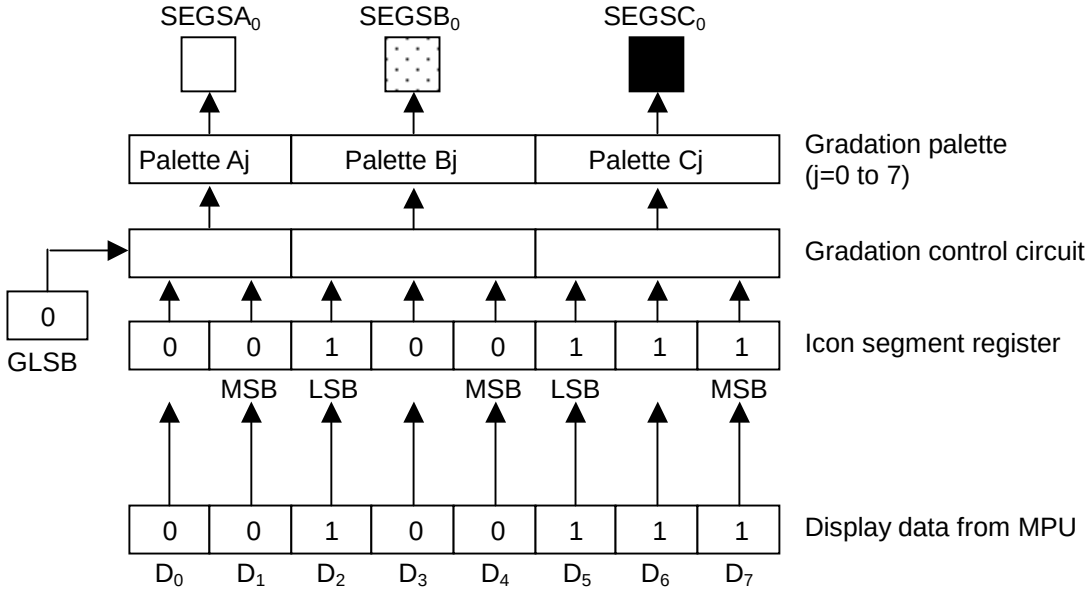
  column address
  00_H: $SEGSA_0$, $SEGSB_0$, $SEGSC_0$, $SEGSA_1$, $SEGSB_1$, $SEGSC_1$
  01_H: $SEGSA_2$, $SEGSB_2$, $SEGSC_2$, $SEGSA_3$, $SEGSB_3$, $SEGSC_3$

The icon segment drivers can support the "ALLON" and "REV" registers in the "Display control (1), (2)" instructions but they cannot support the "LREV" and "BT" registers in the "Line inverse control" instruction. As well as the read sequence for the DDRAM, the sequence for the segment registers also requires the dummy read.

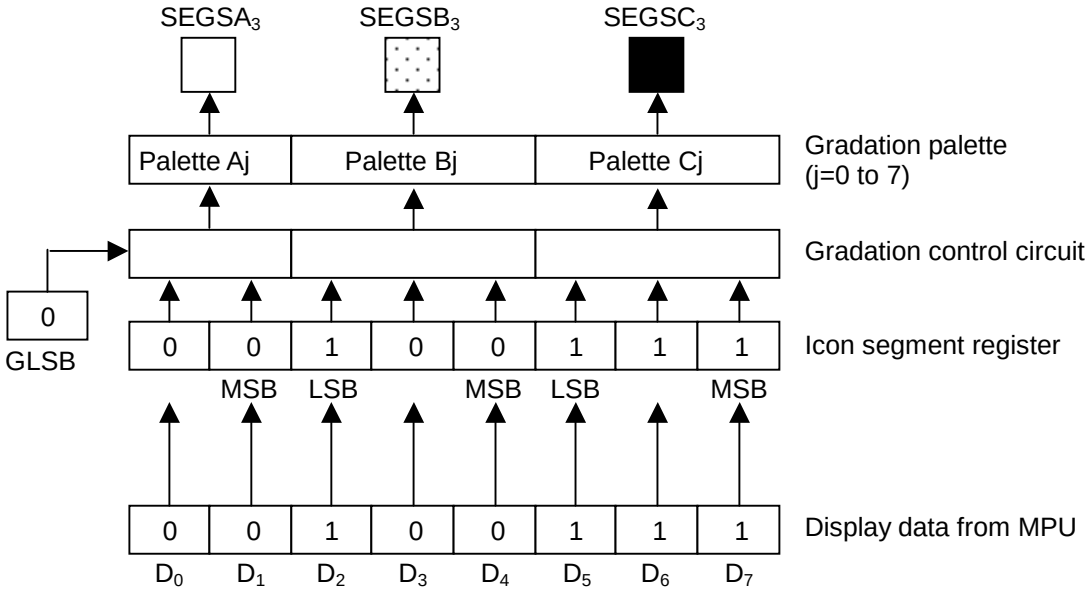
RS	DMY	68 series	80 series		Function
		R/W	RD	WR	
0	0	1	0	1	Read data from DDRAM
0	0	0	1	0	Write data into DDRAM
0	1	1	0	1	Read data from icon segment register
0	1	0	1	0	Write data into icon segment register

● Examples for the icon segment registers (DMY="1")
(In the 8-bit data bus mode, gradation mode, (REF, SWAP)=(0,0))

column address: 00_H



column address: 03_H



(21) Oscillator

The oscillator generates the internal clocks for the display timing and the voltage booster. It is enabled only in the master mode operation by setting the "M/S" terminal to "1". The C and R for the oscillator are on chipped, therefore, there is no C, R required as an external components. Use an external R instead of internal R is also available(CKS=1), in this time connect the resister between OSC_1 and OSC_2 terminals. However, when the internal oscillator is not used, an external clock inputs to the OSC_1 terminal.

In addition, the feed back resister for the oscillator is varied by programming the "Rf" register in the "Frequency control" instruction, so that it is possible to optimize the frame frequency for a LCD panel. Setting examples of the MON(B&W /Gradation) and the PWM(Variable gradation /Fixed gradation) are described, as follows.

Internal oscillation mode (CKS=0)

Symbol	FFL	MON	PWL	Display mode
f_1	1	0	0	Variable gradation mode
f_2	0	0	0	
f_3	1	0	1	Fixed gradation mode
f_4	0	0	1	
f_5	1	1	*	B&W mode
f_6	0	1	*	

*: Don't care

- External resistor oscillation mode (CKS=1)

  The internal clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "FFL", "MON" and "PWM" register must be set as well.

- External clock input mode (CKS=1)

  The external clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "FFL", "MON" and "PWM" register must be set as well.

(22) Power supply circuits

The internal power supply circuits are composed of the voltage booster, the electrical variable resister (EVR), voltage regulator, reference voltage generator and the voltage followers.

The condition of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers on the "Power control" instruction. For this arrangement, some parts of the internal power supply circuits are activated in using an external power supply, as shown in the following table.

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4	1, 3
0	1	Disable	Enable	VOUT	2, 3
1	1	Enable	Enable	–	–

Note1) The internal power circuits are not used. The external V_{OUT} is required and C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{REF}, V_{REG} and V_{EE} terminals must be open.

Note2) The internal power circuits except the voltage booster are used. The external V_{OUT} is required and the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+ and C_6- terminals must be open. The reference voltage is required to V_{REF} terminal.

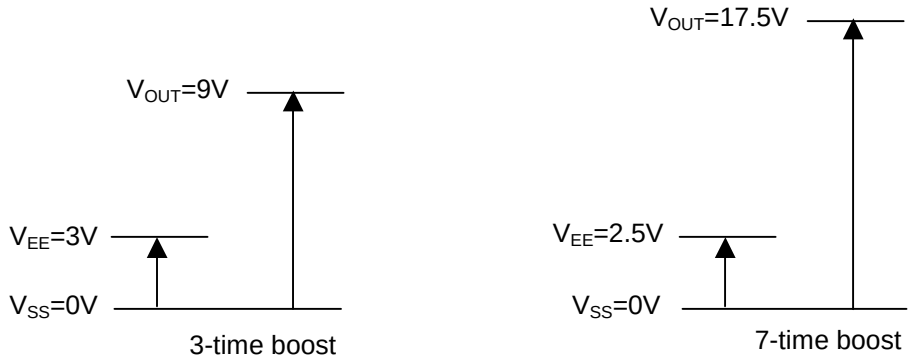
Note3) The relation among the voltages should be maintained as follows.

$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$

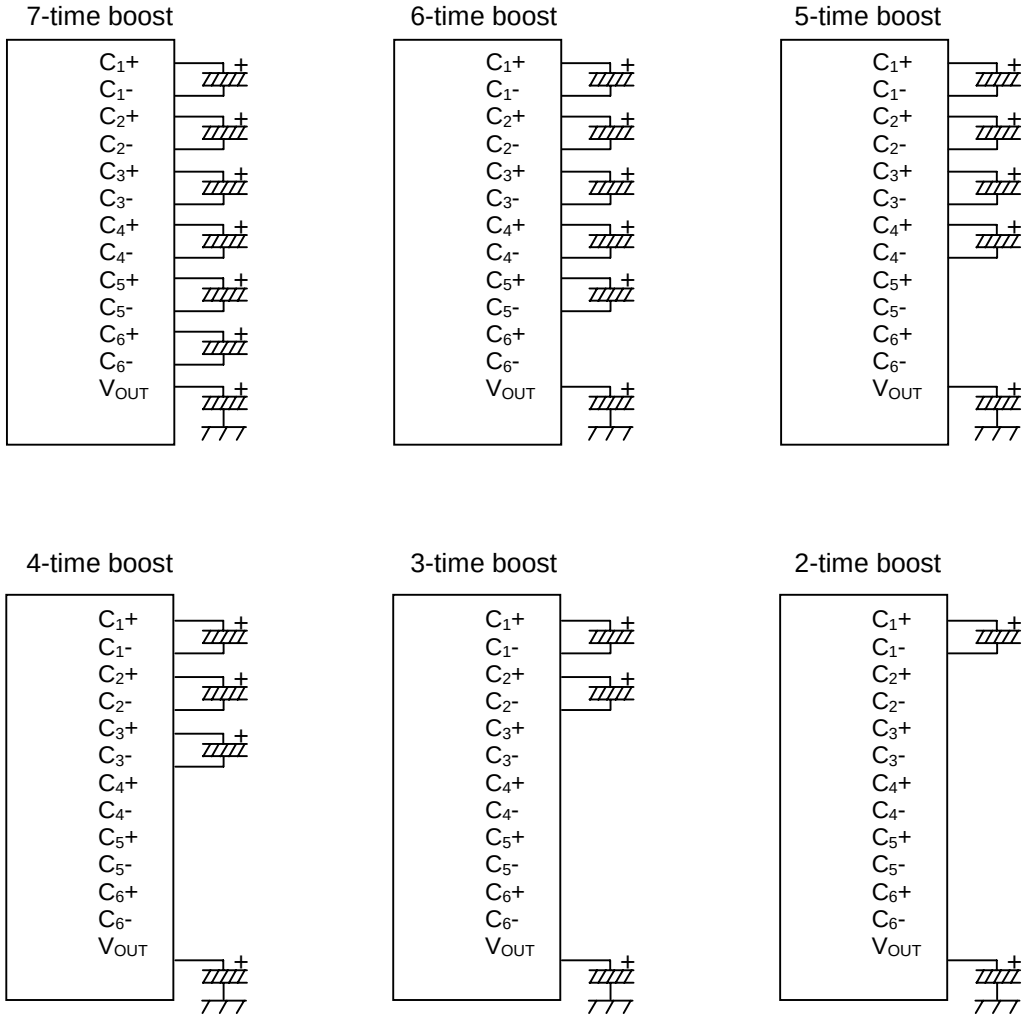
(23) Voltage booster

The voltage booster generates maximum 7x voltage of the V_{EE} level. It is programmed so that the boost level is selected out of 1x, 2x, 3x, 4x, 5x, 6x and 7x by the “Boost level select” instruction. The boosted voltage V_{OUT} must not exceed beyond the value of 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

- Boosted voltages



- Capacitor connections for the voltage Booster



(24) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}), which is output from the V_{BA} terminal and should be input to the V_{REF} terminal.

$$V_{BA} = V_{EE} \times 0.9$$

(25) Voltage regulator

The voltage regulator, composed of the gain control circuit and an operational amplifier, and is used to gain the reference voltage (V_{REF}) and to create the regulated voltage (V_{REG}). The V_{REG} is used as an input voltage to the EVR circuits, which is programming by the “VU” register of the “Boost level” instruction.

$$V_{REG} = V_{REF} \times N \qquad \text{(N: register value for the boost level)}$$

(26) Electrical variable resister (EVR)

The EVR is variable within 128-step, and is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the “DV” register in the “EVR control” instruction, so that it is possible to optimize the contrast level of LCD panels.

$$V_{LCD} = 0.5 \times VREG + M\,(VREG - 0.5 \times VREG) / 127 \qquad \text{(M: register value for the EVR)}$$

(27) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the V_{LCD} voltage levels as V_{LCD}, V_1, V_2, V_3 and V_4 with internal E.V.R and the Bleeder resistors. The bias ratio of the LCD driving voltage is selected out of 1/5, 1/6, 1/7, 1/8, 1/9, and 1/10.

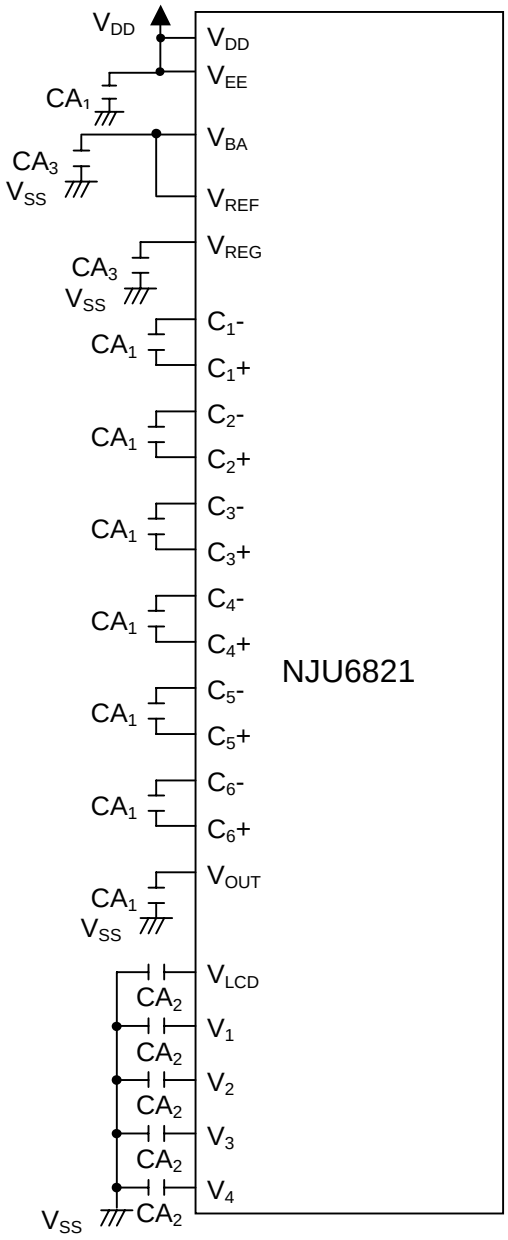
In using the internal power supply, the capacitors CA_2 must be connected to the V_{LCD}, V_1, V_2, V_3 and V_4 terminals, and the CA_2 value must be determined by the evaluation with actual LCD modules.

In using the external power supply, the external LCD driving voltages such as the V_{LCD}, V_1, V_2, V_3 and V_4 are supplied and the internal power supply circuits must be set to “OFF” by DCON = AMPON = "0". In this mode, voltage booster terminals such as C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+, C_5-, C_6+, C_6-, V_{EE}, V_{REF} and V_{REG} must be opened.

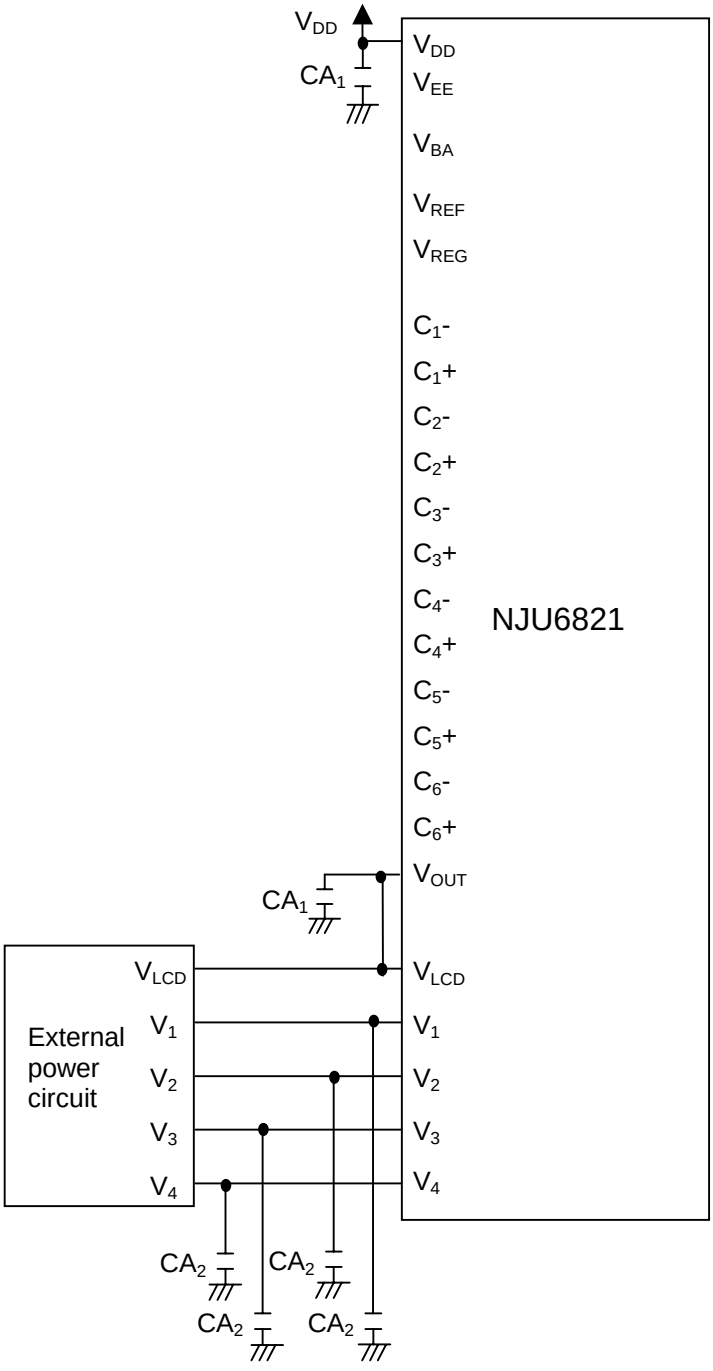
In case that the voltage booster is not used but only some parts of internal power supply circuits (Voltage followers, Voltage regulator and EVR) are used, the C_1+, C_1-, C_2+, C_2-, C_3+, C_3-, C_4+, C_4-, C_5+ C_5-, C_6+, and C_6- terminals must be opened. And, the external power supply is input to the V_{OUT} terminal, and the reference voltage to the V_{REF} terminal. The capacitor CA_3 must connect to the V_{REG} terminal for voltage stabilization.

● Connections of the capacitors for the voltage booster

Using all of the internal power supply circuits (7-time boost)



Using only external power supply circuits



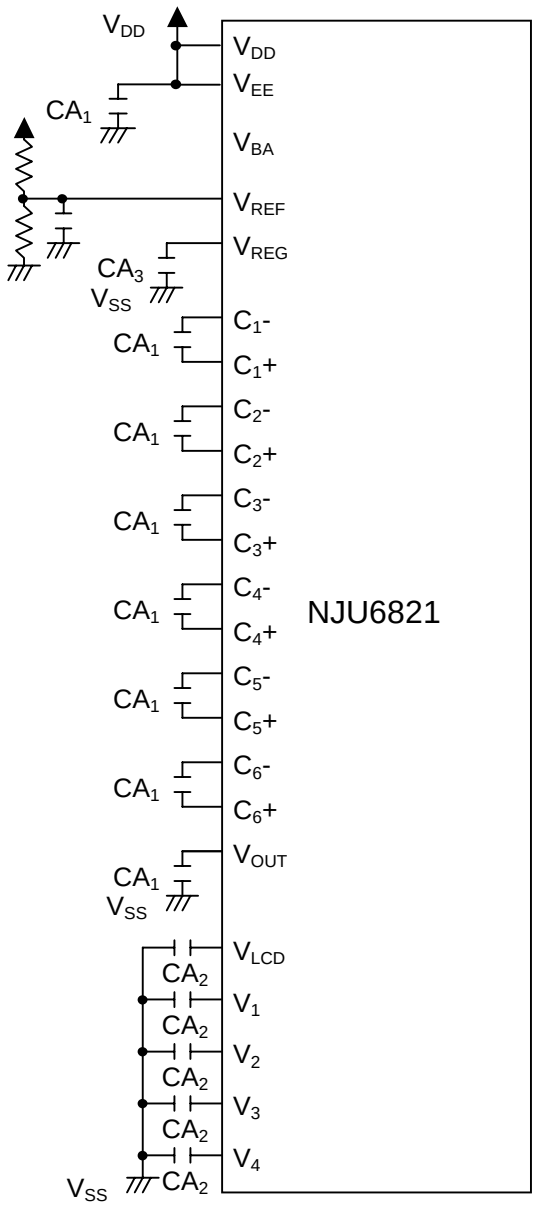
Reference values

CA_1	1.0 - 4.7µF
CA_2	1.0 - 2.2µF
CA_3	0.1µF

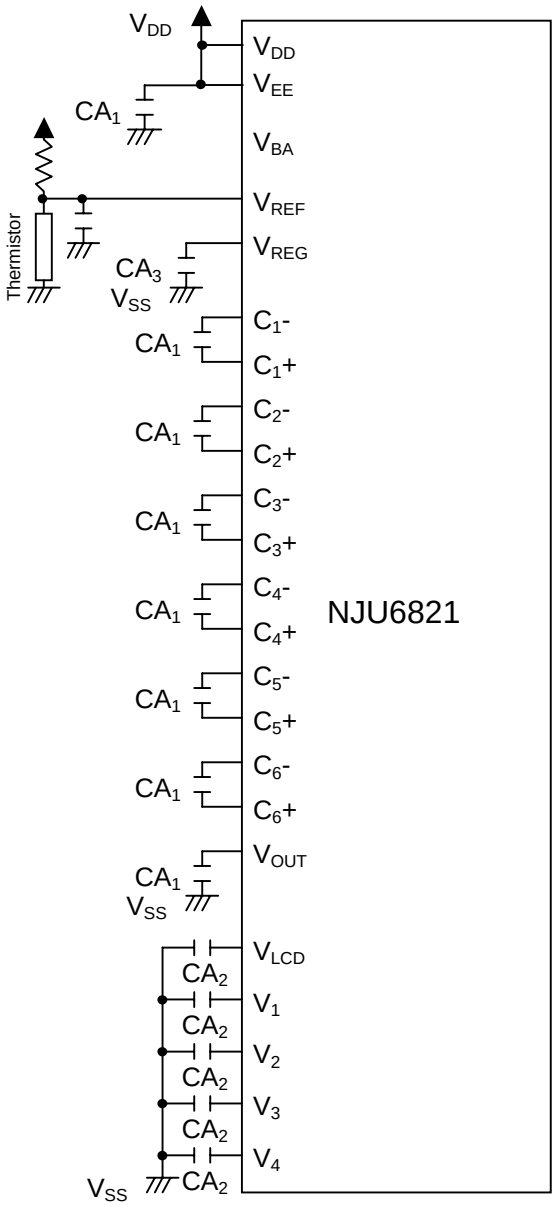
Note1) B grade capacitor is recommended for CA_1-CA_3. Testing actual samples with an LCD panel is recommended to decide an optimum value of these capacitors.

Note2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces the step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, use the shortest possible wires and place the capacitors to be as close as possible to the LSI.

Using internal power supply circuits
Without the reference voltage generator (1)
(7-time boost)



Using internal power supply circuits
Without the reference voltage generator (2)
(7-time boost)



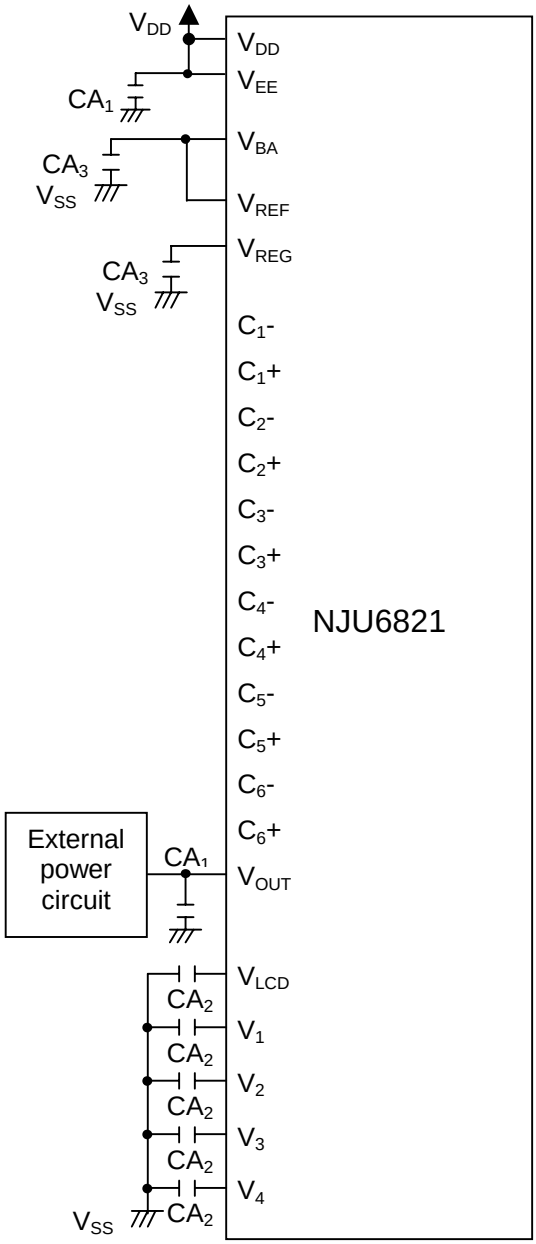
Reference values

CA_1	1.0 - 4.7µF
CA_2	1.0 - 2.2µF
CA_3	0.1µF

Note1) B grade capacitor is recommended for CA_1-CA_3. Testing actual samples with an LCD panel is recommended to decide an optimum value of these capacitors.

Note2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces the step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, use the shortest possible wires and place the capacitors to be as close as possible to the LSI.

Using nternal power supply circuits
Without the voltage booster



Reference values

CA_1	1.0 - 4.7µF
CA_2	1.0 - 2.2µF
CA_3	0.1µF

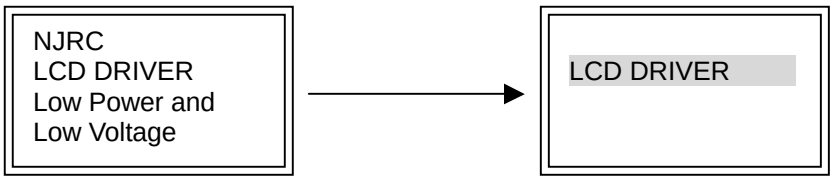
Note1) B grade capacitor is recommended for CA_1-CA_3. Testing actual samples with an LCD panel is recommended to decide an optimum value of these capacitors.

Note2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces the step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, use the shortest possible wires and place the capacitors to be as close as possible to the LSI.

(28) Partial display function

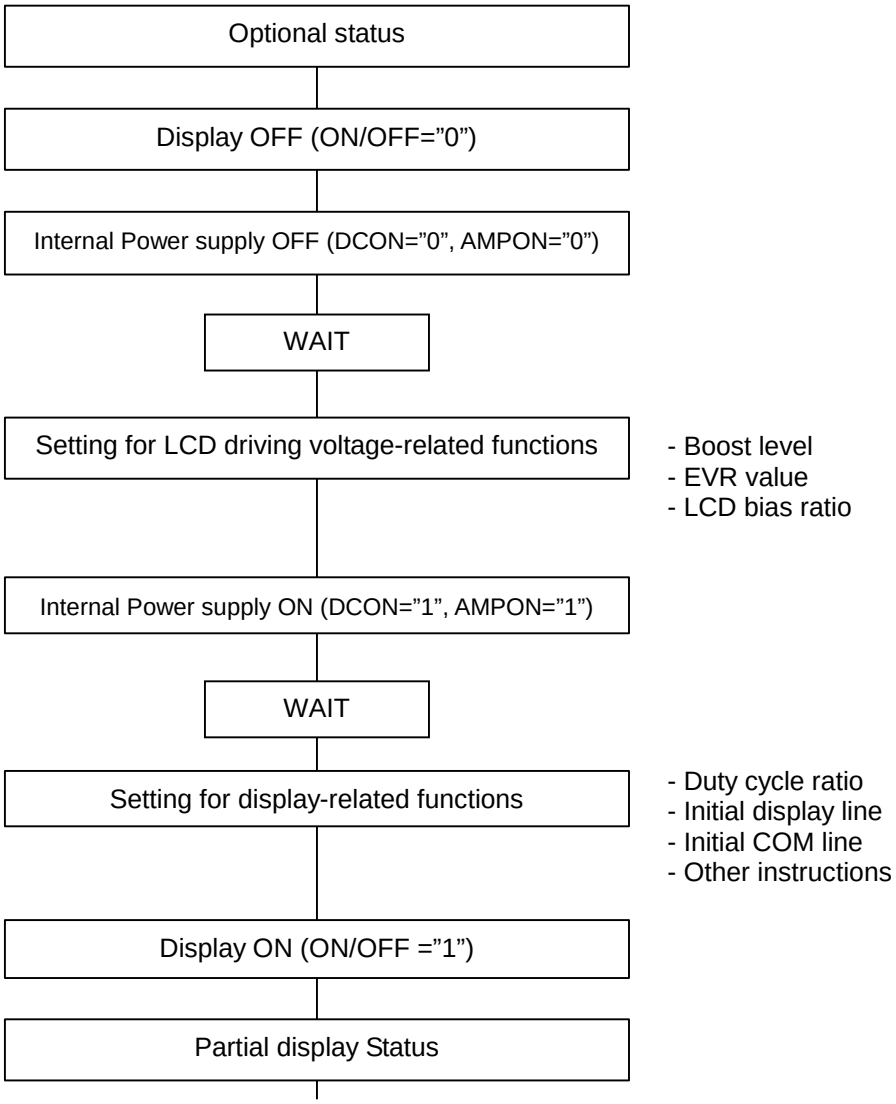
The partial display function is used to specify some parts of display area on a LCD panels. By using this function, LCD modules can work in lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. It is usually used to display a time and calendar in the extremely low power consumption. It can be programmed to select the duty cycle ratio (1/17, 1/26, 1/32, 1/38, 1/47, 1/66, 1/77), the LCD bias ratio, the boost level and EVR value by the instructions.

- Partial display image



Normal display　　Partial display

- Partial display sequence



(29) Discharge circuit

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and V_{LCD} terminals. This circuit is activated by setting “0” to the “DIS” register of the “Discharge” instruction or by setting the “RESb” terminal to ”0” level. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

(30) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RESb terminal to “0” level. The RESb terminal is usually required to connect to MPU reset terminal in order that the LSI can be initialized at the same timing of the MPU.

- Default status

1. DDRAM display data :Undefined
2. column address :00_H
3. row address :00_H
4. Initial display line :0_H(1st line)
5. Display ON/OFF :OFF
6. Reverse display ON/OFF :OFF (normal)
7. Duty cycle ratio :1/82 duty
8. N-line Inversion ON/OFF :OFF
9. COM scan direction :$COM_0 \rightarrow COM_{79}$, $COMI_0$, $COMI_1$
10. Increment mode :OFF
11. Reverse SEG direction :OFF (normal)
12. SWAP mode :OFF (normal)
13. EVR value :(0, 0, 0, 0, 0, 0, 0)
14. Internal power supply :OFF
15. Display mode :Gradation display mode
16. LCD bias ratio :1/9 bias
17. Gradation Palette 0 :(0, 0, 0, 0, 0)
18. Gradation Palette 1 :(0, 0, 1, 0, 1)
19. Gradation Palette 2 :(0, 1, 0, 1, 0)
20. Gradation Palette 3 :(0, 1, 1, 1, 0)
21. Gradation Palette 4 :(1, 0, 0, 0, 1)
22. Gradation Palette 5 :(1, 0, 1, 0, 1)
23. Gradation Palette 6 :(1, 1, 0, 1, 0)
24. Gradation Palette 7 :(1, 1, 1, 1, 1)
25. Gradation mode control :Variable gradation mode
26. GLSB :GLSB=0
27. Data bus length :8-bit data bus length
28. Discharge circuit :OFF

(31) Power supply ON/OFF sequences

The following paragraphs describe power supply ON/OFF sequences, which are to protect the LSI from over current.

(31-1) Using an external power supply

- Power supply ON sequence

  Logic voltage (V_{DD}) must be always input first, and next the LCD driving voltages (V_1 to V_4 and V_{LCD}) are turned on. In using the external V_{OUT}, the V_{DD} must be input first, next the reset operation must be performed, and finally the V_{OUT} can be input.

- Power supply OFF sequence

  Either the reset operation, cutting off the V_1 to V_4 and V_{LCD} from the LSI by the RESb terminal or the "Power control" instruction must be performed first, and next the V_{DD} is turned off. It is recommended that a series-resister between 50Ω and 100Ω is added on the V_{LCD} line (or V_{OUT} line in using only the external V_{OUT} voltage) in order to protect the LSI from the over current.

(31-2) Using the internal power supply circuits

- Power supply ON sequence

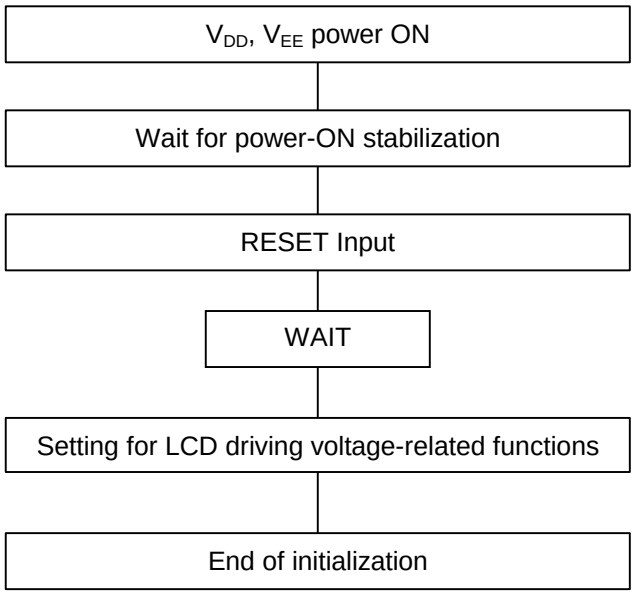
  The V_{DD} must be input first, next the reset operation must be performed, and finally the V_1 to V_4 and V_{LCD} can be turned on by setting "1" to the "DCON" and "AMPON" registers of the "Power control" instruction.

- Power supply OFF sequence

  Either the reset operation by the RESb terminal or the "Power control" instruction must be performed first, and next the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off. If the V_{EE} is supplied from different power sources for V_{DD}, the V_{EE} is turned off first, and next the V_{DD} is turned off.

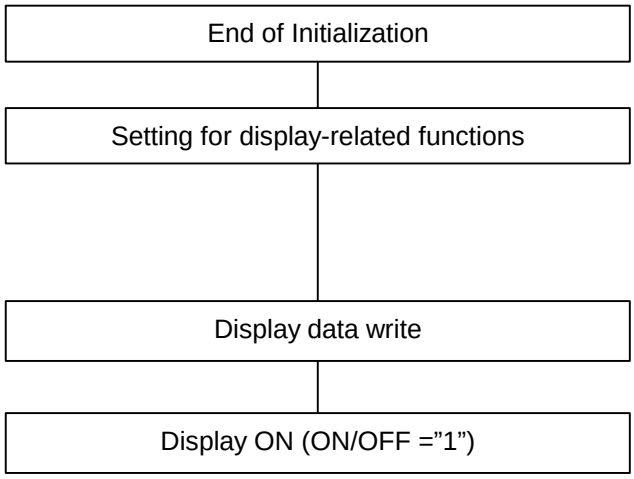
(32) Referential instruction sequences

(32-1) Initialization in using the internal power supply circuits



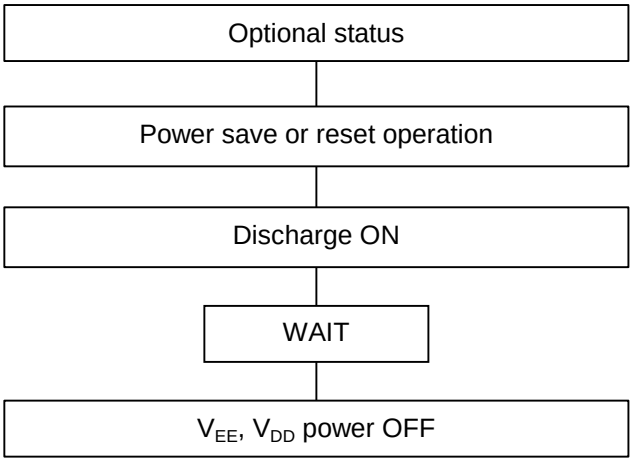
- EVR value
- LCD bias ratio
- Power control (DCON="1", AMPON="1")

(32-2) Display data writing



- Initial display line
- Increment mode
- Column address
- Row address

(32-3) Power OFF



- All COM/SEG output V_{SS} level.

(33) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
column address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
column address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	*	AX6	AX5	AX4	DDRAM column address
row address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
row address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	*	AY6	AY5	AY4	DDRAM row address
Initial display line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Row address for an initial COM line (Scan start line)
Initial display line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Row address for an initial COM line (Scan start line)
N-line inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	The number of N-line inversion
N-line inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	The number of N-line inversion
Display control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF REF: Segment direction
Increment control [AH]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Window addressing mode ON/OFF AIM: Read-modify-write ON/OFF AYI: Row auto-increment mode ON/OFF AXI: Column auto-increment mode ON/OFF
Power control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	*	DS2	DS1	DS0	Sets LCD duty cycle ratio
Boost level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Sets boost level
LCD bias ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

Note 1) * : Don't care.

Note 2) $[N_H]$: Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A0 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03	PA02	PA01	PA00	Sets palette values to gradation palette A0
Gradation palette A0 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04	Sets palette values to gradation palette A0
Gradation palette A1 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13	PA12	PA11	PA10	Sets palette values to gradation palette A1
Gradation palette A1 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14	Sets palette values to gradation palette A1
Gradation palette A2 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23	PA22	PA21	PA20	Sets palette values to gradation palette A2
Gradation palette A2 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24	Sets palette values to gradation palette A2
Gradation palette A3 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33	PA32	PA31	PA30	Sets palette values to gradation palette A3
Gradation palette A3 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34	Sets palette values to gradation palette A3
Gradation palette A4 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43	PA42	PA41	PA40	Sets palette values to gradation palette A4
Gradation palette A4 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44	Sets palette values to gradation palette A4
Gradation palette A5 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53	PA52	PA51	PA50	Sets palette values to gradation palette A5
Gradation palette A5 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54	Sets palette values to gradation palette A5
Gradation palette A6 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63	PA62	PA61	PA60	Sets palette values to gradation palette A6
Gradation palette A6 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64	Sets palette values to gradation palette A6
RE register [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

Note 1) * : Don't care.

Note 2) $[N_H]$: Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A7 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73	PA72	PA71	PA70	Sets palette values to gradation palette A7
Gradation palette A7 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74	Sets palette values to gradation palette A7
Gradation palette B0 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03	PB02	PB01	PB00	Sets palette values to gradation palette B0
Gradation palette B0 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04	Sets palette values to gradation palette B0
Gradation palette B1 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13	PB12	PB11	PB10	Sets palette values to gradation palette B1
Gradation palette B1 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14	Sets palette values to gradation palette B1
Gradation palette B2 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23	PB22	PB21	PB20	Sets palette values to gradation palette B2
Gradation palette B2 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24	Sets palette values to gradation palette B2
Gradation palette B3 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	PB33	PB32	PB31	PB30	Sets palette values to gradation palette B3
Gradation palette B3 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34	Sets palette values to gradation palette B3
Gradation palette B4 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	PB43	PB42	PB41	PB40	Sets palette values to gradation palette B4
Gradation palette B4 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44	Sets palette values to gradation palette B4
Gradation palette B5 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	PB53	PB52	PB51	PB50	Sets palette values to gradation palette B5
Gradation palette B5 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54	Sets palette values to gradation palette B5
RE register [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

Note 1) * : Don't care.

Note 2) $[N_H]$: Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette B6 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63	PB62	PB61	PB60	Sets palette values to gradation palette B6
Gradation palette B6 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64	Sets palette values to gradation palette B6
Gradation palette B7 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73	PB72	PB71	PB70	Sets palette values to gradation palette B7
Gradation palette B7 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74	Sets palette values to gradation palette B7
Gradation palette C0 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03	PC02	PC01	PC00	Sets palette values to gradation palette C0
Gradation palette C0 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04	Sets palette values to gradation palette C0
Gradation palette C1 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13	PC12	PC11	PC10	Sets palette values to gradation palette C1
Gradation palette C1 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14	Sets palette values to gradation palette C1
Gradation palette C2 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23	PC22	PC21	PC20	Sets palette values to gradation palette C2
Gradation palette C2 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24	Sets palette values to gradation palette C2
Gradation palette C3 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33	PC32	PC31	PC30	Sets palette values to gradation palette C3
Gradation palette C3 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34	Sets palette values to gradation palette C3
Gradation palette C4 (Lower) [CH]	0	1	1	0	0	1	1	1	1	0	0	PC43	PC42	PC41	PC40	Sets palette values to gradation palette C4
Gradation palette C4 (Upper) [DH]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44	Sets palette values to gradation palette C4
RE register [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette C5 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53	PC52	PC51	PC50	Sets palette values to gradation palette C5
Gradation palette C5 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54	Sets palette values to gradation palette C5
Gradation palette C6 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63	PC62	PC61	PC60	Sets palette values to gradation palette C6
Gradation palette C6 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64	Sets palette values to gradation palette C6
Gradation palette C7 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73	PC72	PC71	PC70	Sets palette values to gradation palette C7
Gradation palette C7 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74	Sets palette values to gradation palette C7
Initial COM line [6H]	0	1	1	0	1	0	0	0	1	1	0	*	SC2	SC1	SC0	Sets scan-starting common driver
EXCS control [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	*	EXCS	Controls EXCS signal
Gradation mode control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	GLSB	*	*	Sets variable or fixed gradation mode
Data bus length [9H]	0	1	1	0	1	0	0	1	0	0	1	*	*	CKS	WLS	Sets 8- or 16-bit data bus length
EVR control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [DH]	0	1	1	0	1	0	0	1	1	0	1	FFL	RF2	RF1	RF0	Oscillation frequency
Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	Discharge the electric charge in capacitors on V1 to V4 and VLCD
RE register [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag
Instruction register address [CH]	0	1	1	0	1	0	0	1	1	0	0	RA3	RA 2	RA 1	RA 0	Sets instruction register address
Instruction register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Read out instruction register data

Note 1) * : Don't care.
Note 2) $[N_H]$: Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.
Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Window end column address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	*	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LR EV	Controls reverse line display
Dummy segment register ON/OFF [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	DM Y	Controls icon segment register
PWM control [AH]	0	1	1	0	1	0	1	1	0	1	0	PW MS	PW MA	PW MB	PW MC	Sets PWM mode
RE register [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	RE flag

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(34) Instruction descriptions

This chapter provides detail descriptions and instruction registers. Nonexistent instruction codes must not be set into the LSI.

(34-1) Display data write

The “Display data write” instruction is used to write 8-bit display data into the DDRAM.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	1	0	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
Display data							

(34-2) Display data read

The “Display data read” instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address must be specified beforehand by the “column address” and “row address” instructions. The dummy read is required just after the “column address” and “row address” instructions.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(34-3) Column address

The “column address” instruction is used to specify the column address for display data’s reading and writting operations. It requires dual bytes for lower 4-bit and upper 3-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 3-bit.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX3	AX2	AX1	AX0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	AX6	AX5	AX4

(34-4) Row address

The “row address” instruction is used to specify the row address for the display data read and write operations. It requires dual bytes for lower 4-bit and upper 3-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for upper 3-bit.

The row address is specified in between 00_H and 51_H, where the address 50_H and 51_H are assigned to the PGRAM for the icon display. The setting for the nonexistent row address between 52_H and FF_H is prohibited.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY3	AY2	AY1	AY0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	AY6	AY5	AY4

(34-5) Initial display line

The “Initial display line” instruction is used to specify the line address corresponding to the initial COM line. The initial COM line specified by the “Initial COM line” instruction and indicates the common driver that starts scanning data.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA3	LA2	LA1	LA0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	LA6	LA5	LA4

LA_6	LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	1	79

(34-6) N-line inversion

The “N-line inversion” instruction is used to control the alternate rates of the liquid crystal direction. It is programmed to select the N value between 2 and 80, and the FR signal toggles once every N lines by setting “1” into the “NLIN” register of the “Display control (2)” instruction. When the N-line inversion is disabled by setting “0” into the “NLIN” register, the FR signal toggles by the frame.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N_3	N_2	N_1	N_0

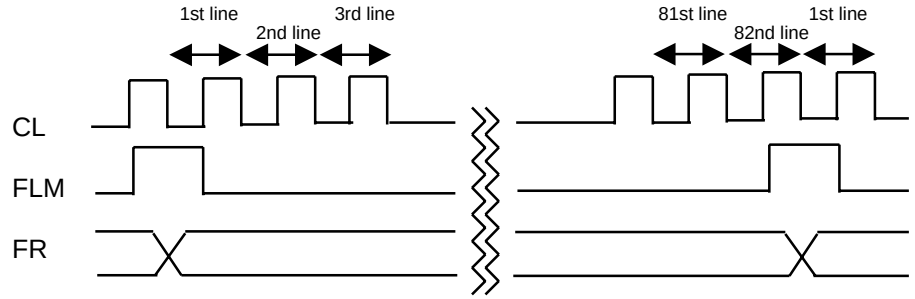
CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	N_6	N_5	N_4

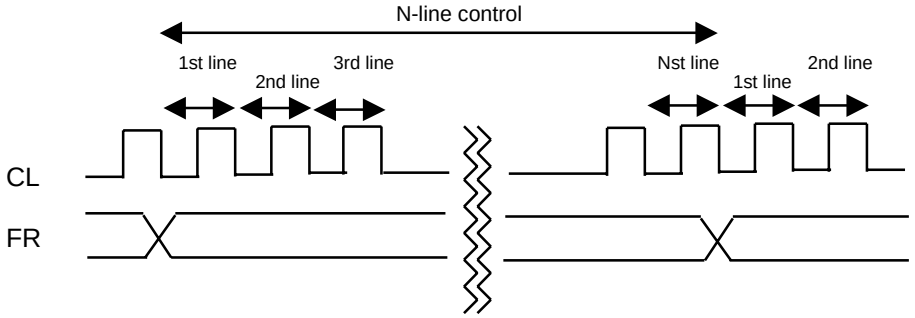
N_6	N_5	N_4	N_3	N_2	N_1	N_0	N value
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
			:				:
1	0	0	1	1	1	1	80

- N-line Inversion Timing (1/82 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(34-7) Display control (1)

The “Display control (1)” instruction is used to control display conditions by setting the “Display ON/OFF”, “All pixels ON/OFF”, Display mode” and “Common direction” registers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

- ON/OFF register

  ON/OFF=0 : Display OFF (All COM/SEG output Vss level.)
  ON/OFF=1: Display ON

- All ON register

  The “All pixels ON/OFF” register is used to turn on all pixels without changing display data of the DDRAM. The setting for the “All pixels ON/OFF” register has a priority over the “Reverse display ON/OFF” register.

  ALLON=0 : Normal
  ALLON=1 : All pixels turn on.

- MON register

  MON=0 : Gradation mode
  MON=1 : B&W mode

- SHIFT register

  SHIFT=0 : COM0 → COM79
  SHIFT=1 : COM79 → COM0

(34-8) Display control (2)

The “Display control (2)” instruction is used to control display conditions by setting the “Segment direction”, “SWAP mode ON/OFF”, “N-line inversion ON/OFF” and “Reverse display ON/OFF” registers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

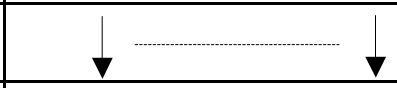
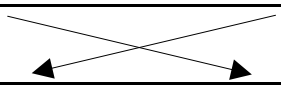
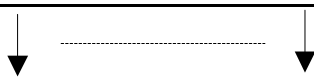
- REF register

  The “REF” register is used to reverse the assignment between segment drivers and column address, and it is possible to reduce restrictions for placement of the LSI on the LCD module. For more information, see (10) “The relation among the DDRAM column address, display data and segment drivers”.

- SWAP register

  The “SWAP” register is used to reverse the arrangement of the display data in the DDRAM.

  SWAP=0 : SWAP mode OFF (Normal)
  SWAP=1 : SWAP mode ON

	SWAP=”0”	SWAP=”1”
Write data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
		
RAM data	d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	d_0 d_1 d_2 d_3 d_4 d_5 d_6 d_7
		
Read data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

- NLIN register

  The “NLIN” is used to enable or disable the N-line inversion.

  NLIN=0 : N-line inversion OFF (The FR signal toggles by the flame.)
  NLIN=1 : N-line inversion ON (The FR signal toggles once every N frames.)

- REV register

  The “REV” register is used to enable or disable the reverse display mode that reverses the polarity of the display data without changing the display data of the DDRAM.

  REV=0 : Reverse display mode OFF
  REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(34-9) Increment control

The “Increment control” instruction is used for the increment mode. In using the auto-increment mode, DDRAM address automatically increment (+1) whenever the DDRAM is accessed by the “Display data write” or “Display data read” instruction, Therefore, once “Display data write” or “Display data read” instruction is established, it is possible to continuously access to the DDRAM without the “column address” and “row address” instructions. The settings for the “AIM”, “AXI” and “AYI” registers are listed in the following tables.

CS	RS	RD	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	WIN	AIM	AYI	AXI

- AIM, AYI and AXI registers

AIM	Increment mode	Note
0	Auto-increment for both of the display data read and write operations	-
1	Auto-increment for the display write operation (Read modify write)	-

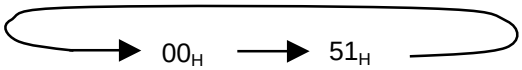
AYI	AXI	Increment mode	Note
0	0	No auto-increment	1
0	1	Auto-increment for the column address	2
1	0	Auto-increment for the row address	3
1	1	Auto-increment for the column address and row address	4

Note 1) Auto-increment is disabled independent of the “AIM” register.

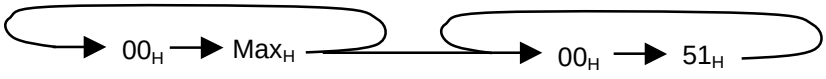
Note 2) Auto-increment of the column address is enabled in accordance with the “AIM” register.

MAXH in the 8-bit data bus mode : 7FH
MAXH in the 16-bit data bus mode : 3FH

Note 3) Auto-increment of the row address is enabled in accordance with the “AIM” register.



Note 4) Auto-increment of the column address and row address are enabled. The row address increments whenever the column address reaches to the MAX_H.



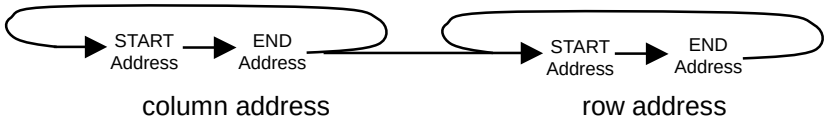
MAXH in the 8-bit data bus mode : $7F_H$
MAXH in the 16-bit data bus mode : $3F_H$

- WIN register

  The “WIN” register is used to access to the DDRAM for the window display area, where the start point is determined by the “column address” and “row address” instructions, and the end point by the “Window end column address “and ”Window end row address” instructions. The setting sequence for the window display area is listed as follows. For more detail, see (7) “Window addressing mode”.

  WIN=0 :Window addressing mode OFF
  WIN=1 :Window addressing mode ON

  1. Set WIN=1, AXI=1, and AYI=1 by “Increment control” instruction
  2. Set the start point by the “column address” and “row address” instructions
  3. Set the end point by the “Window end column address” and “Window end row address” instructions
  4. Enable to access to the DDRAM in the window addressing mode



column address row address

(34-10) Power control

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

- ACL register

  The “ACL” register is used to initialize the internal power supply circuits. It is available only in the master mode.

  ACL=0 : Initialization OFF (Normal)
  ACL=1 : Initialization ON

  When the data of the “ACL register” is read out by the “Instruction register read” instruction, the read-out data is “1” during the initialization and “0” after the initialization. This initialization is performed by using the signal produced by 2 clocks on the OSC_1. For this reason, the wait time for 2 clocks of the OSC_1 is necessary until next instruction after the initialization by programming “ACL” register.

- DCON register

  The “DCON” register is used to enable or disable the voltage booster.

  DCON=0 : Voltage booster OFF
  DCON=1 : Voltage booster ON

- HALT register

  The “HALT” register is used to enable or disable the power save mode. It is possible to reduce operating current down to stand-by level. The internal status in the power save mode is listed below.

  HALT=0 : Power save OFF (Normal)
  HALT=1 : Power save ON

  Internal status in the power save mode

  - The oscillation circuits and internal power supply circuits are halted.
  - All segment and common drivers output Vss level.
  - The clock input into the OSC_1 is inhibited.
  - The display data in the DDRAM is maintained.
  - The operational modes before the power save mode are maintained.
  - The V_1 to V_4 and V_{LCD} are in the high impedance.

  As a power save ON sequence, the “Display OFF” must be executed first, next the “Power save ON” instruction, and then all common and segment drivers output the Vss level. And as power save OFF sequence, the “Power save OFF” instruction is executed first, next the “Display ON” instruction. If the “Power save OFF” instruction is executed in the display ON status, unexpected pixels may instantly turn on.

- AMPON register

  The “AMPON” register is used to enable or disable the voltage followers, voltage regulator and EVR.

  AMPON=0 : The voltage followers, voltage regulator and the EVR OFF
  AMPON=1 : The voltage followers, voltage regulator and the EVR ON

(34-11) Duty cycle ratio

The “Duty cycle ratio” instruction is used to select LCD duty cycle ratio for the partial display function. The partial display function specifies some parts of display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. Therefore, it is possible to optimize the LSI’s conditions with extremely low power consumption.

It can be also programmed to select not only the duty cycle ratio but also the LCD bias ratio, boost level and EVR value by the instructions so that it is possible to optimize the LSI conditions in accordance with the display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	*	DS_2	DS_1	DS_0

DS_2	DS_1	DS_0	Duty cycle ratio
0	0	0	1/82
0	0	1	1/77
0	1	0	1/66
0	1	1	1/47
1	0	0	1/32
1	0	1	1/17
1	1	0	1/38
1	1	1	1/26

(34-12) Boost level

The “Boost level” is used to select the multiple of the voltage booster for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

VU_2	VU_1	VU_0	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	6-time
1	1	0	7-time
1	1	1	Inhibited

(34-13) LCD bias ratio

The “LCD bias ratio” is used to select the LCD bias ratio for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

B_2	B_1	B_0	LCD bias ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	Inhibited
1	1	1	Inhibited

(34-14) RE flag

The “RE flag” registers are used to determine the contents for the Rf registers (RE2, RE1 and RE0) and it is possible to access to the instruction registers.

The data in the “TST0” register must be “0”, and it is used only for maker tests only.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST0	RE_2	RE_1	RE_0

(34-15) Gradation palette A, B and C

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	1	0	0	0	0	PA_{03}	PA_{02}	PA_{01}	PA_{00}
0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA_{04}
0	1	1	0	0	0	1	0	0	1	0	PA_{13}	PA_{12}	PA_{11}	PA_{10}
0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA_{14}
0	1	1	0	0	0	1	0	1	0	0	PA_{23}	PA_{22}	PA_{21}	PA_{20}
0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA_{24}
0	1	1	0	0	0	1	0	1	1	0	PA_{33}	PA_{32}	PA_{31}	PA_{30}
0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA_{34}
0	1	1	0	0	0	1	1	0	0	0	PA_{43}	PA_{42}	PA_{41}	PA_{40}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA_{44}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA_{53}	PA_{52}	PA_{51}	PA_{50}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA54

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA_{63}	PA_{62}	PA_{61}	PA_{60}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA_{64}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA_{73}	PA_{72}	PA_{71}	PA_{70}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA_{74}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{03}	PB_{02}	PB_{01}	PB_{00}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{04}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB_{13}	PB_{12}	PB_{11}	PB_{10}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB_{14}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB_{23}	PB_{22}	PB_{21}	PB_{20}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB_{24}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB_{33}	PB_{32}	PB_{31}	PB_{30}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB_{34}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB_{43}	PB_{42}	PB_{41}	PB_{40}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB_{44}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB_{53}	PB_{52}	PB_{51}	PB_{50}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB_{54}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB_{63}	PB_{62}	PB_{61}	PB_{60}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB64

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{73}	PB_{72}	PB_{71}	PB_{70}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{74}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{03}	PC_{02}	PC_{01}	PC_{00}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{04}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC_{13}	PC_{12}	PC_{11}	PC_{10}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC_{14}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC_{23}	PC_{22}	PC_{21}	PC_{20}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC_{24}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC_{33}	PC_{32}	PC_{31}	PC_{30}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC_{34}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC_{43}	PC_{42}	PC_{41}	PC_{40}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC_{44}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC_{53}	PC_{52}	PC_{51}	PC_{50}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC_{54}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC_{63}	PC_{62}	PC_{61}	PC_{60}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC_{64}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{73}	PC_{72}	PC_{71}	PC_{70}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{74}

Gradation palette table (Variable gradation mode, PWM="0" and MON="0")

(Palette Aj, Palette Bj, Palette Cj (j=0 to 7))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0 0	0	Palette 0 (default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 4 (default)
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 1 (default)	1 0 1 0 1	21/31	Palette 5 (default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	Palette 2 (default)	1 1 0 1 0	26/31	Palette 6 (default)
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	Palette 3 (default)	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	Palette 7 (default)

(34-16) Initial COM line

The “Initial COM line” instruction is used to specify the common driver that starts scanning the display data. The line address, corresponding to the initial COM line, is specified by the “Initial display line” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	*	SC_2	SC_1	SC_0

SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	COM_0	COM_{79}
0	0	1	COM_{15}	COM_{64}
0	1	0	COM_{30}	COM_{49}
0	1	1	COM_{45}	COM_{34}
1	0	0	COM_{60}	COM_{19}
1	0	1	COM_{75}	COM_4
1	1	0	Inhibited	Inhibited
1	1	1	Inhibited	Inhibited

SHIFT=0: Positive direction (for instance, $COM_0 \rightarrow COM_{79}$)
SHIFT=1: Negative direction (for instance, $COM_{79} \rightarrow COM_0$)

(34-17) EXCS control

The “EXCS control” instruction is available only in the master mode, where it is used to control the polarity for the EXCS output.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	EXCS

EXCS=0: Output level “0”
EXCS=1: Output level “1”

(34-18) Gradation mode control

The “Gradation mode control” is used to determine the display data for the GLSB and select the gradation mode.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	GLSB	*	*

- GLSB register

GLSB=0: GLSB “0”
GLSB=1: GLSB “1”

- PWM register

PWM=0: Variable gradation mode
(Variable 8-gradation levels out of 32-gradation level of the gradation palette)
PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

(34-19) Data bus length

The “Data bus length” instruction is used to select the 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, instruction data must be 16-bit data (D_{15} to D_0) as well as display data. However, for the access to the instruction registers, the lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	CKS	WLS

- WLS register

  WLS =0: 8-bit data bus length
  WLS =1: 16-bit data bus length

- CKS register

  CKS =0: Internal oscillation
  (The OSC_1 and OSC_2 must be fixed “1” or “0”.)
  CKS =1: External oscillation
  (By the external clock into the OSC_1 or external resister between the OSC_1 and OSC_2.
  OSC_2 should be open when clock is inputted from OSC_1.)

(34-20) EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) so that it is possible to optimize the contrast level for a LCD panel.

This instruction must be programmed by the upper 3-bit data first, next lower 4-bit data. And it becomes enabled when the lower 4-bit data is programmed, so that it can prevent unexpected high voltage for the V_{LCD} from being generated.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV_6	DV_5	DV_4

DV_6	DV_5	DV_4	DV_3	DV_2	DV_1	DV_0	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

The formula of the V_{LCD} is shown below.

VLCD [V] = 0.5 x VREG + M (VREG – 0.5 x VREG) / 127

$V_{BA} = V_{EE} \times 0.9$
$V_{REG} = V_{REF} \times N$

V_{BA} : Output voltage of the reference voltage generator
V_{REF} : Input voltage of the voltage regulator
V_{REG} : Output voltage of the voltage regulator
N : Register value for the voltage booster
M : Register value for the EVR

(34-21) Frequency control

The “Frequency control” instruction is used to control the frame frequency for a LCD panel.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	FFL	Rf2	Rf1	Rf0

- Rfx register (x=0, 1, 2)

  The “Rfx” register is used to determine the feed back resister value for the internal oscillator and it is possible to adjust the frame frequency for the LCD modules.

Rf_2	Rf_1	Rf_0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

- FFL register

  The “FFL” register is used to select normal or high-speed frame frequency mode.

  FFL =0: Normal (Frame frequency: 73Hz typical)
  FFL =1: High-speed mode (Frame frequency: 150Hz typical)

Note) The above values for the typical frame frequency are based on the following conditions.
Variable gradation mode, 1/82 duty cycle ratio, (Rf_2, Rf_1, Rf_0) = (0,0,0)

(34-22) Discharge ON/OFF

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and the V_{LCD} terminals. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	*	DIS

DIS =0: Discharge OFF
DIS =1: Discharge ON

(34-23) Instruction register address

The “Instruction register address” is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the “Instruction register read” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA_3	RA_2	RA_1	RA_0

(34-24) Instruction register read

The “Instruction register read” instruction is used to read out the contents of the instruction register in combination with the “Instruction register address” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data read			

(34-25) Window end column address

The “Window end column address” is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX_3	EX_2	EX_1	EX_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	EX_6	EX_5	EX_4

(34-26) Window end row address set

The “Window end row address” is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY_3	EY_2	EY_1	EY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	EY_6	EY_5	EY_4

(34-27) Initial reverse line

The “Initial reverse line” instruction is used to specify the initial line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 3-bit data. It is programmed in between 00_H and $4F_H$ and the line address beyond $4F_H$ is inhibited. The address relation: LSi < LEi (i=6 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS_3	LS_2	LS_1	LS_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	LS_6	LS_5	LS_4

(34-28) Last reverse line

The “Last reverse line” instruction is used to specify the last reverse line address for the reverse line display. Lower 4-bit must be programmed first, next upper 3-bit data. It is programmed in between 00_H and $4F_H$ and the line address beyond $4F_H$ is inhibited. The address relation: LSi < LEi (i=6 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE_3	LE_2	LE_1	LE_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	LE_6	LE_5	LE_4

(34-29) Reverse line display ON/OFF

The “Reverse line display ON/OFF” is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

- LREV register

The “LREV” register is used to enable or disable the reverse line display.

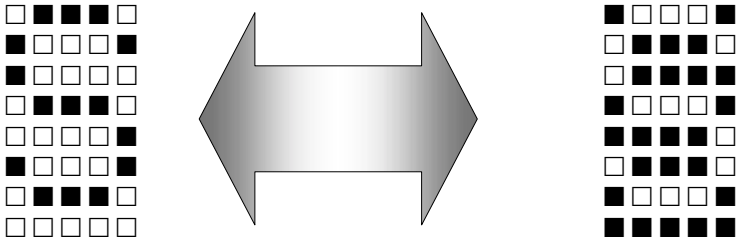
LREV =0: Reverse line display OFF (Normal)
LREV =1: Reverse line display ON

- BT register

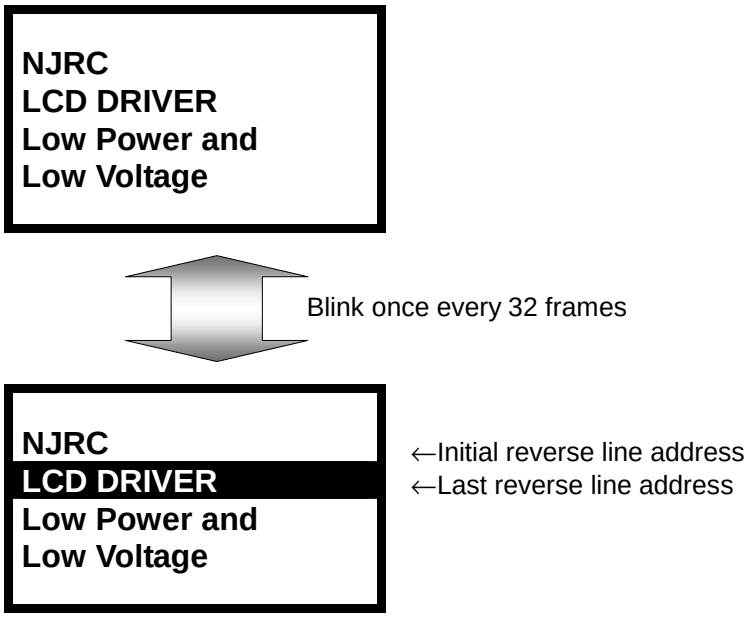
  The “BT” register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

  BT =0: Normal reverse line display
  BT =1: Blink once every 32 frames

Display examples in the LREV=”1” and BT=”1”



Blink once every 32 frames



(34-30) Icon segment register ON/OFF

The “Icon segment address ON/OFF” is used to enable or disable to access to the icon segment register.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	DMY

- DMY register

  DMY=0: Access to the DDRAM
  DMY=1: Access to the icon segment register

(34-31) PWM control

The “PWM control” is used to determine the PWM type for the segment waveforms, where the type can be specified for each of the SEGAi, SEGBi and SEGCi (i=0-127) drivers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

- PWMS register

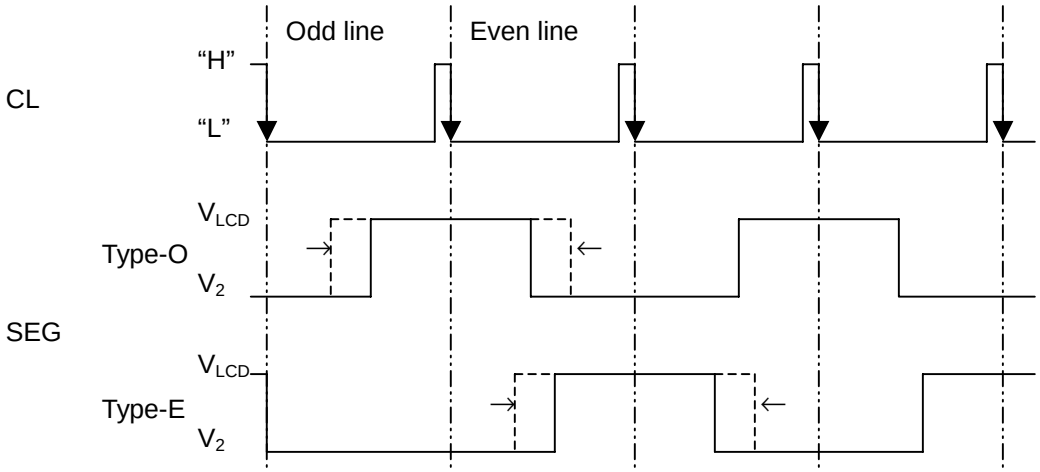
  PWMS=0: Type 1
  PWMS=1: Type 2

- PWMA, B and C registers

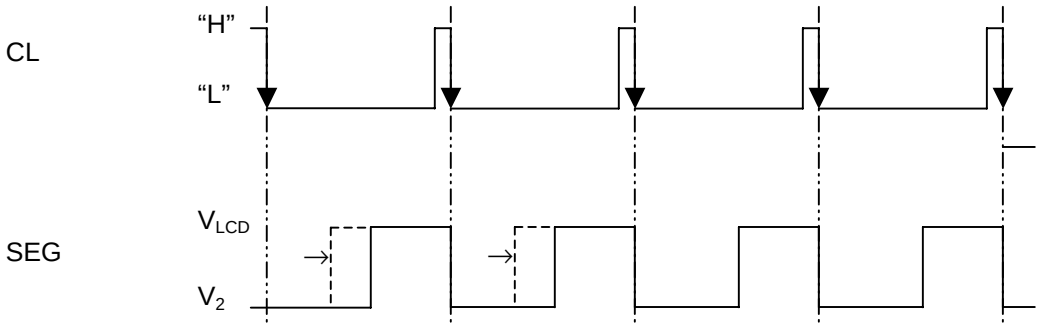
  The “PWMA, PWMB and PWMC” registers are used to select the type 1-O or type 1-E.

  PWMZ=0 (Z=A, B and C): Type 1-O
  PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS=”0”)



PWM type2 (PWMS=”1”)



(35) The relationship between Common drivers and row addresses

Row address assignment for common drivers is programmed by the “SHIF” register of the “Display control (1), and “Duty cycle ratio”, “Initial display line” and “Initial COM line” instructions. The assignment for the $COMI_0$ and $COMI_1$ are independent of these instructions and always fixed.

- When initial display line is “0”

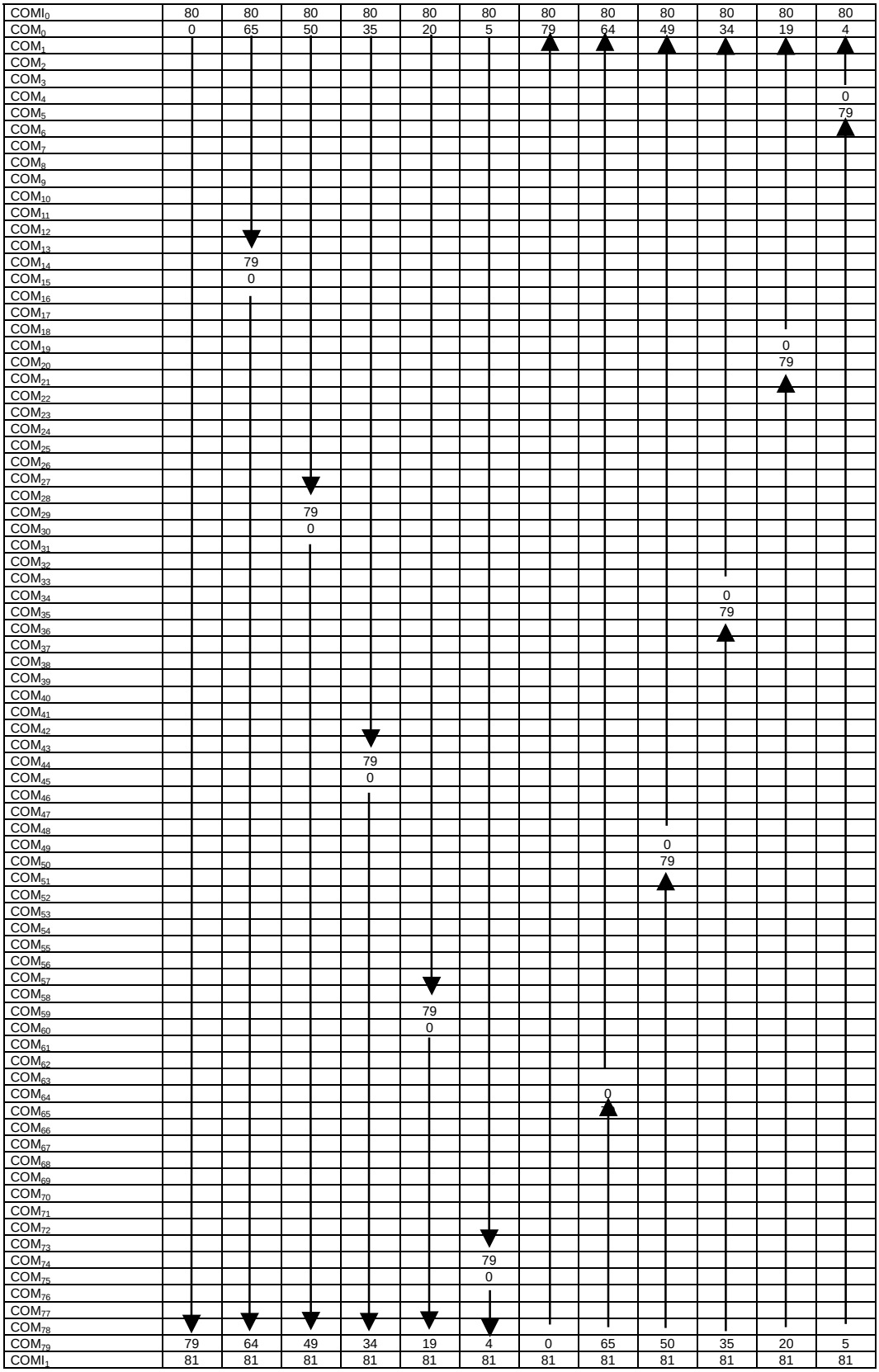
The relation between common drivers and row address of DDRAM (MY) is changing each 15dots unit by the “Duty cycle ratio” and “Initial COM line” instructions. If the shift bit is “0”, the order of common scanning is normal and if it is “1”, the common scanning order is inversed. When LA_0 to LA_6 of initial display line setting is “0”, the “MY” corresponding to the Initial COM line is also “0”. And “MY” is increasing.
Regardless above, $COMI_0$ and $COMI_1$ is fixed to MY_{80} and MY_{81} respectively.

- When initial display line is not “0”

The relation between common drivers and row address of DDRAM (MY) is changing each 15dots unit by the “Duty cycle ratio” and “Initial COM line” instructions. If the shift bit is “0”, the order of common scanning is normal and if it is “1”, the common scanning order is inversed. When LA0 to LA6 of initial display line setting is not “0”, the “MY” corresponding to the Initial COM line is biased by the setting value. During the display, “MY” is increasing up to “79”. When “MY” over than “79”, its back to “0”. And “MY” is increasing from 0 continuously.
Regardless above, $COMI_0$ and $COMI_1$ is fixed to MY_{80} and MY_{81} respectively.

(35-1) Initial display line “0”, 1/82 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“000” (1/82 duty)						“000” (1/82 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					



DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-2) Initial display line “0”, 1/77 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“001” (1/77 duty)						“001” (1/77 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0	65	50	35	20	5		64	49	34	19	4	
COM_1													
COM_2													
COM_3													
COM_4													0
COM_5							74						
COM_6													
COM_7													
COM_8													
COM_9		74											
COM_{10}													74
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												0	
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}			74										
COM_{25}												74	
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											0		
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}				74									
COM_{40}											74		
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}										0			
COM_{50}													
COM_{51}													
COM_{52}						74							
COM_{53}													
COM_{54}						74							
COM_{55}										74			
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}						0							
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}									0				
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}							74						
COM_{70}									74				
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}	74												
COM_{75}							0						
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}		64	49	34	19	4	0	65	50	35	20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-3) Initial display line “0”, 1/66 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“010” (1/66 duty)						“010” (1/66 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0		50	35	20	5			49	34	19	4
COM_1								63				
COM_2												
COM_3												
COM_4												0
COM_5												
COM_6												
COM_7												
COM_8												
COM_9												
COM_{10}												
COM_{11}												
COM_{12}												
COM_{13}			63									
COM_{14}												
COM_{15}		0										
COM_{16}							63					
COM_{17}												
COM_{18}												
COM_{19}											0	
COM_{20}												
COM_{21}												63
COM_{22}												
COM_{23}												
COM_{24}												
COM_{25}												
COM_{26}												
COM_{27}												
COM_{28}				63								
COM_{29}												
COM_{30}			0									
COM_{31}												
COM_{32}												
COM_{33}												
COM_{34}										0		
COM_{35}												
COM_{36}											63	
COM_{37}												
COM_{38}												
COM_{39}												
COM_{40}												
COM_{41}												
COM_{42}												
COM_{43}					63							
COM_{44}												
COM_{45}				0								
COM_{46}												
COM_{47}												
COM_{48}												
COM_{49}										0		
COM_{50}												
COM_{51}											63	
COM_{52}												
COM_{53}												
COM_{54}												
COM_{55}												
COM_{56}												
COM_{57}												
COM_{58}							63					
COM_{59}												
COM_{60}						0						
COM_{61}												
COM_{62}												
COM_{63}	63											
COM_{64}										0		
COM_{65}												
COM_{66}											63	
COM_{67}												
COM_{68}												
COM_{69}												
COM_{70}												
COM_{71}												
COM_{72}												
COM_{73}												
COM_{74}												
COM_{75}							0					
COM_{76}												
COM_{77}												
COM_{78}		63										
COM_{79}			49	34	19	4	0		50	35	20	5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-4) Initial display line “0”, 1/47 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“011” (1/47 duty)						“011” (1/47 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0			35	20	5				34	19	4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5											44		
COM_6													
COM_7													
COM_8													
COM_9				44									
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												0	
COM_{20}										44			
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}					44								
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}									44				
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}						44							
COM_{40}													44
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}	44												
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}												44	
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}		44											
COM_{60}					0								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}												44	
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}			44										
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}				34	19	4	0			35	20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-5) Initial display line “0”, 1/32 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“100” (1/32 duty)						“100” (1/32 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	0				20	5					19	4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5											29		
COM_6													
COM_7													
COM_8													
COM_9					29								
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											0		
COM_{20}										29			
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}						29							
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}	29												
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											0		
COM_{35}										29			
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}		29											
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}									29				
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													29
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}			29										
COM_{60}					0								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}												29	
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}				29									
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}					19	4	0				20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-6) Initial display line “0”, 1/17 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“101” (1/17 duty)						“101” (1/17 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	0					5						4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5											14		
COM_6													
COM_7													
COM_8													
COM_9						14							
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}	14												
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											0		
COM_{20}												14	
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}		14											
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}											14		
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}			14										
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}										14			
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}				14									
COM_{60}					0								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}									14				
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													14
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}					14								
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}						4		0					5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-7) Initial display line “0”, 1/38 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“110” (1/38 duty)						“110” (1/38 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	0			35	20	5				34	19	4	
COM_1													
COM_2													
COM_3													
COM_4												0	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}											35		
COM_{15}		0			35								
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}												0	
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}										35			
COM_{30}			0			35							
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												0	
COM_{35}	35												
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}									35				
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		35
COM_{50}		35											
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}					0								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										0		35	
COM_{65}			35										
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}						0							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}				34	19	4	0				35	20	5
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-8) Initial display line “0”, 1/26 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“111” (1/26 duty)						“111” (1/26 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000000” (Initial display line 0)						“0000000” (Initial display line 0)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	0				20	5					19	4	
COM_1													
COM_2													
COM_3					23								
COM_4												0	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}											23		
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		0											
COM_{16}													
COM_{17}													
COM_{18}						23							
COM_{19}											0		
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}	23												
COM_{24}													
COM_{25}													
COM_{26}										23			
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			0										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											0		
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}		23											
COM_{39}													
COM_{40}													
COM_{41}										23			
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}				0									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											0		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}			23										
COM_{54}													
COM_{55}													
COM_{56}									23				
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}					0								
COM_{61}												23	
COM_{62}													
COM_{63}													
COM_{64}										0			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}				23									
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}						0							
COM_{76}											23		
COM_{77}													
COM_{78}													
COM_{79}					19	4	0				20	5	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-9) Initial display line “5”, 1/82 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“000” (1/82 duty)						“000” (1/82 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	5	70	55	40	25	10	4	69	54	39	24	9	
COM_1													
COM_2													
COM_3													
COM_4							0					5	
COM_5							79						
COM_6													
COM_7													
COM_8													
COM_9		79										0	
COM_{10}		0										79	
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											5		
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}			79								0		
COM_{25}			0								79		
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}										5			
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}				79						0			
COM_{40}				0						79			
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}									5				
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}					79				0				
COM_{55}					0				79				
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}					5								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}								5					
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}						79		0					
COM_{70}						0		79					
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}	79												
COM_{75}	0					5							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}	4	69	54	39	24	9	5	70	55	40	25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-10) Initial display line “5”, 1/77 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“001” (1/77 duty)						“001” (1/77 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5	70	55	40	25	10		69	54	39	24	9		
COM_1														
COM_2														
COM_3														
COM_4													5	
COM_5							79							
COM_6														
COM_7														
COM_8														
COM_9		79												
COM_{10}														79
COM_{11}														
COM_{12}														
COM_{13}														
COM_{14}														
COM_{15}		5												
COM_{16}														
COM_{17}														
COM_{18}														
COM_{19}												5		
COM_{20}														
COM_{21}														
COM_{22}														
COM_{23}														
COM_{24}			79											
COM_{25}												79		
COM_{26}														
COM_{27}														
COM_{28}														
COM_{29}														
COM_{30}			5											
COM_{31}														
COM_{32}														
COM_{33}														
COM_{34}												5		
COM_{35}														
COM_{36}														
COM_{37}														
COM_{38}														
COM_{39}				79										
COM_{40}												79		
COM_{41}														
COM_{42}														
COM_{43}														
COM_{44}														
COM_{45}				5										
COM_{46}														
COM_{47}														
COM_{48}														
COM_{49}											5			
COM_{50}														
COM_{51}														
COM_{52}														
COM_{53}														
COM_{54}							79							
COM_{55}											79			
COM_{56}														
COM_{57}														
COM_{58}														
COM_{59}														
COM_{60}							5							
COM_{61}														
COM_{62}														
COM_{63}														
COM_{64}										5				
COM_{65}														
COM_{66}														
COM_{67}														
COM_{68}														
COM_{69}							79							
COM_{70}										79				
COM_{71}														
COM_{72}														
COM_{73}														
COM_{74}	79													
COM_{75}							5							
COM_{76}														
COM_{77}														
COM_{78}														
COM_{79}		69	54	39	24	9	5	70	55	40	25	10		
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-11) Initial display line “5”, 1/66 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“010” (1/66 duty)						“010” (1/66 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5		55	40	25	10			54	39	24	9	
COM_1								68					
COM_2													
COM_3													
COM_4													5
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}			68										
COM_{14}													
COM_{15}		5											
COM_{16}								68					
COM_{17}													
COM_{18}													
COM_{19}												5	
COM_{20}													
COM_{21}													68
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}				68									
COM_{29}													
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												5	
COM_{35}													
COM_{36}													68
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}						68							
COM_{44}													
COM_{45}					5								
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}													
COM_{51}												68	
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}							68						
COM_{59}													
COM_{60}						5							
COM_{61}													
COM_{62}													
COM_{63}	68												
COM_{64}										5			
COM_{65}													
COM_{66}											68		
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}							5						
COM_{76}													
COM_{77}													
COM_{78}		68											
COM_{79}			54	39	24	9	5		55	40	25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-12) Initial display line “5”, 1/47 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“011” (1/47 duty)						“011” (1/47 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5			40	25	10				39	24	9	
COM_1													
COM_2													
COM_3													
COM_4												5	
COM_5									49				
COM_6													
COM_7													
COM_8													
COM_9				49									
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											5		
COM_{20}									49				
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}					49								
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												5	
COM_{35}									49				
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}						49							
COM_{40}													49
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}	49												
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}												49	
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}		49											
COM_{60}					5								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}												49	
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}			49										
COM_{75}						5							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}				39	24	9	5			40	25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-13) Initial display line “5”, 1/32 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“100” (1/32 duty)						“100” (1/32 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	5				25	10					24	9	
COM_1													
COM_2													
COM_3													
COM_4												5	
COM_5											34		
COM_6													
COM_7													
COM_8													
COM_9					34								
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											5		
COM_{20}										34			
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}						34							
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}	34												
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											5		
COM_{35}										34			
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}		34											
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}									34				
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}												34	
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}			34										
COM_{60}					5								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}												34	
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}				34									
COM_{75}						5							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}					24	9	5				25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-14) Initial display line “5”, 1/17 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” Common backward scan)					
DS_2	DS_1	DS_0	“101” (1/17 duty)						“101” (1/17 duty)					
SC_2	SC1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	5					10						9	
COM_1													
COM_2													
COM_3													
COM_4												5	
COM_5											19		
COM_6													
COM_7													
COM_8													
COM_9						19							
COM_{10}													
COM_{11}													
COM_{12}													
COM_{13}													
COM_{14}	19												
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}													
COM_{19}											5		
COM_{20}												19	
COM_{21}													
COM_{22}													
COM_{23}													
COM_{24}													
COM_{25}													
COM_{26}													
COM_{27}													
COM_{28}													
COM_{29}		19											
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}												5	
COM_{35}											19		
COM_{36}													
COM_{37}													
COM_{38}													
COM_{39}													
COM_{40}													
COM_{41}													
COM_{42}													
COM_{43}													
COM_{44}			19										
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}										19			
COM_{51}													
COM_{52}													
COM_{53}													
COM_{54}													
COM_{55}													
COM_{56}													
COM_{57}													
COM_{58}													
COM_{59}				19									
COM_{60}					5								
COM_{61}													
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}									19				
COM_{66}													
COM_{67}													
COM_{68}													
COM_{69}													
COM_{70}													19
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}					19								
COM_{75}						5							
COM_{76}													
COM_{77}													
COM_{78}													
COM_{79}						9	5						10
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-15) Initial display line “5”, 1/38 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“110” (1/38 duty)						“110” (1/38 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM_0	5			40	25	10						39	24	9
COM_1														
COM_2														
COM_3														
COM_4														5
COM_5														
COM_6														
COM_7														
COM_8														
COM_9														
COM_{10}														
COM_{11}														
COM_{12}														
COM_{13}														
COM_{14}											40			
COM_{15}		5			40									
COM_{16}														
COM_{17}														
COM_{18}														
COM_{19}													5	
COM_{20}														
COM_{21}														
COM_{22}														
COM_{23}														
COM_{24}														
COM_{25}														
COM_{26}														
COM_{27}														
COM_{28}														
COM_{29}										40				
COM_{30}			5			40								
COM_{31}														
COM_{32}														
COM_{33}														
COM_{34}												5		
COM_{35}	40													
COM_{36}														
COM_{37}														
COM_{38}														
COM_{39}														
COM_{40}														
COM_{41}														
COM_{42}														
COM_{43}														
COM_{44}									40					
COM_{45}				5										
COM_{46}														
COM_{47}														
COM_{48}														
COM_{49}											5			40
COM_{50}		40												
COM_{51}														
COM_{52}														
COM_{53}														
COM_{54}														
COM_{55}														
COM_{56}														
COM_{57}														
COM_{58}														
COM_{59}														
COM_{60}					5									
COM_{61}														
COM_{62}														
COM_{63}														
COM_{64}										5			40	
COM_{65}			40											
COM_{66}														
COM_{67}														
COM_{68}														
COM_{69}														
COM_{70}														
COM_{71}														
COM_{72}														
COM_{73}														
COM_{74}														
COM_{75}						5								
COM_{76}														
COM_{77}														
COM_{78}														
COM_{79}				39	24	9	5					40	25	10
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	81	81

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

(35-16) Initial display line “5”, 1/26 duty cycle

SHIFT set value			SHIFT=”0” (Common forward scan)						SHIFT=”1” (Common backward scan)					
DS_2	DS_1	DS_0	“111” (1/26 duty)						“111” (1/26 duty)					
SC_2	SC_1	SC_0	“000”	“001”	“010”	“011”	“100”	“101”	“000”	“001”	“010”	“011”	“100”	“101”
LA_6	·····	LA_0	“0000101” (Initial display line 5)						“0000101” (Initial display line 5)					

$COMI_0$	80	80	80	80	80	80	80	80	80	80	80	80	
COM_0	5				25	10					24	9	
COM_1													
COM_2													
COM_3					28								
COM_4												5	
COM_5													
COM_6													
COM_7													
COM_8													
COM_9													
COM_{10}													
COM_{11}											28		
COM_{12}													
COM_{13}													
COM_{14}													
COM_{15}		5											
COM_{16}													
COM_{17}													
COM_{18}						28							
COM_{19}											5		
COM_{20}													
COM_{21}													
COM_{22}													
COM_{23}	28												
COM_{24}													
COM_{25}													
COM_{26}											28		
COM_{27}													
COM_{28}													
COM_{29}													
COM_{30}			5										
COM_{31}													
COM_{32}													
COM_{33}													
COM_{34}											5		
COM_{35}													
COM_{36}													
COM_{37}													
COM_{38}		28											
COM_{39}													
COM_{40}													
COM_{41}										28			
COM_{42}													
COM_{43}													
COM_{44}													
COM_{45}				5									
COM_{46}													
COM_{47}													
COM_{48}													
COM_{49}											5		
COM_{50}													
COM_{51}													
COM_{52}													
COM_{53}			28										
COM_{54}													
COM_{55}													
COM_{56}									28				
COM_{57}													
COM_{58}													
COM_{59}													
COM_{60}					5								
COM_{61}												28	
COM_{62}													
COM_{63}													
COM_{64}										5			
COM_{65}													
COM_{66}													
COM_{67}													
COM_{68}				28									
COM_{69}													
COM_{70}													
COM_{71}													
COM_{72}													
COM_{73}													
COM_{74}													
COM_{75}						5							
COM_{76}											28		
COM_{77}													
COM_{78}													
COM_{79}					24	9	5				25	10	
$COMI_1$	81	81	81	81	81	81	81	81	81	81	81	81	

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +20.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +20.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	VI		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}			-45 to +125	°C

Note 1) D_0 to D_{15}, CSb, RS, M/S, RDb, WRb, OSC_1, CL, FLM, FR, CLK, RESb, TEST terminals.
Note 2) To stabilize the voltage booster operation, decoupling capacitors must be connected between the V_{DD} and V_{SS} pins and between the V_{EE} and V_{SSH} pins.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	°C	

Note1) Applies to the condition when the reference voltage generator is not used.
Note2) Applies to the condition when the reference voltage generator is used.
Note3) Applies to the condition when the voltage booster is used.
Note4) The following relationship among the supply voltages must be maintained.
$V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}\leq V_{OUT}$
Note5) The relationship: $V_{REF}<V_{EE}$ must be maintained.

■ DC CHARACTERISTICS 1

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.22V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4 mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1 mA				0.4	V	*3
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	|ΔV_{ON}| = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CSb=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C	FFL = "0" (Standard)	305	372	439	kHz	*8
	f_{OSC2}			68	84	99.2		*9
	f_{OSC3}			9.8	12	14.2		*10
	f_{OSC4}		FFL = "1" (Hi-speed)	625.3	762.6	899.9		*8
	f_{OSC5}			141.2	172.2	203.2		*9
	f_{OSC6}			20.1	24.6	29.1		*10
External oscillation Frequency	fr_1	Rf=10kΩ		726	807	888	kHz	*16
	fr_2	Rf=20kΩ		401	445	490		
	fr_3	Rf=51kΩ		175	194	213		
	fr_4	Rf=110kΩ		86.2	95.8	105.4		
	fr_5	Rf=390kΩ		25.2	28	30.8		
	fr_6	Rf=820kΩ		12	13.3	14.6		
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 7) RL = 500kΩ (VOUT - VSS)		N x V_{EE} x 0.95			V	*11
Supply current (1)	I_{DD1}	V_{DD} = 2.5V 7-time booster (Whole ON pattern)	FFL = "0"		580	870	µA	*12
Supply current (2)	I_{DD2}		FFL = "1"		870	1300		
Supply current (3)	I_{DD3}	V_{DD} = 2.5V 7-time booster (Checker pattern)	FFL = "0"		670	1010		
Supply current (4)	I_{DD4}		FFL = "1"		1060	1590		
Supply current (5)	I_{DD5}	V_{DD} = 3V 6-time booster (Whole ON pattern)	FFL = "0"		490	740		
Supply current (6)	I_{DD6}		FFL = "1"		760	1140		
Supply current (7)	I_{DD7}	V_{DD} = 3V 6-time booster (Checker pattern)	FFL = "0"		580	870		
Supply current (8)	I_{DD8}		FFL = "1"		930	1400		
Supply current (9)	I_{DD9}	V_{DD} = 3V 5-time booster (Whole ON pattern)	FFL = "0"		330	500		
Supply current (10)	I_{DD10}		FFL = "1"		520	780		
Supply current (11)	I_{DD11}	V_{DD} = 3V 5-time booster (Checker pattern)	FFL = "0"		390	590		
Supply current (12)	I_{DD12}		FFL = "1"		650	980		
Supply current (13)	I_{DD13}	V_{DD} = 3V 4-time booster (Whole ON pattern)	FFL = "0"		220	330		
Supply current (14)	I_{DD14}		FFL = "1"		360	540		
Supply current (15)	I_{DD15}	V_{DD} = 3V 4-time booster (Checker pattern)	FFL = "0"		260	390		
Supply current (16)	I_{DD16}		FFL = "1"		450	680		
VBA Operating Voltage	V_{BA}	V_{EE} = 2.4 to 3.3V		(0.9 V_{EE}) x 0.98	0.9 V_{EE}	(0.9 V_{EE}) x 1.02	V	*13
VREG Operating Voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 0.9 x VEE N-time booster (N=2 to 7)		(V_{REF} ×N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*14

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Output voltage	V_2		-100	0	+100	mV	*15
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYNBOL	Display mode	Display duty cycle ratio (1/D)			NOTE
			1/82, 1/77, 1/66	1/47, 1/38, 1/32, 1/26	1/17	
Internal clock	f_{OSC}	Gradation mode	f_{OSC} / (62xD)	f_{OSC} / (62xDx2)	f_{OSC} / (62xDx4)	FLM
		Simplified gradation mode	f_{OSC} / (14xD)	f_{OSC} / (14xDx2)	f_{OSC} / (14xDx4)	
		B&W mode	f_{OSC} / (2xD)	f_{OSC} / (2xDx2)	f_{OSC} / (2xDx4)	
External clock	f_{CK}	Gradation mode	f_{CK} / (62xD)	f_{CK} / (62xDx2)	f_{CK} / (62xDx4)	
		Simplified gradation mode	f_{CK} / (14xD)	f_{CK} / (14xDx2)	f_{CK} / (14xDx4)	
		B&W mode	f_{CK} / (2xD)	f_{CK} / (2xDx2)	f_{CK} / (2xDx4)	

APPLIED TERMINALS and CONDITIONS

Note 1) D_0-D_{15}, CSb, RS, M/S, RDb, WRb, P/S, SEL68, CLK, CL, FLM, FR, RESb

Note 2) D_0-D_{15}

Note 3) CL, FLM, FR, CLK

Note 4) CSb, RS, M/S, SEL68, RDb, WRb, P/S, RESb, OSC_1

Note 5) D_0-D_{15}, CL, FLM, FR, CLK in the high impedance

Note 6) $SEGA_0$-$SEGA_{127}$, $SEGB_0$-$SEGB_{127}$, $SEGC_0$-$SEGC_{127}$, COM_0-COM_{79}, $COMI_0$, $COMI_1$
- Defines the resistance between the COM/SEG terminals and the power supply terminals (V_{LCD}, V_1, V_2, V_3 and V_4) at the condition of 0.5V deference and 1/9 LCD bias ratio.

Note 7) V_{DD}
- The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers.

Note 8) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the variable gradation mode.

Note 9) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the fixed gradation mode.

Note 10) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(1,0,0) (12kHz),
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,1,1) (24kHz),
in the black and white mode.

Note 11) V_{OUT}
- Applies to the condition when the internal voltage booster (N=2-7), the internal oscillator and the internal power circuits are used.
- V_{EE}=2.4V to 3.3V, EVR= (1,1,1,1,1,1,1)
- 1/5 to 1/10 LCD bias, 1/82 duty cycle, No-load on the COM/SEG drivers.
- RL=500Kohm between V_{OUT} and V_{SS}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1"

Note 12) V_{DD}
- Applies to the condition using the internal oscillator and internal power circuits, no accsess between the LSI and MPU.
- EVR= (1,1,1,1,1,1,1), All pixels turned-on or checkerboard display in gradation mode.
- 1/82 duty cycle, No-load on the COM/SEG drivers
- V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1", NLIN="0",
1/82 Duty, Ta=25°C

Note 13) V_{REG}

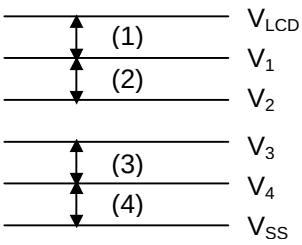
- Applies to the condition that $V_{BA}=V_{REF}$ and voltage booster N= 1.
DCON="0", V_{OUT}=13.5V input.

Note 14) V_{REG}

- V_{EE}=2.4V to 3.3V, V_{REF}=0.9VEE, V_{OUT}=18.0V, 1/5 to 1/10 LCD bias ratio, 1/82 duty cycle, EVR=(1,1,1,1,1,1,1)
- Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 7
$CA_1=CA_2$=1.0 uF, CA_3=0.1 uF, DCON="0", AMPON="1", NLIN="0"

Note 15) V_{LCD}, V_1, V_2, V_3, V_4

- V_{EE} = 3.0V, V_{REF} = 0.9 V_{EE}, V_{OUT} =15.0V, bias=1/5~1/10, EVR= "1111111".
Display OFF, No-load on the COM/SEG drivers, the voltage booster N=5
CA_2=1.0µF, CA_3=0.1µF, DCON="0", AMPON="1"

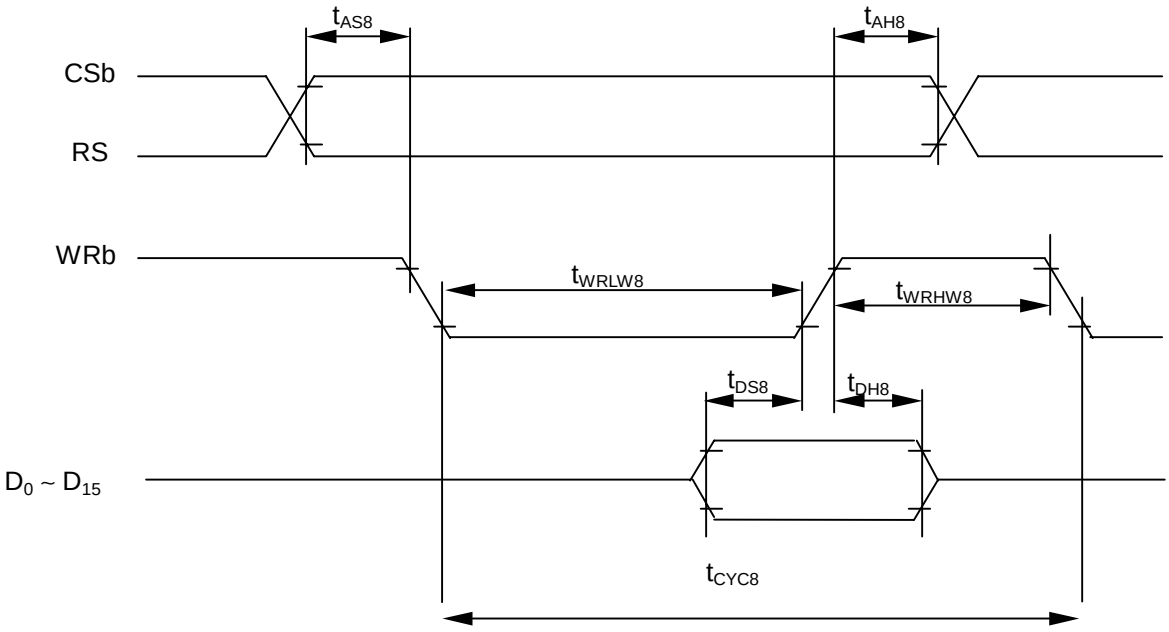


V_{D12} : (1) – (2)
V_{D34} : (3) – (4)
V_{D24} : (2) – (4)

Note 16) V_{DD}=3V, Ta=25°C

■ AC CHARACTERISTERISTICS

● **Write operation (80-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

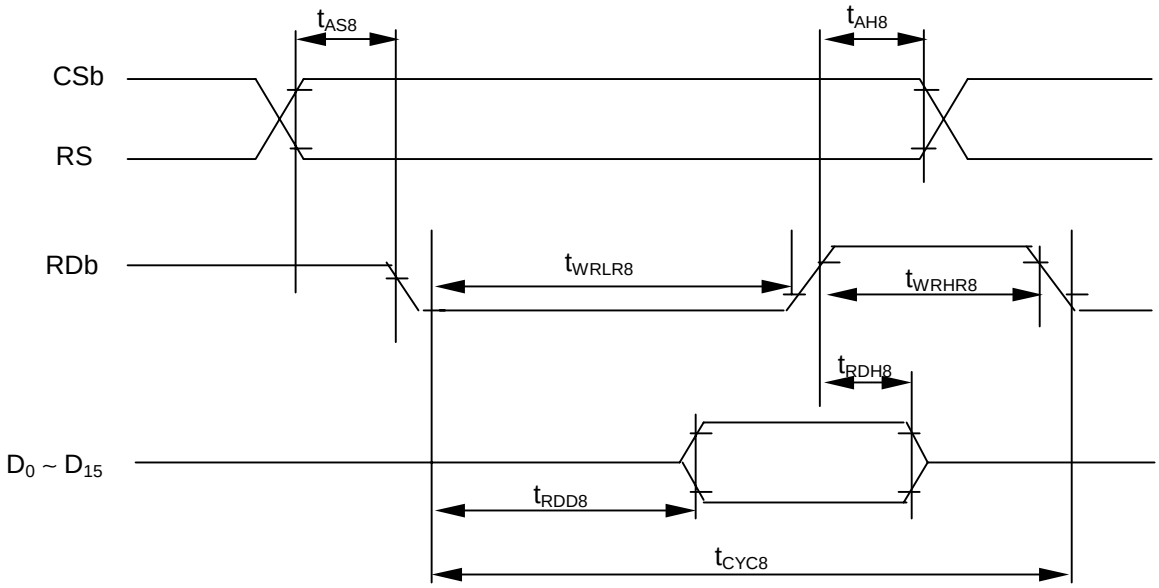
PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (80-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

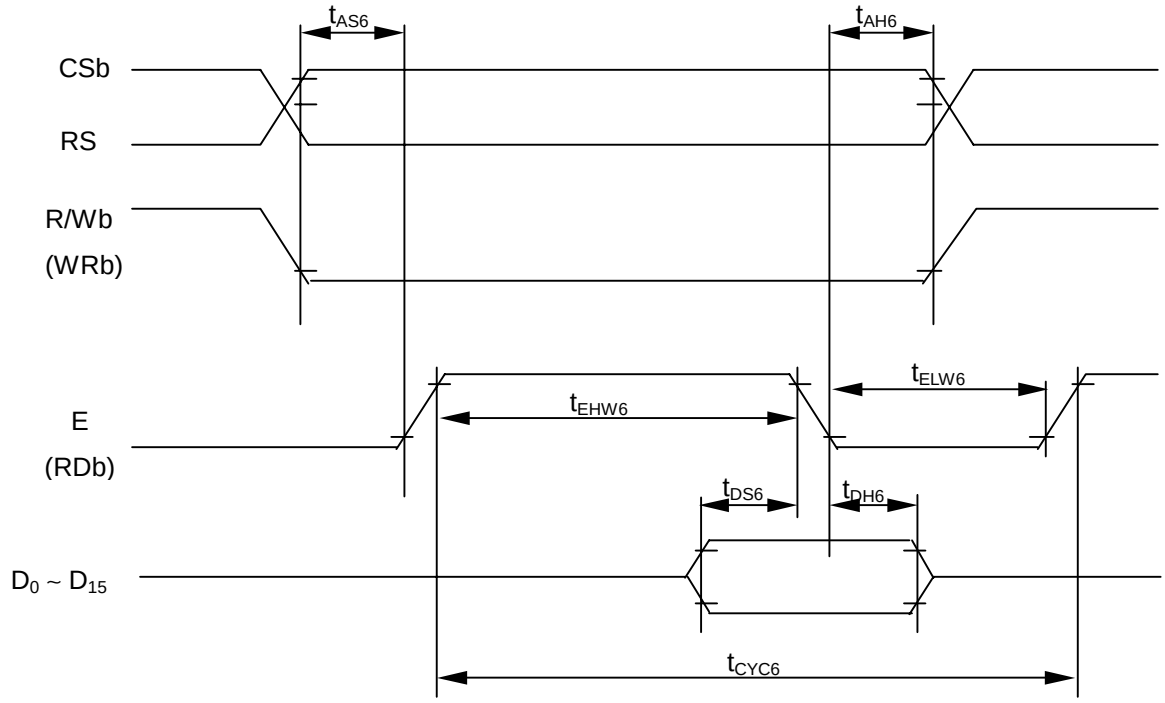
PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	110	ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Write operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		90 35 35		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=2.4 to 2.7V, Ta=-30 to +85°C)

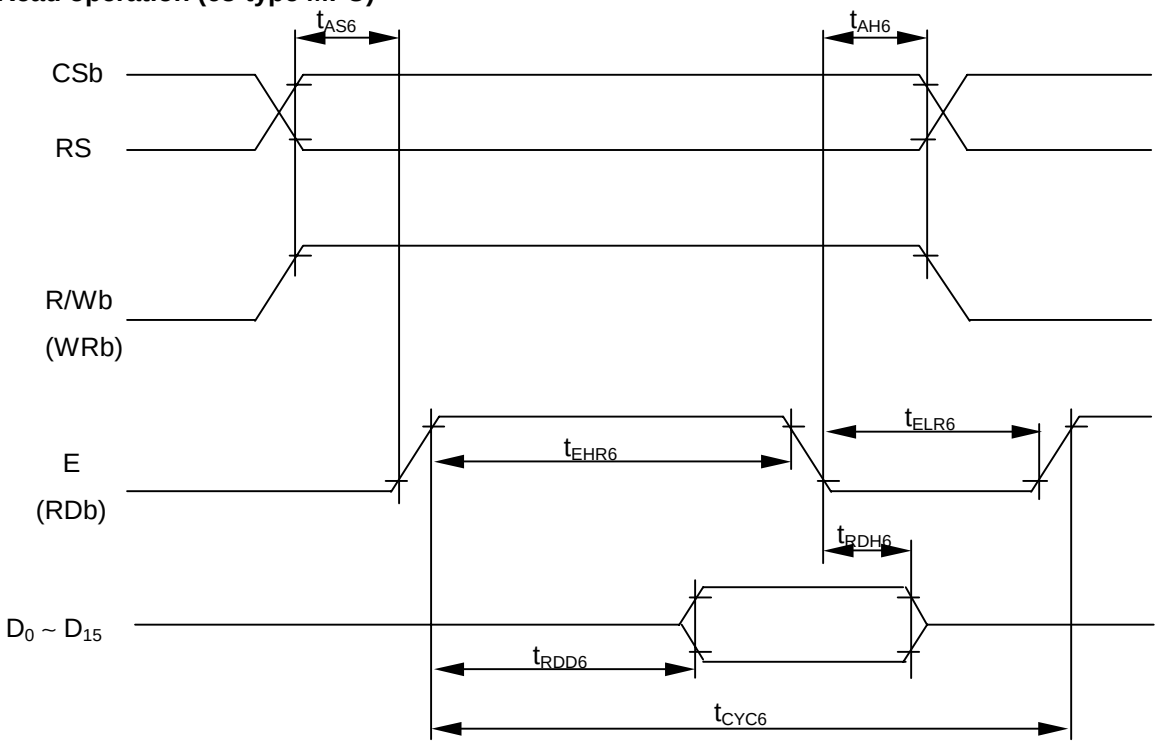
PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	$\overline{CS}$ RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		160 70 70		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		50 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		180 80 80		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	 0	70	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

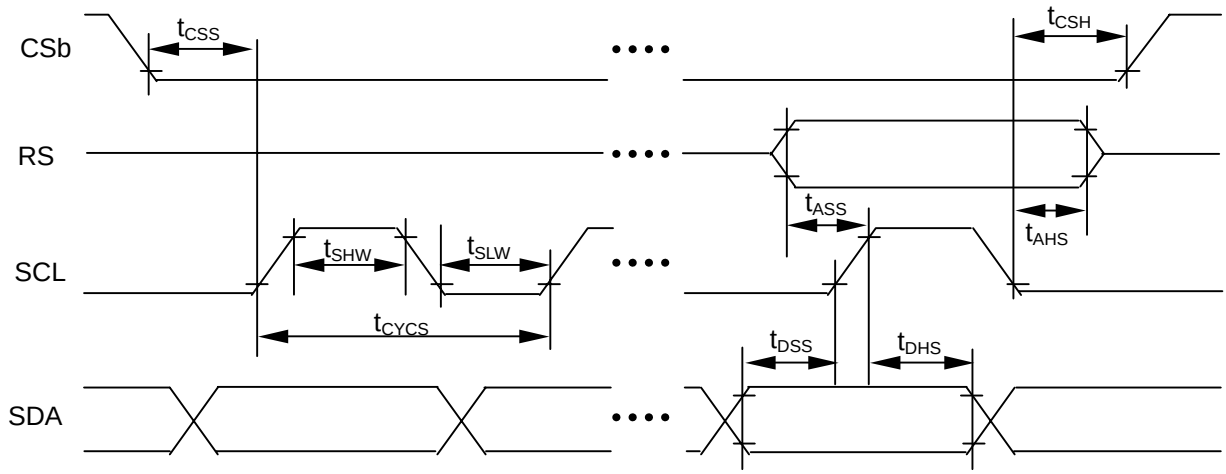
PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR8}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	 0	70	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PRMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	 0	110	ns ns	D0 ~ D15

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Serial interface**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

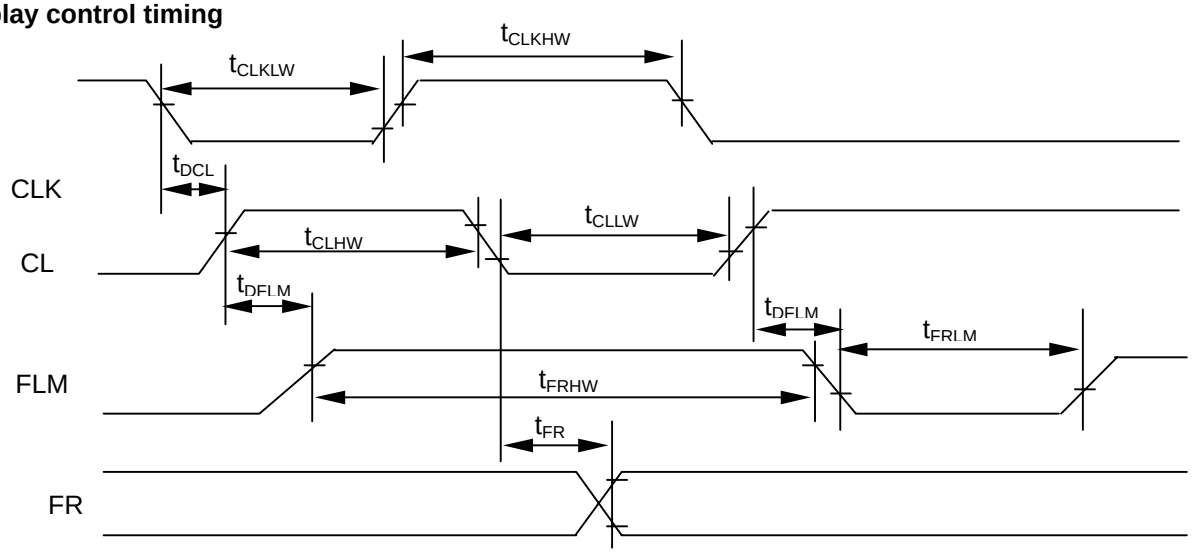
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

● **Display control timing**



<FFL=1>

Input timing (Slave mode) (V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
CLK "H" level pulse width CLK "L" level pulse width	t_{CLKHW} t_{CLKLW}		530 530		ns ns	CLK
CL "H" level pulse width CL "L" level pulse width	t_{CLHW} t_{CLLW}		32.9 32.9		µs µs	CL
CL delay time	t_{DCL}		0	250	ns	CL
FLM delay time	t_{DFLM}		-1.0	1.0	µs	FLM
FR delay time	t_{FR}		-1.0	1.0	µs	FR

Output timing (Master mode) (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
CLK "H" level pulse width CLK "L" level pulse width	t_{CLKHW} t_{CLKLW}		540 540		ns ns	CLK
CL "H" level pulse width CL "L" level pulse width	t_{CLHW} t_{CLLW}		33.5 33.5		µs µs	CL
FLM "H" level pulse width FLM "L" level pulse width	t_{FRHW} t_{FRLW}		67 5427		µs µs	FLM
CL delay time	t_{DCL}	CL=15pF	0	200	ns	CL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}	CL=15pF	0	500	ns	FR

Output timing (Master mode) (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
CLK "H" level pulse width CLK "L" level pulse width	t_{CLKHW} t_{CLKLW}		540 540		ns ns	CLK
CL "H" level pulse width CL "L" level pulse width	t_{CLHW} t_{CLLW}		33.5 33.5		µs µs	CL
FLM "H" level pulse width FLM "L" level pulse width	t_{FRHW} t_{FRLW}		67 5427		µs µs	FLM
CL delay time	t_{DCL}	CL=15pF	0	200	ns	CL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}	CL=15pF	0	1000	ns	FR

Note) Each timing is specified based on 20% and 80% of V_{DD}.
1/82 Duty

<FFL=0>

Input timing (Slave mode) (V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
CLK "H" level pulse width CLK "L" level pulse width	t_{CLKHW} t_{CLKLW}		1100 1100		ns ns	CLK
CL "H" level pulse width CL "L" level pulse width	t_{CLHW} t_{CLLW}		80 80		µs µs	CL
CL delay time	t_{DCL}		0	250	ns	CL
FLM delay time	t_{DFLM}		-1.0	1.0	µs	FLM
FR delay time	t_{FR}		-1.0	1.0	µs	FR

Output timing (Master mode) (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

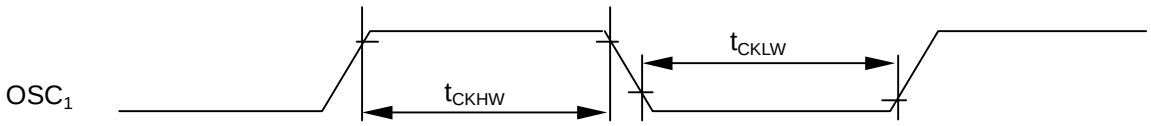
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
CLK "H" level pulse width CLK "L" level pulse width	t_{CLKHW} t_{CLKLW}		1120 1120		ns ns	CLK
CL "H" level pulse width CL "L" level pulse width	t_{CLHW} t_{CLLW}		81 81		µs µs	CL
FLM "H" level pulse width FLM "L" level pulse width	t_{FRHW} t_{FRLW}		138 11250		µs µs	FLM
CL delay time	t_{DCL}	CL=15pF	0	200	ns	CL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}	CL=15pF	0	500	ns	FR

Output timing (Master mode) (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
CLK "H" level pulse width CLK "L" level pulse width	t_{CLKHW} t_{CLKLW}		1120 1120		ns ns	CLK
CL "H" level pulse width CL "L" level pulse width	t_{CLHW} t_{CLLW}		81 81		µs µs	CL
FLM "H" level pulse width FLM "L" level pulse width	t_{FRHW} t_{FRLW}		138 11250		µs µs	FLM
CL delay time	t_{DCL}	CL=15pF	0	200	ns	CL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}	CL=15pF	0	1000	ns	FR

Note) Each timing is specified based on 20% and 80% of V_{DD}.
1/82 Duty

- **Input clock timing**

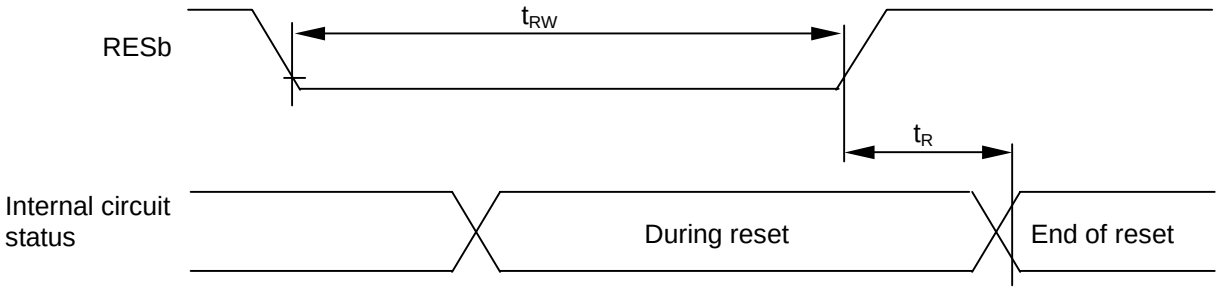


(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC_1 "H" level pulse width (1)	t_{CKHW1}		0.525	1.64	µs	OSC_1
OSC_1 "L" level pulse width (1)	t_{CKLW1}		0.525	1.64	µs	∗1
OSC_1 "H" level pulse width (2)	t_{CKHW2}		2.45	7.35	µs	OSC_1
OSC_1 "L" level pulse width (2)	t_{CKLW2}		2.45	7.35	µs	∗2
OSC_1 "H" level pulse width (3)	t_{CKHW3}		17.2	51.0	µs	OSC_1
OSC_1 "L" level pulse width (3)	t_{CKLW3}		17.2	51.0	µs	∗3

Note) Each timing is specified based on 20% and 80% of V_{DD}.
Note *1) Applied to the variable gradation mode / MON="0", PWM="0"
Note *2) Applied to the fixed gradation mode / MON="0", PWM="1"
Note *3) Applied to the B&W mode / MON="1"

- **Reset input timing**



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

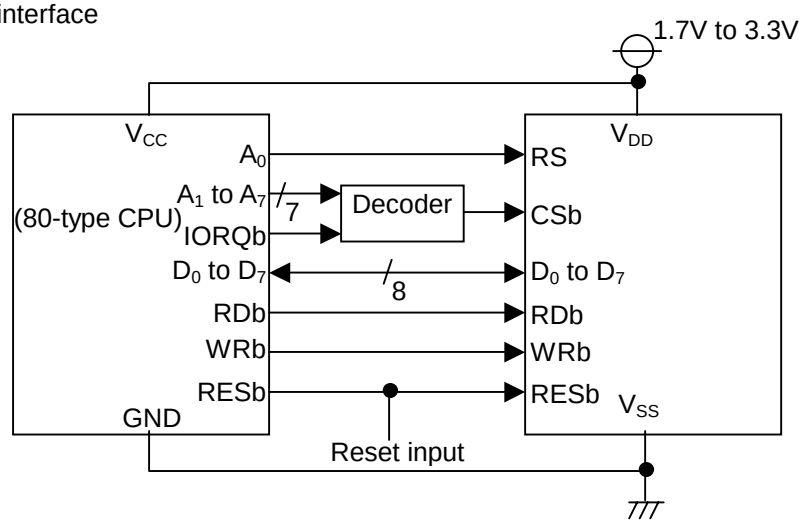
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

Note) Each timing is specified based on 20% and 80% of V_{DD}.

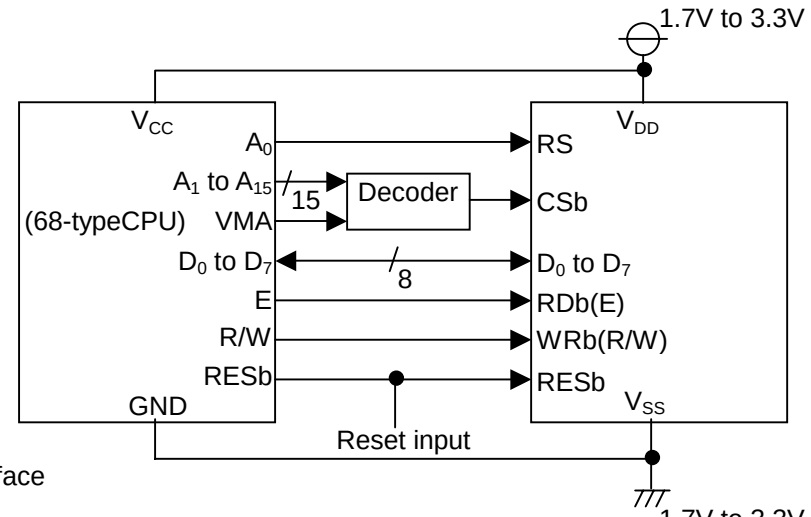
■ APPLICATION CIRCUIT EXAMPLES

● MPU Connections

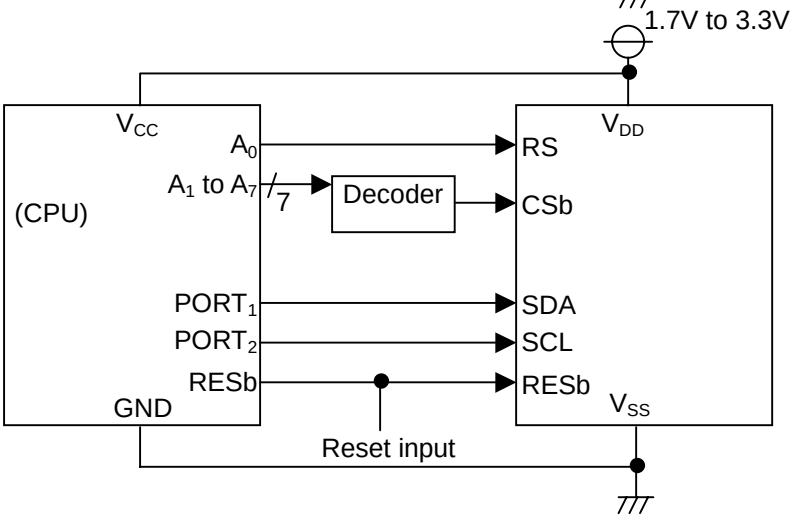
80-type MPU interface



68-type MPU interface



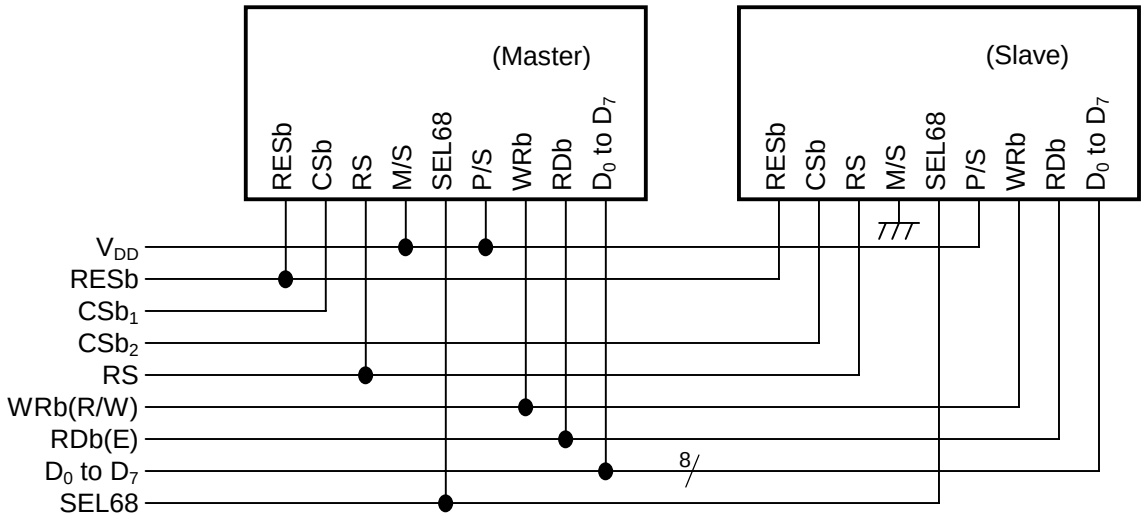
Serial interface



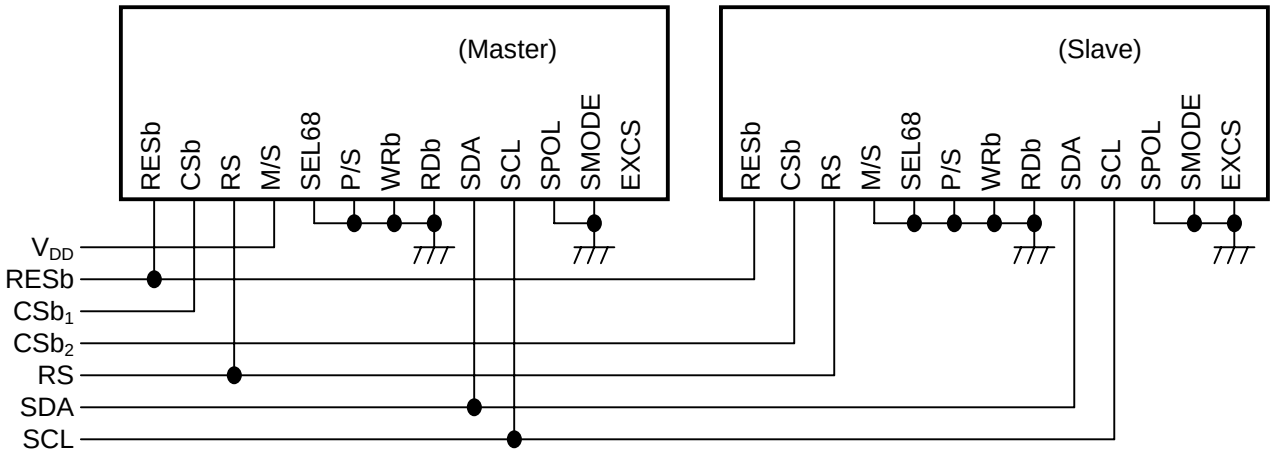
- **Master LSI and Slave LSI Connections**

a) Input interface

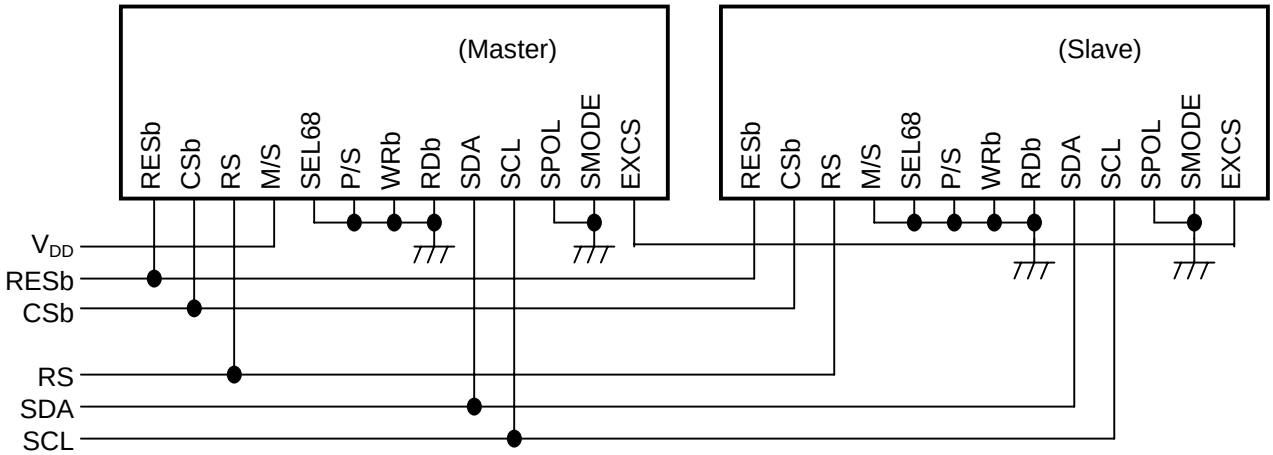
(Parallel interface)



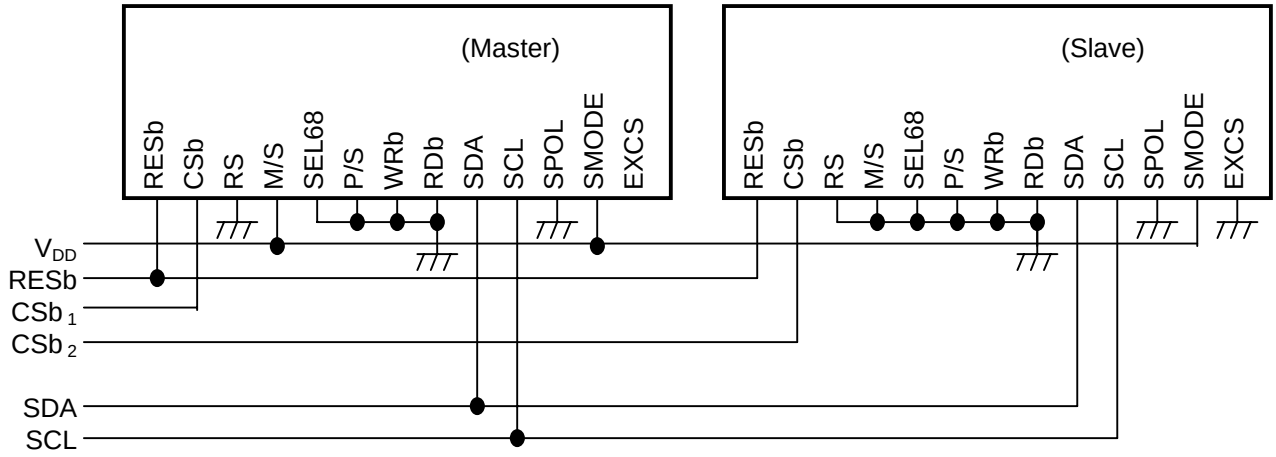
(4-line serial interface)



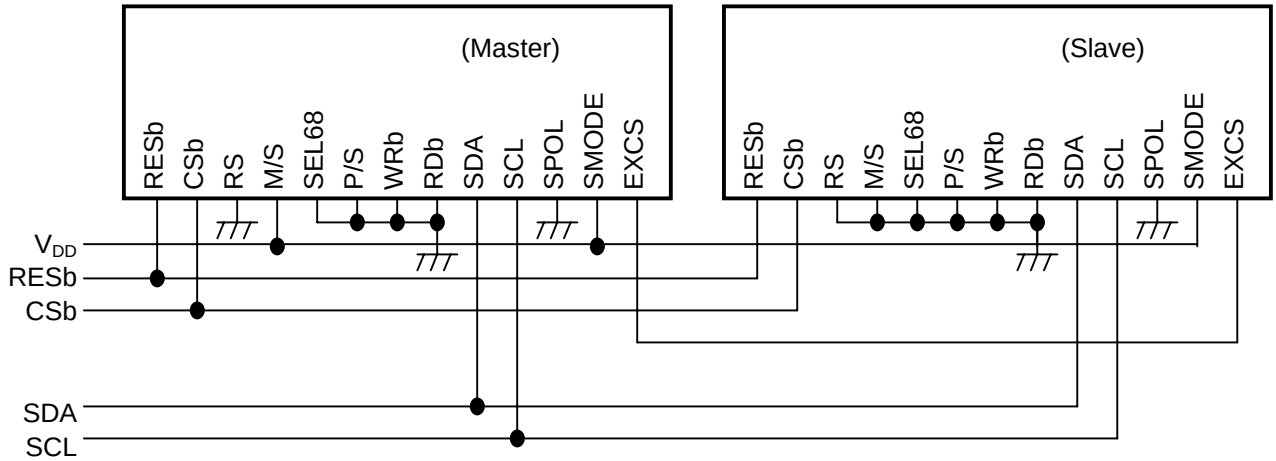
(4-line serial interface, EXCS unification)



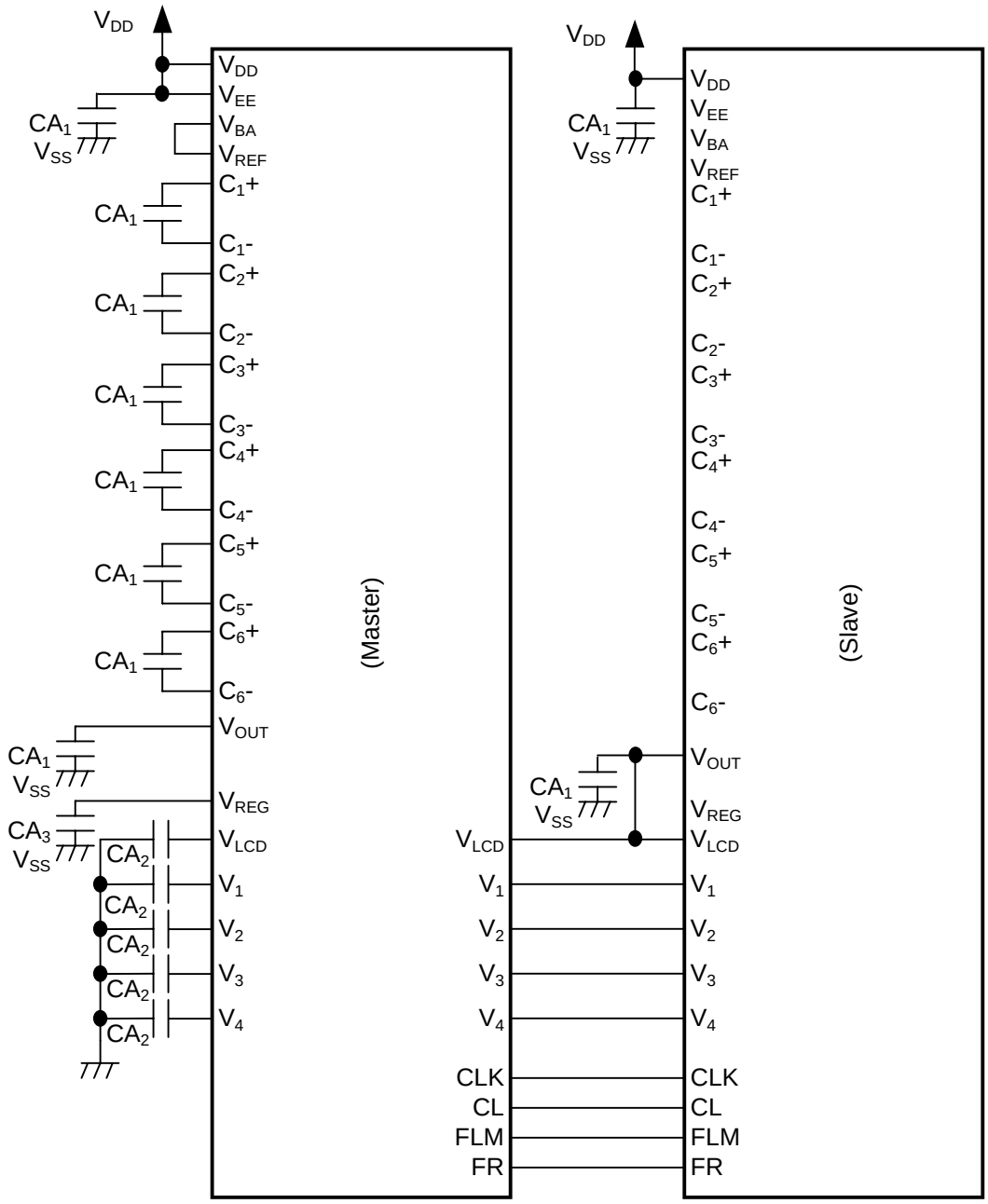
(3-line serial interface)



(3-line serial interface, EXCS unification)



b) LCD driving generation circuit



The following paragraphs describes the caution of Master/Slave operation.

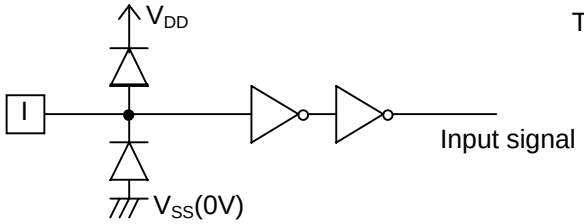
1) Display timing is controlled by Master chip. The CL, FLM, FR, CLK signals are stopped when Master chip is display OFF. When “Display OFF” executions, Slave chip must execute “Display OFF” before Master.
2) When “HALT” command is executed in Master chip, the voltage booster circuit and voltage regulator circuit is turned off. LCD driver outputs V_{SS} level voltage then display goes to turn off. And V_{LCD} for Slave chip goes to stop supply. When “HALT” command is executed in Master chip, Display off must be executed before. Because V_{LCD} for Slave chip is stopped.
3) The EVR control is valid in only Master chip (on this circuit diagram).
4) V_{OUT} terminal should connect to V_{LCD} to prevent condition of floating.
5) OSC_1 terminal and OSC_2 in Slave chip should be open.

- Typical characteristic

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gste	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

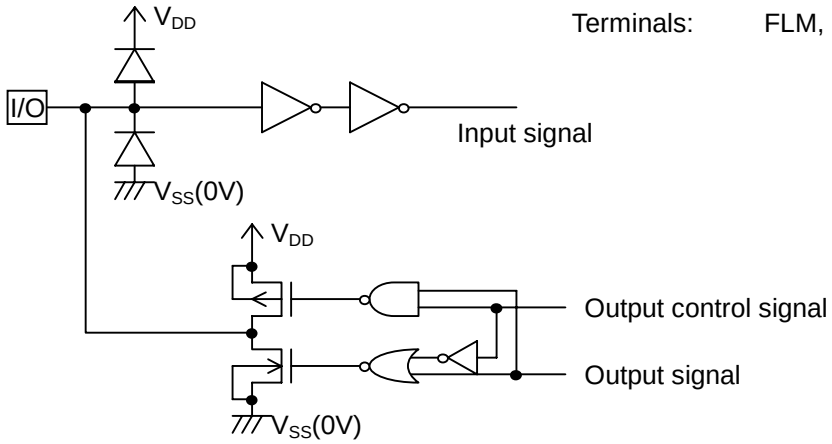
- Input output terminal type

(a) Input circuit1



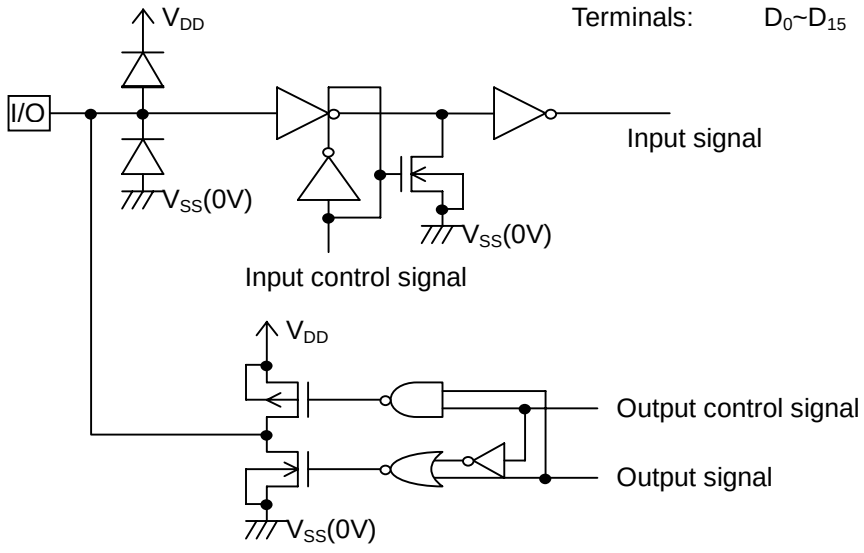
Terminals: CSb, RS, RDb, WRb, SEL68, M/S P/S, RESb

(b-1) Input/Output circuit 1



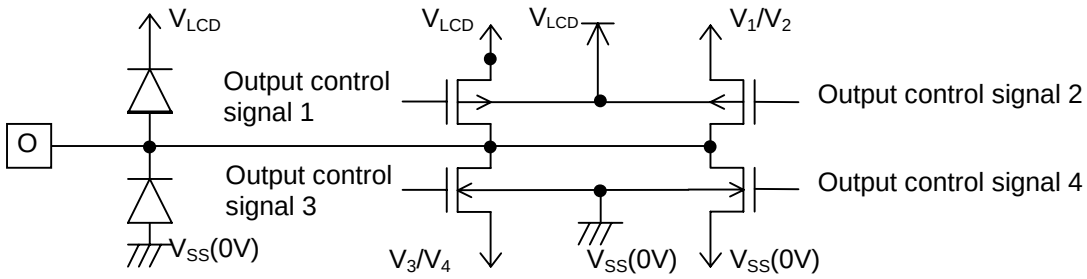
Terminals: FLM, CL, FR, CLK

(b-2) Input/Output circuit 2



Terminals: D_0~D_{15}

(c) Display output circuit



Terminals: $SEGA_0$ to $SEGA_{127}$
$SEGB_0$ to $SEGB_{127}$
$SEGC_0$ to $SEGC_{127}$
COM_0 to COM_{79}
$COMI_0$, to $COMI_1$
$SEGSA_0$, to $SEGSA_3$
$SEGSB_0$, to $SEGSB_3$
$SEGSC_0$, to $SEGSC_3$