DALSA INC.
CCD Image Sensors

IL-C2-0512 TURBOSENSOR™

IL-C2-0512 Linear Image Sensor Array

T-41-55

FEATURES

- **TURBOSENSOR™ Ultra High Speed Technology**
- **512 Elements**
- **White References**
- **60 MHz Effective Data Rate**
- **Linear Response Photoelements**
- **14μm (H) x 42μm (V) Pixel Size**
- **Dual Output Architecture for Improved Throughput**

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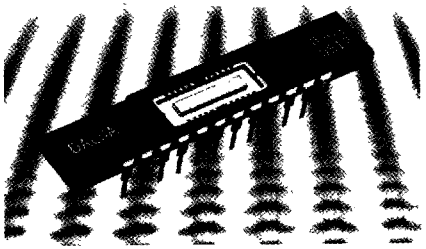


in an 8 pin package for applications such as bar code scanning. Contact DALSA for more information.

DESCRIPTION

DALSA's IL-C2-0512 linear image sensor uses TURBOSENSOR™ technology to provide very high output data rates of 30 MHz per output for an effective output rate of 60 MHz. The IL-C2-0512 is ideally suited for high speed, high resolution applications, and employs buried channel CCD shift registers to maximize output speed and reduce noise.

The dynamic range of the photoelements exceeds 5,000:1 and provides an output which is linear for all output levels.

The IL-C2-0512 does not have an exposure control feature. A similar part (IL-C9-0512) is available from DALSA which incorporates exposure control. Contact DALSA for further information.

The IL-C2 sensor is also available with 128 elements

APPLICATIONS

The IL-C2-0512 is ideally suited for applications requiring high speed and high resolution. The IL-C2-0512 provides over 100 points-per-inch resolution across five inches.

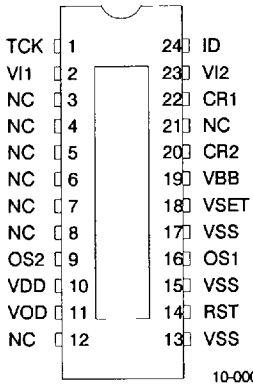
DALSA also offers the CL-C2-0512 line scan camera which uses the IL-C2-0512 for:

- **High Performance Document Scanning**
- **Inspection**
- **Bar Code Scanning**
- **Gauging and Measurement**

For mechanical information regarding package size and tolerance, refer to package #50-01-24005 in **Optical and Mechanical Considerations of Sensors** on pp 101-104 of this databook.

IL-C2-0512 PIN FUNCTIONAL DESCRIPTION

PIN	SYMBOL	NAME
1	TCK	Transfer Clock
2	VI1	White Reference Input 1
3-8	NC	No Connection
9	OS2	Output Signal 2, Even Pixels
10	VDD	Amplifier Supply Voltage
11	VOD	Output Drain Bias Voltage
12	NC	No connection
13	VSS	Ground Reference
14	RST	Output Reset Clock
15	VSS	Ground Reference
16	OS1	Output Signal 1, Odd Pixels
17	VSS	Ground Reference
18	VSET	Output Node Set Voltage
19	VBB	Substrate Bias Voltage
20	CR2	Readout Clock, Phase 2
21	NC	No Connection
22	CR1	Readout Clock, Phase 1
23	VI2	White Reference Input 2
24	ID	Electrical Reference Diode Input



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NOTE: Documentation and Pinout apply to REV B Sensors only.

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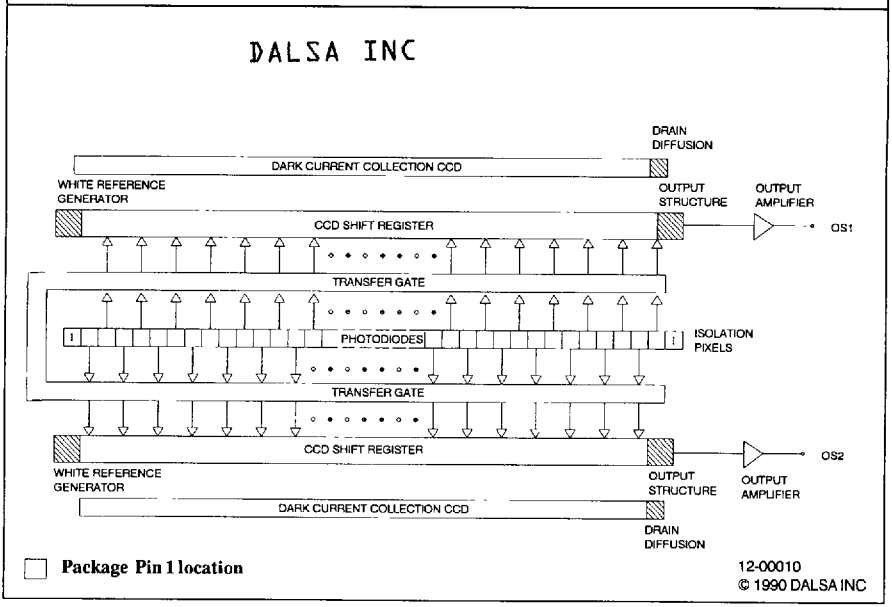
IL-C2 IMAGE SENSOR BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PHOTOELEMENTS

The linear array consists of a line of 512 photoelements, each with a photosensitive area of 588 square micrometers and center to center spacing of 14 micrometers.

The TURBOSENSOR™ photoelement offers ultra high speed operation and responds linearly with respect to input light intensity. The photodiode sensing region offers high sensitivity with a 3:1 height to width aspect ratio.

TRANSFER GATE

This gate controls the flow of light generated signal charge from the photoelements into the CCD shift registers. Electrons from the photoelement are transferred when a high potential (equal to the high clock voltage) is applied to the transfer gate. A single input to the device (TCK) controls the transfer gate for both the even and the odd pixels

CCD SHIFT REGISTERS

There are two buried channel CCD signal transport shift registers, one on each side of the line of photoelements. Buried channel shift registers are used to maximize speed, improve charge transfer efficiency and reduce noise. Alternate signal charge packets are transferred to the inner pair of transport CCD shift registers and serially shifted towards the output signal amplifiers The use of bilinear CCD shift registers increases the effective data rate to 60 MHz by providing access to even and odd photoelements simultaneously.

In addition to the signal transport CCDs, two outer CCD shift registers provide protection to the inner shift registers from peripherally generated electron noise.

WHITE REFERENCES

A white reference signal is created in the first element of the CCD shift registers and is controlled by the input signals VI1, VI2, and ID. The reference pulses occur at the end of the output data. Adjustment of the voltages VI1 and VI2 varies the amplitude of these pulses to provide approximately 150% of the maximum video output signal. For simple operation, disable white reference by grounding VI1, VI2 and apply a high potential to ID.

OUTPUT STRUCTURE

The signal charge packets from the transport shift registers are transferred serially, over the SET gate, to a floating sensing diffusion. As the signal charge is received, the corresponding potential on the diffusion is applied to the input of a two stage low noise amplifier structure, producing an output signal voltage (OS1 or OS2). The floating sensing diffusion is cleared of signal charge by the reset gate, driven by the reset clock (RST) in preparation for the subsequent signal charge packet.

RECOMMENDED DC OPERATION

SIGNAL NAMES

The signal names assigned to the package pins describe both the function of the pin as well as the sense of input signals. DC (unclocked) bias and supply voltages are designated with signal names beginning with "V". Clocked signals begin with any other letter and are representative of the function of the pin.

SUPPLY VOLTAGES

VDD provides operating current to the on chip output amplifier and hence should be well regulated. The substrate, or bulk bias voltage, VBB, is negative with respect to ground in some applications. This low current bias should be well regulated. Since protection diodes are provided between many clock lines and the substrate, no clocks can be permitted to go below VBB. A negative VBB can reduce charge injection.

OUTPUT BIAS

A high impedance DC gate bias, VSET, controls transfer of signal charge onto the output sensing diffusion. This voltage should be adjusted externally to optimize output structure operation. If VSET is not optimized, single bright pixels (or a white reference pixel) will appear to "bleed" into adjacent pixels and could be mistaken for very poor CTE or crosstalk.

The shift register output drain voltage, VOD, is a bias provided to the output structure to discharge signal electrons after sensing. This voltage can be fixed at VDD but should be filtered to reduce noise.

WHITE REFERENCE BIAS

The electrical reference generator uses two high impedance DC biases, VI1 and VI2, to produce a reference output pixel. Adjustment of the relative voltages of VI1 and VI2, via resistive dividers will allow the user to set the electrical reference output equal to the maximum output voltage. The VI2 potential should be higher than the VI1 potential in order to create a white reference. To disable the white reference the VI2 potential should be lower than the VI1 potential.

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IL-C2 DC OPERATING CONDITIONS

Recommended Operating Conditions at Tp = 25°C. (See notes)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Amplifier supply voltage	11.0	15.0	16.0	V
VBB	Substrate voltage	-3.0	-0.5	0.0	V
VOD	Shift register drain voltage	11.0	15.0	16.0	V
VI1	White Reference Input 1	0.5	3.0	12.0	V
VI2	White Reference Input 2	2.0	6.0	12.0	V
VSET	Set Voltage	2.0	3.5	9.0	V
VLS	Light Shield Voltage	0.0	0.0	0.0	V

NOTES:

(1) Voltages with respect to ground (VSS).
(2) Tp is defined as the package temperature.
(3) VSET voltage will increase as VDD is increased from the typical value.

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RECOMMENDED CLOCK OPERATION

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PHOTOELEMENTS

Signal charge electrons are photogenerated during the exposure period, which is set by the time between the high to low transitions of the transfer pulse (TCK).

When TCK is pulsed high the pixel data is transferred into the first phase (CR1) of the CCD readout shift register.

TRANSPORT CLOCKS

Two phase readout clocks (CR1,CR2) are required for this array. The readout clocks can be operated at 50% duty cycle continuously with CR1 and CR2 complementary non-overlapping signals. The clock high voltages can be set by the user for the specific application. In general, higher clock voltages will provide better CTE and higher operating speeds; however, power dissipation on the device will increase due to an increase in C dV/dt current to the clocks.

TRANSFER CLOCK

Transfer clock TCK controls the transfer of signal from the pixel into the CCD readout shift register. The high voltage on this clock line should be equal to the high voltage on the readout clocks. The TCK low voltage can be brought as far negative as VBB.

WHITE REFERENCE

The one clock required for reference pulse generation is ID, and is active low. This pulse occurs at the same time as the TCK pulse. If electrical reference output is not required, VID should be maintained at a high DC voltage (VDD).

OUTPUT CONTROL CLOCKS

One output structure clock (RST) is required to clear the output node after sensing. This clock should go to a high voltage equal to the readout clock (CR) high voltages, and to a low of VSS. During RST high, the outputs (OS1 and OS2) will go to a reset level as shown in the clock timing diagrams.

OUTPUT SIGNALS

The output signals OS1 and OS2 provide video data for the even and odd pixels, respectively. The frequency of OS1 and OS2 is equal to the frequency of the RST clock; the effective video output frequency is equal to twice the frequency of the RST clock. The output signal is an AC signal on a DC offset. AC coupling is recommended after the signal has been buffered from the image sensor.

IL-C2 CLOCK CHARACTERISTICS

Recommended Operating Conditions at Tp = 25°C.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VH(CR)	Transport clock HIGH	8.0	12.0	15.0	V
VL(CR)	Transport clock LOW	0.0	0.0	0.5	V
VH(TCK)	Transfer clock HIGH	7.0	12.0	15.0	V
VL(TCK)	Transfer clock LOW	0.0	0.0	0.5	V
VH(ID)	Input Diode clock HIGH	8.0	12.0	15.0	V
VL(ID)	Input Diode clock LOW	0.0	0.0	0.5	V
VH(RST)	Reset clock HIGH	7.0	12.0	15.0	V
VL(RST)	Reset clock LOW	0.0	0.0	0.5	V
f(RST)	Reset freq.(per output rate)		15	30	MHz
f(DATA)	Data freq. (effective data rate)		30	60	MHz

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IL-C2-0512 TURBOSENSOR™

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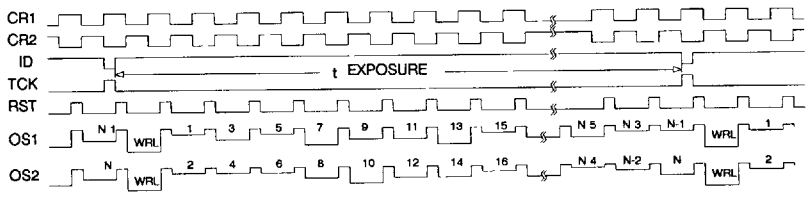
IL-C2 CLOCKING

Overall Clocking



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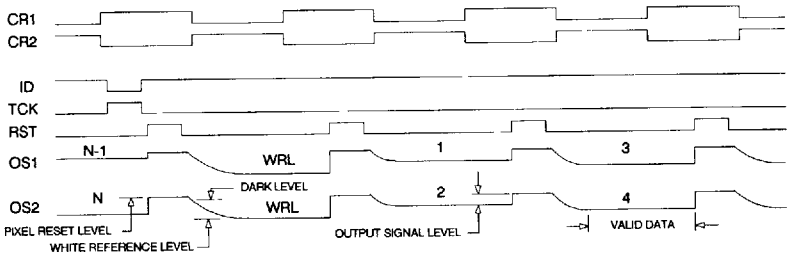
Detailed Clocking



NOTE The clocking is shown for a minimum of 257 CR1 clock pulses between TCK pulses

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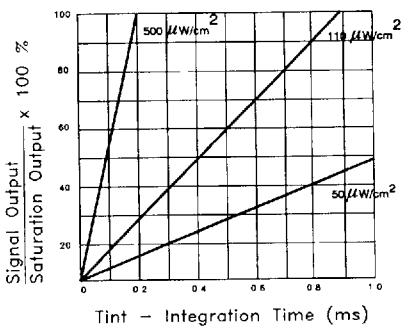
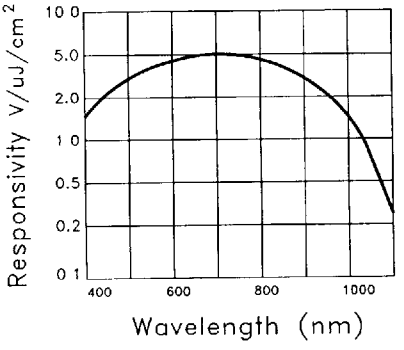
IL-C2 PERFORMANCE MEASUREMENTS



Output vs. Integration Time



Spectral Response

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IL-C2-0512 TURBOSENSOR™

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IL-C2 PERFORMANCE CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C. (See notes).				
Dynamic range[1]		5,000:1		
Noise Equivalent Exposure (NEE)		20		pJ/cm²
Saturation Equivalent Exposure (SEE)[2]		100		nJ/cm²
Responsivity[2]		5.0		V/μJ/cm²
Saturation Output Amplitude (V_{SAT})[3]		800		mV
V_{NOISE}[4]				
Peak-Peak		0.8		mV
RMS		0.16		mV
FPN (exposure control disabled)		1.0		mV
FPN (exposure control enabled)		10.0		mV
PRNU (exposure control disabled)[5]		5		% V_{SAT}
PRNU (exposure control enabled)[5]		15		% V_{SAT}
CTE[6]	0.9999	0.99999	0.999999	
White Reference Amplitude[3]		500		mV
DC Output Offset	7	9	12	
DC Balance		100		mV
Output Gain Mismatch		10		% V_{SAT}
Storage Temperature (T_P)[7]	−70		+125	°C
Operating Temperature (T_P)[7]	−60		+90	°C

Notes:

1. Ratio of VSAT to RMS Noise with reset noise eliminated through correlated double sampling (CDS).
2. Responsivity at peak Quantum Efficiency (near 700 nm).
3. Output amplitude with respect to dark reference level.
4. Amplifier noise measured with reset noise eliminated through correlated double sampling (CDS).
5. PRNU is measured at approximately 50% VSAT and is the difference between the active pixels with the lowest and highest outputs, expressed as a percentage of VSAT.
6. CTE is the measurement for a one stage transfer, measured at f_{RST} = 3.75 MHz
7. TP is package temperature

Test Conditions:

1. All tests are done at f_{RST} = 3.75 MHz, or f_{DATA} = 7.5 MHz.
2. Light Source QTH lamp with WBHM, unless otherwise noted.
3. VDD, VOD = 15 V; VBB = 0 V; Clock high voltage 12 V, low voltage 0 V, (includes CRx, Clx, CSx, TCK, RST as applicable); VSET as required for maximum VSAT and CTE
4. All measurements exclude first and last pixel of each output.

IL-C2 ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C.				
Output impedance		200		Ω
Amplifier supply current		20		mA
DC Bias Currents (VOD, VSET, VBB)			1	mA
Amplifier power dissipation	225	300	550	mW
Resistance to VBB				
Transport clock (CR1, CR2)		5		MΩ
Transfer clock		5		MΩ
Reset, Set clock		5		MΩ
Capacitance to VBB				
Transport clock (CR1, CR2)		160		pF
Transfer clock (TCK)		15		pF
Reset (RST), Set (VSET) gate		8		pF

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Optical and Mechanical Considerations of Sensors

Optical and Mechanical Considerations of DALSA CCD Image Sensors

DALSA INC T-90-20

This applications note provides packaging information for the sensors listed in this databook. Please refer to the tables on the following pages for the critical dimensions of each image sensor series. For more information on a particular image sensor, please refer to the specific datasheet.

FIGURE 1. DIMENSIONS OF PACKAGE # 50-01-24005

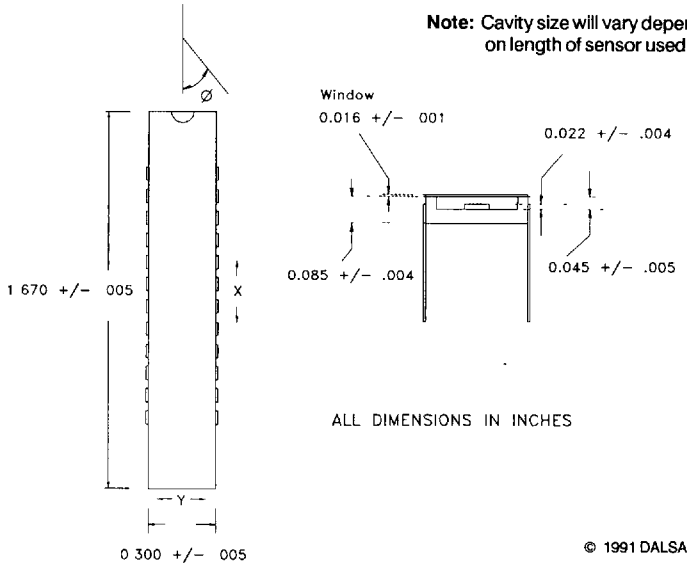

TABLE 1. PACKAGE # 50-01-24005 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-24005	IL-C3-0128	0.55 ± .09	0.15 ± .02	$0^{o} \pm 3.0^{o}$
50-01-24005	IL-C3-0256	0.55 ± .08	0.15 ± .02	$0^{o} \pm 2.5^{o}$
50-01-24005	IL-C3-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C9-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C4-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C4-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C5-2048	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C5-4096	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C6-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-E1-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-E1-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-E1-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-F2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-F2-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-F2-2048	0.55 ± .04	0 15 ± .02	$0^{o} \pm 1.0^{o}$

Note: X = center imaging area to center pin 1 along package Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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Optical and Mechanical Considerations of Sensors

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FIGURE 2. DIMENSIONS OF PACKAGE # 50-01-40003

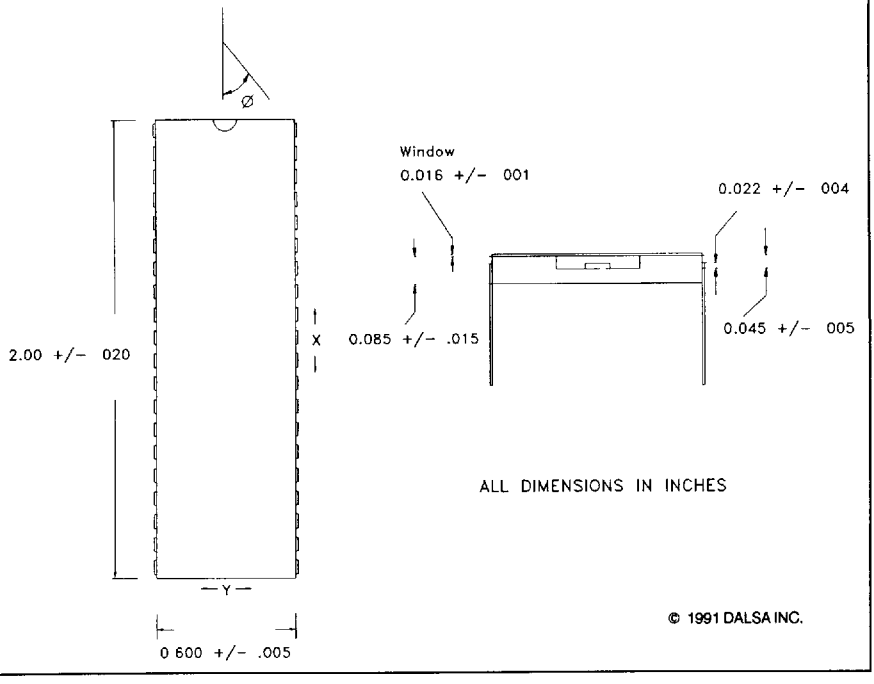

TABLE 2. PACKAGE # 50-01-40003 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40003	IT-C5-2048	0.95 ± 0.1	0.3 ± 0.05	$0^{\circ} \pm 2.5^{\circ}$
50-01-40003	IT-C5-4096	0.95 ± 0.08	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-E1-1536	0.95 ± 0.08	0.3 ± 0 05	$0^{\circ} \pm 2.0^{\circ}$
50-01-40003	IT-E1-2048	0.95 ± 0.06	0.3 ± 0.05	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-F2-2048	0.95 ± 0.06	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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FIGURE 3. DIMENSIONS OF PACKAGE # 50-01-24002

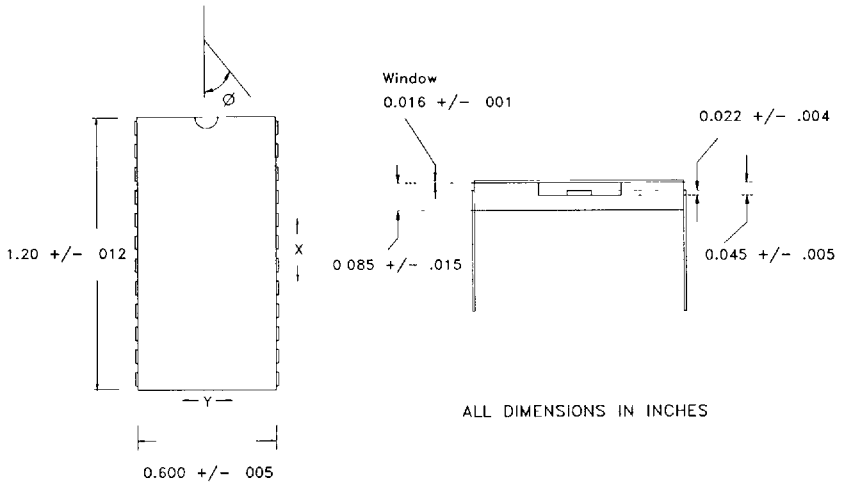

TABLE 3. PACKAGE # 50-01-40002 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40002	IA-D1-0032	0.56 ± 0.12	0.3 ± 0.05	$0^{o} \pm 5.0^{o}$
50-01-40002	IA-D1-0064	0.57 ± 0.09	0.3 ± 0.04	$0^{o} \pm 4.0^{o}$
50-01-40002	IA-D1-0128	0.59 ± 0.12	0.3 ± 0.03	$0^{o} \pm 2.5^{o}$
50-01-40002	IA-D1-0256	0.71 ± 0.10	0.3 ± 0.03	$0^{o} \pm 1.5^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation

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FIGURE 4. DIMENSIONS OF PACKAGE # 50-01-28004

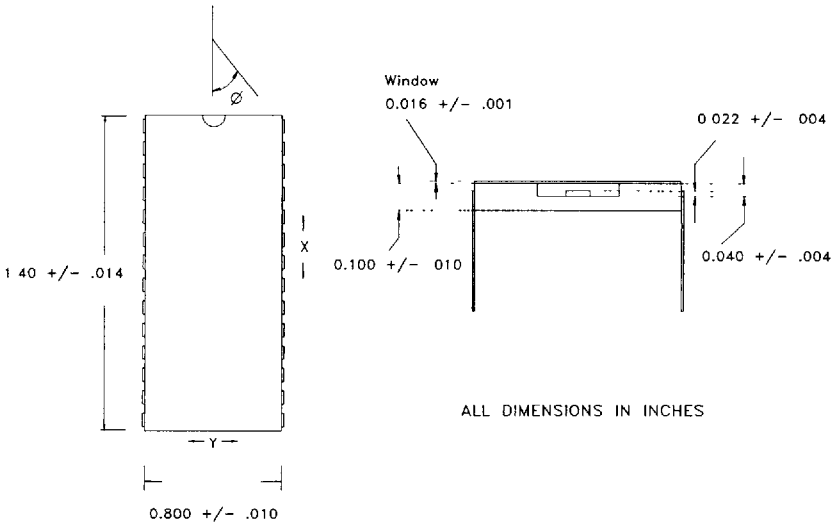

TABLE 4. PACKAGE # 50-01-28004 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-28004	IA-D2-0512	0.65 ± 0.08	0.4 ± 0.04	$0^{o} \pm 3.0^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation