General Information

System Considerations

Most system designs are on a continuous path toward higher integration, with greater proprietary intellectual content per IC, as a means to:

- improve overall system performance
- enhance system functionality
- differentiate one's product from the competition.

As a result, the number of applications for discrete logic is diminishing.

However, the need for low level integration will never completely disappear. Some functions cannot be integrated because:

- Technology limitations: Different functions may require diverse process technologies, which frequently cannot be integrated onto one die.

- Practical PC board considerations: It may be difficult, or impossible, to place many large scale integration ICs in the perfect location. It may therefore be necessary to distribute certain functions using small scale integration solutions.

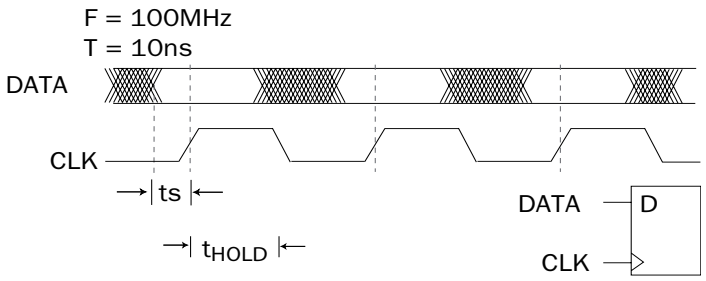
Frequency Considerations

Process geometries continue to shrink rapidly, enabling faster circuit operation. Frequencies that were leading edge and highly impractical years ago are now quite common.

This higher speed operation has yielded tremendous benefits in overall system performance. However, it has also created new problems that existing glue logic and SSI components are ill-suited to resolve. More specifically, as frequencies increase, the amount of timing variation that can be tolerated in multiple paths becomes smaller.

Historically, clock generation was treated carefully, with much attention paid to distributing a clean and stable clock signal throughout a system. Data signals, on the other hand, were considered less important. As long as adequate setup and hold times at the destination were maintained, little more was required.

Example A:



In this example, the ICs responsible for distributing the clock and data signals may suffer several nanoseconds of variation due to:

1) ΔTpd: part to part
2) ΔTpd: channel to channel (within a part)
3) ΔTpd+/-: different propagation delays for a positive vs. negative transition
4) ΔTr/f: rise / fall time mismatches
5) ΔTpd vs. frequency, duty cycle, and pattern
6) ΔTpd vs. environmental changes, particularly temperature and supply voltage
7) Transmission line imperfections and mismatches.

Adding up all these error terms yields the total timing uncertainty. But as long as the relationship

$$(\text{Total Error}) + Ts + Thold \leq T$$

holds true, the system will still function properly.

A worst case system level error of several nanoseconds (~3 ns) is quite reasonable using multiple instances of most standard components. With a setup and hold time of ~2 ns each, a 100 MHz system works with several nanoseconds of margin.

$$\text{Total Error} + Ts + Thold = \sim 3\text{ ns} + \sim 2\text{ ns} + \sim 2\text{ ns}$$
$$\cong 7\text{ ns} \leq 10\text{ ns}$$

General Information *(con'd)*

However, consider a 500 MHz example.

Example B:

F = 500 MHz, T = 2 ns, ts = 500 ps, Thold = 500 ps

This situation leaves only 1 ns for all remaining sources of timing error. Using the same clock and data distribution components, with a total error of ~3 ns, the system no longer functions.

Total Error+ ts+ Thold = ~3 ns+.5 ns + .5 ns ≥ 2 ns!

There is no longer adequate setup and hold time.

Semtech "EPiC Family" Product Line

To address applications where **E**very **Pi**coseconds **C**ounts, Semtech offers the EPiC Product Line, consisting of three product families - the 15XX, 19XX, and 44XX. All three product families are optimized for high speed clock and data distribution applications in terms of:

- Speed
- Accuracy
- Integration
- Functionality

Speed and Accuracy

The EPiC product line is extremely fast and accurate. All three families operate up to 3 GHz while maintaining timing accuracy.

All EPiC products have very accurate, tight, stable, and repeatable timing characteristics. The EPiC product line is designed to minimize any timing errors associated with:

1) part to part variation
2) channel to channel variation
3) rise / fall time mismatches
4) positive vs. negative transition propagation delays
5) changes in duty cycle, pattern, or frequency
6) environmental changes (voltage and temperature).

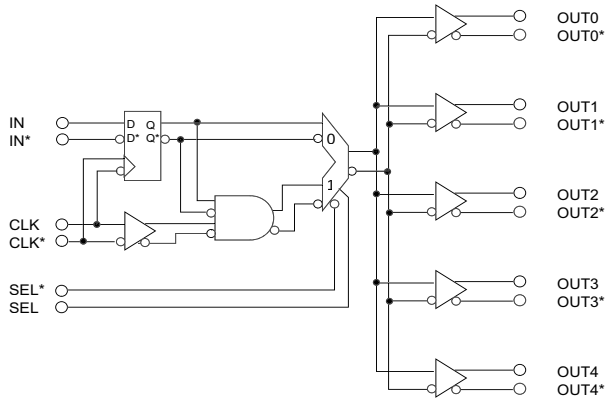
Functionality and Integration

The EPiC product lines support unusually high levels of integration via three techniques:

1) Packaging - the 5 mm x 5 mm TQFP package has a very small footprint with very low pin inductance.
2) Functional Integration - each part can perform several functions traditionally implemented with distinct ICs:
   a) level translation (wide voltage range input capability: ECL, PECL, and double swing output options)
   b) resynchronization (flip-flop and MUX integrated)
   c) fanout (1:5, 1:9 available)
   d) synchronous enable / disable
3) On-chip terminations - the inclusion of current sources and resistors integrates many space consuming passive components typically placed on the PCB. For further ECL/PECL termination techniques, refer to the applcation note AN1003.

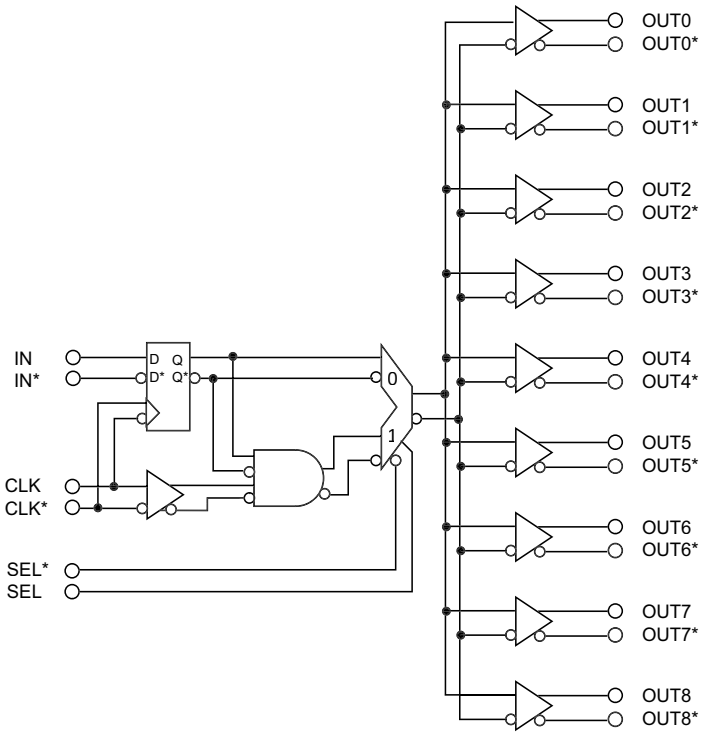
SK15XX, SK19XX Functionality

The 15XX and 19XX product families are designed to buffer a high speed signal, resynchronize it (if required), and then distribute multiple identical versions of this signal to multiple destinations.

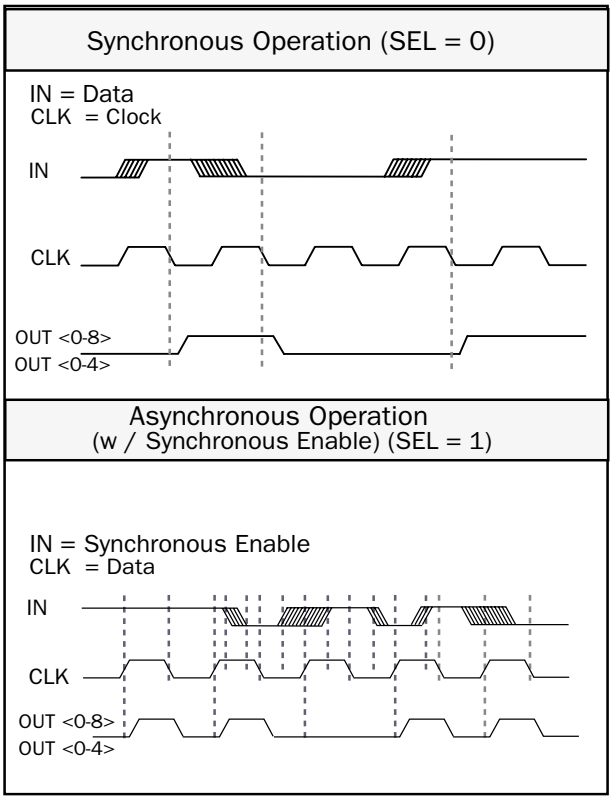


SK15XX Functional Block Diagram

SK15XX, SK19XX Functionality *(con'd)*



SK19XX Functional Block Diagram



Asychronous Operation

When used asychronously (SEL = 1), IN is a synchronous enable and CLK is the input signal. With IN = 1, CLK passes directly and continuously to all output pins. With IN = 0, all outputs will transition to a logical 0 (Q = low, Q* = high) after the next falling edge of CLK. The outputs will remain low until after a falling edge of CLK while IN = 1. IN is designed to allow signals to be enabled and disabled synchronously, with no glitches or runt pulses at the output during enable / disable transition time.

The following truth table summarizes the 15XX and 19XX operation.

SEL	IN	CLK	OUT (<0-8>, <0-4>)	Comments
0	0	↓	0	Synchronous operation
0	1	↓	1	IN Functions like a data input. Outputs transition on falling edge of CLK.
1	1	0	0	Asynchronous Operation.
1	1	1	1	IN is a synchronous enable, CLK passes directly to OUT <0-8> (or <0-4>.
1	0	↓	0	Asychronous operation. OUT <0-8> (or <0-4>) go low synchronously on falling dege of CLK.

SK15XX / 19XX Truth Table

Default Conditions

It is good practice to tie all unused inputs to a known, stable, and a valid voltage level. However, several signals have internal pull up or pull down resistors and therefore, have a known state when left floating. The following chart summarizes the default conditions on the 15XX and 19XX inputs.

Signal	Default State	Mode
IN / IN*	High / Low	Enabled
SEL / SEL*	High / Low	Asynchronous Operation
CLK / CLK*	No Internal Resistors	Do NOT Float

15XX / 19XX Default Condition Chart

SK15XX, SK19XX Functionality *(con'd)*

Input Signal Level Conditions: SK15XX/SK19XX

These devices accept a wide range of input levels. The input levels can be as low as 200 mV and as high as 4.3V peak-to-peak. Refer to the data sheet for specific input levels.(See Figure A for more detail.)

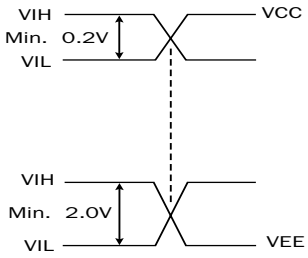


Figure A: Input Swing

Output Signal Level Conditions:

Figure B shows output signal levels for the following devices: SK1500, SK1503, SK1525/SK1900, SK1903, SK1925.

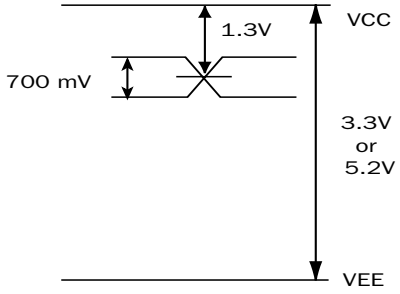


Figure B: Output Swing

Figure C shows output signal levels for SK1501/ SK1901.

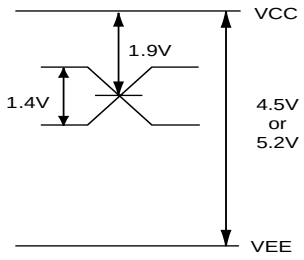


Figure C: Output Swing

Figure D shows output signal levels for the following devices: SK1502, SK1504, SK1527, SK1529/ SK1902, SK1904, SK1927, SK1929

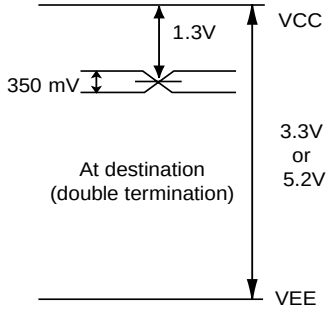


Figure D: Output Swing

SK15XX, SK19XX Functionality *(con'd)*

Figure E shows output signal levels for SK1528, SK1530/ SK1928, SK1930.

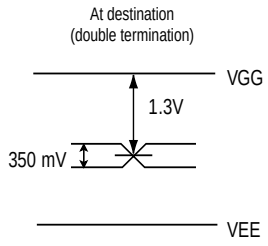


Figure E: Output Swing

Figure F shows output signal levels for the following devices: SK1526/SK1926.

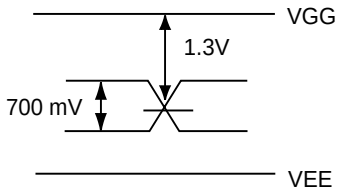
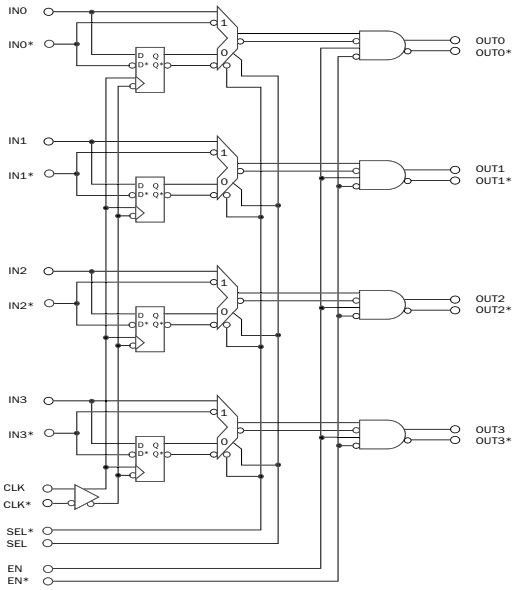


Figure F: Output Swing

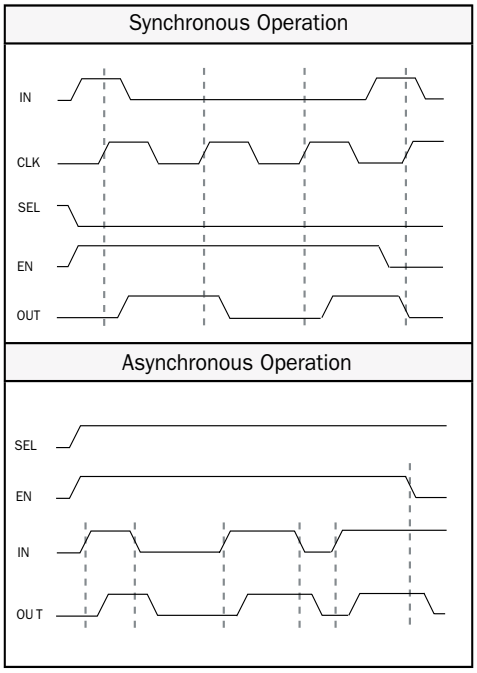
SK44XX Functionality

The 44XX family has similar functionality to the 15XX and 19XX families, only the 44XX is designed for 1:1 buffer applications rather than fanout applications.

EN	SEL	IN <0-3>	CLK	OUT <0-3>	Comments
0	X	X	X	0	Disabled
1	1	0	X	0	Asynchronous Operation IN <0-3> passes directly to OUT <0-3>
1	0	0 1	↓ ↓	0 1	Synchronous Operation



SK44XX Functional Block Diagram



Asychronous Buffer

When used asynchronously (SEL = 1), IN – IN3 pass directly to OUT0 - OUT3. CLK has no function. EN is an asynchronous output enable common to all four outputs.

Sychronous Buffer

When used synchronously (SEL = 0), IN0 – IN3 pass data inputs to the flip-flops, all clocked on the rising edge of the CLK. EN is an asynchronous output enable common to all four outputs.

The following truth table summarizes the 44XX operation.

Differential Inputs / Outputs

Every input and output is fully differential. Single-ended operation is permitted, but overall accuracy may be inferior to a fully differential topology.

All inputs are also wide voltage differential compliant, allowing a variety of input swings to come directly into the

Differential Inputs / Outputs *(con'd)*

part. No translator is required for most (virtually all) different standard digital technologies.

There is no headroom requirement on the inputs on a digital high vs. VCC or a digital low vs. VEE. This is important because it allows the EPiC Families to share a VCC and VEE with a CMOS ASIC and receive rail-to-rail swings without having any functional or performance degradations.

Default Conditions

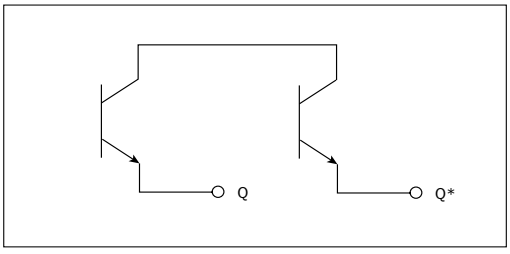
It is good practice to tie all unused inputs to a known, stable, valid voltage level. However, several signals have internal pull up or pull down resistors and, therefore, have a known state when left floating. The following chart summarizes the default conditions on the 44XX inputs.

Signal	Default State	Mode
IN / IN*	No Internal Resistors	Do NOT float
CLK / CLK*	No Internal Resistors	Do NOT float
SEL / SEL*	High / Low	Asynchronous Operation
EN / EN*	High / Low	Outputs Active

Output Configuration Options

There are four basic output structures supported by the EPiC product line. Each configuration is optimized for a specific transmission line topology in order to allow the maximum level of overall system level performance and integration.

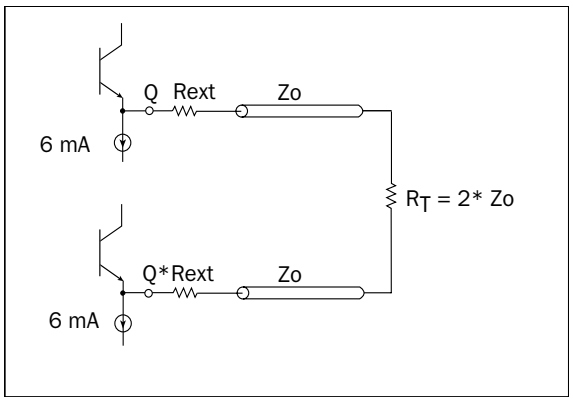
1) Open Emitter



SK44XX Truth Table

The open emitter is the standard ECL output. It is flexible in that it supports point to point routing or daisy chain lines, a wide range of transmission line characteristic impedances, and a variety of termination schemes. Refer to AN1003 for ECL/PECL Signal Termination Techniques.

2) Double Termination



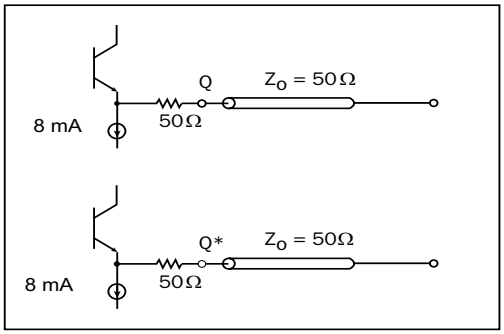
The 50 Ω double termination output structure is optimized for applications with the following characteristics:

a) series (or source) termination and parallel termination
b) point to point routing of a different signal
c) 50Ω transmission lines

In this environment, the double termination output offers the smallest footprint solution for accurate signal distribution.

Note: The double termination output does not function Correctly without a 100 Ω termination resistor at the destination.

3) 50 Ω Source Termination



Output Configuration Options *(con'd)*

The 50Ω source (or series) termination output structure is optimized for applications with the following characteristics:

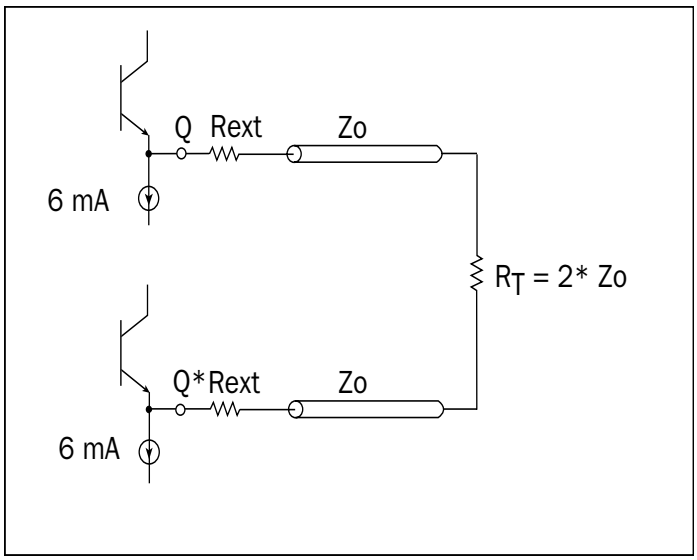
a) point-to-point routing of differential signals (although, it functions for single-ended applications with Q* left disconnected)
b) 50Ω transmission lines

This output configuration does not require any termination resistor at the destination. In fact, it does not require any external components at all.

It is suitable for high-speed data and clock distribution, where double termination is not required.

Note: The source terminated output also works in the double termination environment. However, as a source termination it requires internal 8mA current source, and double termination requires only 6mA, additional power is consumed with no corresponding performance gain.

4) Internal Current Sink (Double Termination)



This output structure is a modified version of the 50Ω double termination output. Accordingly, it is used in applications that require:

1) point-to-point routing of a differential signal
2) series and parallel termination.

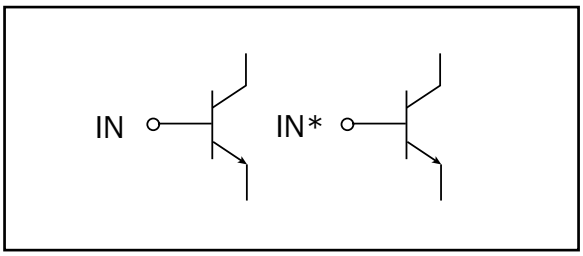
However, as the series termination resistors are not on-chip, this output should be selected in two specific cases:

a) Non-50Ω transmission lines. Use appropriate external resistors to match the line impedance.
b) Ultra high fidelity applications, in situations where the source impedance and line impedance must match extremely close, precision

Input Configuration Options

The 44XX family supports two distinct input options for the IN<0-3> signals.

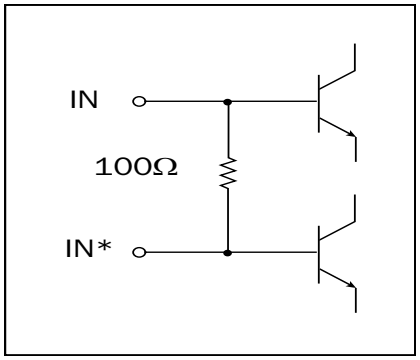
1) High Impedance



This configuration is a standard high impedance input. It is flexible in that it can be used in:

a) multiple destination (display chain), as well as point-to-point applications
b) transmission line environments of a wide range of characteristic impedances (with the appropriate external termination scheme, see AN1003)
c) single-ended applications (with the appropriate VBB brought into CLK*).

2) 100Ω Termination



Input Configuration Options *(con'd)*

The internal 100Ω parallel termination is optimized to provide superior integration and performance in applications that require:

a) differential signals
b) point-to-point routing
c) 50Ω transmission line environment.

The inclusion of the termination resistors integrates four components normally implemented with off-chip discrete components, thus saving considerable PC board real estate.

Input Signal Level Conditions: SK44XX

These devices accept a wide range of input levels. The input levels can be as low as 200 mV and as high as 4.3V peak-to-peak. Refer to the data sheet for specific input levels. (See Figure G for more detail.)

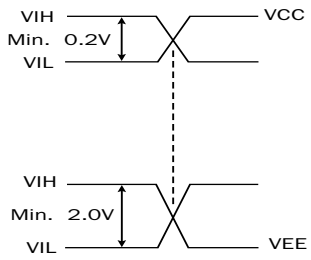


Figure G: Input Swing

Output Signal Level Conditions

Figure H shows output signal levels for the following devices: SK4400, SK4410, SK4425, SK4435.

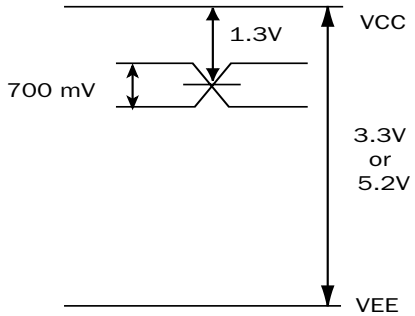


Figure H: Output Swing

Figure I shows output signal levels for the following devices: SK4401, SK4411.

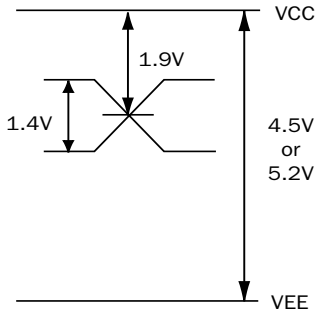


Figure I: Output Swing

Figure J shows output signal levels for the following devices: SK4404, SK4414, SK4426, SK4430, SK4439, SK4440.

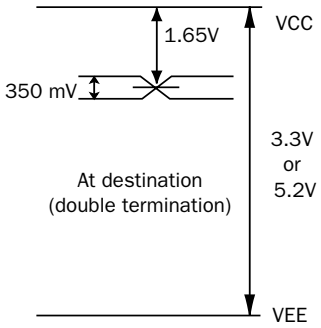


Figure J: Output Swing

Figure K shows output signal levels for SK4436.

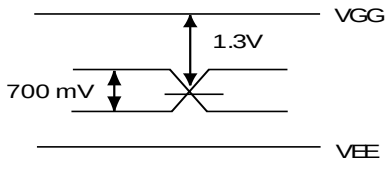


Figure K: Output Swing

The junction temperature may be predicted by the equation:

$$T_J = T_A + \theta_{JA} * P_D$$

However, T_J of any EPiC product will vary over a wide range, depending on the environment. The power consumption is a function of the total supply voltage (VCC - VEE) and the particular output configuration (open emitter, series termination) selected. Thermal resistance θ_{JA}, is heavily dependent upon the particular cooling technique used.

Not all parts may be used reliable for all cooling schemes or power supply conditions. The EPiC Product Line is optimized to provide the most integration and performance for environments using either liquid (or cold plate) cooling, or air flow >300 LFPM. However, the 15XX, 19XX and 44XX families all have several low power options which can be used with little or no forced cooling.

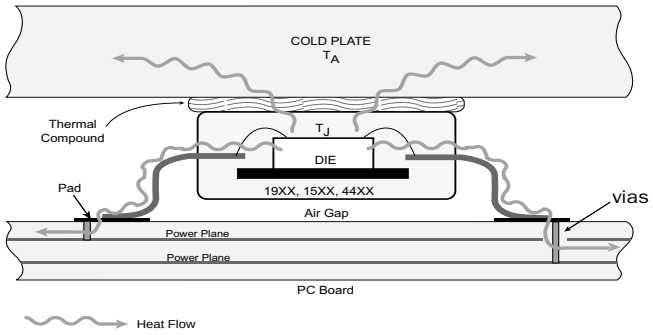
The actual θ_{JA} will be different for each particular environment. However, estimates of typical θ_{JA} performance in several common cooling environments are provided.

Liquid Cooling

In the liquid cooling environment there is no airflow. All cooling is achieved via conduction through the top of the package into a cold plate as well as though the lead frame down into the power planes inside of the printed circuit board.

The following assumptions are made:

1) the part is soldered to a multilayer PC board with internal power planes
2) the part is attached directly to the cold plate on the top side of the package.



In this environment, θ_{JA}, ≅ 30°C / watt.

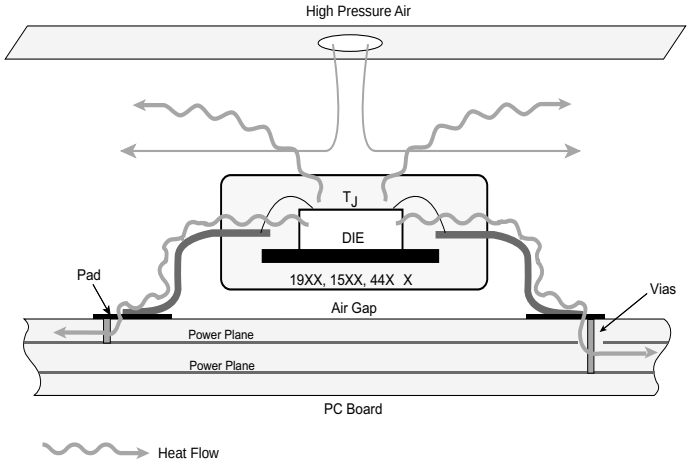
Orthogonal Air Flow

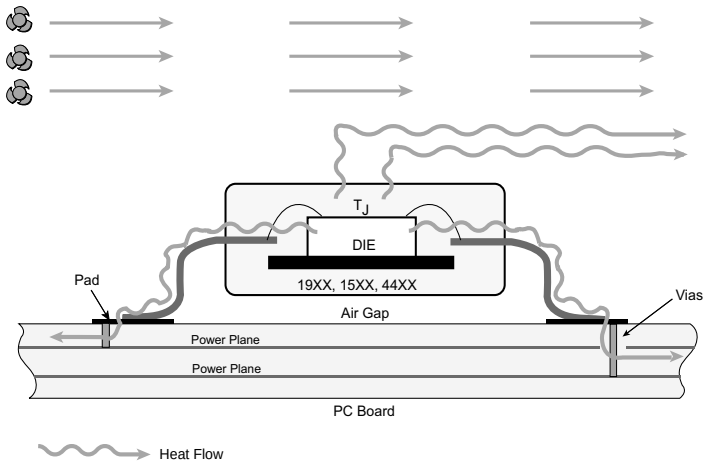
Orthogonal air flow is an environment where cold air flows directly down to the top of the package. In this case, cooling is achieved via convection as the cold air absorbs the heat at the top of the package and carries the heat out on the side, as well as via conduction through the lead frame down into the power planes inside the printed circuit board. This cooling scheme produces the lowest thermal resistance for any air cooled scheme.

The flowing assumptions are made:

1) the part is soldered to a multilayer PC board with internal power planes
2) no heat sink.

Thermal Analysis *(con'd)*





Orthogonal Air Flow

In this environment:

θ_{JA}	Air Flow
	>300 LFPM
	100 LFPM
	50 LFPM

θJ_A	Air Flow
40°C/W	>300 LFPM
	100 LFPM
	50 LFPM

Transverse Air Flow

This is a common technique where cooled air is forced along the top of the PC board. Cooling is achieved via convection, as the cold air passing over the top of the package absorbs the heat and carries it away, as well as via conduction through the lead frame down into the power planes inside the printed circuit board.

The following assumptions are made:

1) the part is soldered to a multilayered PC board with internal power planes
2) laminar air flow.

Translation Summary Table

Source / Destination Technology		Required Fanout			Recommended Suply Levels		
From	To	1:5	1:9	1:1	VCC	VEE	VGG
ECL, TTL, GTL, 3.3V/2.5V/1.8V CMOS, LVTTL, LVPECL	TTL	1501	1901	4401	+3.3V	-2.V	N/A
LVPECL, TTL, GTL, 3.3V/2.5V/1.8V CMOS, LVTTL	ECL	1526, 1528, 1530	1926,1928, 1930	4426, 4430, 4436, 4440	+3.3V	-3.3V	0V
LVPECL, TTL, GTL, 3.3V/2.5V/1.8V CMOS, LVTTL	LVTTL GTL	1526, 1528, 1530	1926,1928, 1930	4426, 4430, 4436, 4440	+3.3V	-2V or -3.3V	+2V
LVTTL, GTL, 1.8v CMOS	ECL	1526, 1528, 1530	1926,1928, 1930	4426, 4430, 4436, 4440	+2V	-3.3V	0V
ECL, TTL, GTL, 3.3V/2.5V/1.8V CMOS	PECL	1525, 1527, 1529	1925, 1927, 1929	4425, 4429, 4435, 4439	+3.3V	-3.3V	N/A

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