

EL2252D Die

Dual 50 MHz Comparator/Pin Receiver

T-45-17

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Voltage between $V+$ and $V-$	36V
Voltage at $V+$	18V
Voltage between $-IN$ and $+IN$ Pins	36V
Output Current	12 mA
Current into $+IN$, $-IN$, HYS, or /TTL	5 mA
Maximum Junction Temperature	175°C

 T_J

Important Note:

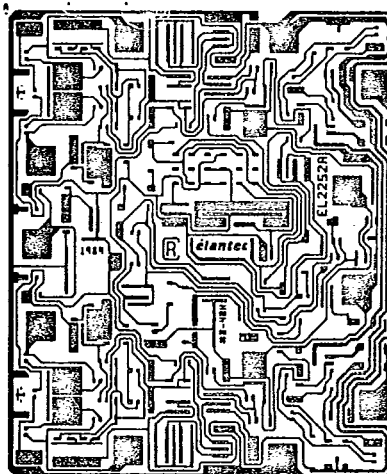
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level

I

Test Procedure

100% production tested in wafer form.
See remarks under Electrical Testing in the General Die section.



DIE SIZE: 65 x 77 MILS

DC Electrical Characteristics $V_S = \pm 15\text{V}$; HYS and i/m TTL grounded; $T_A = 25^\circ\text{C}$

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		1	6	I	mV
I_B	Input Bias Current $V_{CM} = 0\text{V}$, pin 2 or 3		6	12	I	μA
I_{OS}	Input Offset Current $V_{CM} = 0\text{V}$		0.2	1	I	μA
CMRR	Common-Mode Rejection Ratio (Note 1)	70	95		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	70	90		I	dB
V_{CM+} V_{CM-}	Common Mode Input Range	10 -9	13 -12		I	V
A_{VOL}	Large Signal Voltage Gain ($V_{OUT} = 0.8\text{V} + 0.20\text{V}$)	4,000	8,000		I	V/V
V_{OL}	Output Voltage Logic Low $I_{OL} = 0\text{ mA}$	-0.2	0.2	0.4	I	V
	$I_{OL} = 5\text{ mA}$	-0.2	0.4	0.8	I	V
V_{OH}	Output Voltage Logic High CMOS Mode	4	4.6	5.1	I	V
	TTL Mode	2.4	2.7	3.2	I	V
I_{S+}	Positive Supply Current		16	19	I	mA
I_{S-}	Negative Supply Current		17	20	I	mA

Note 1: Two tests are performed with $V_{CM} = 0\text{V}$ to -9V and $V_{CM} = 0\text{V}$ to 10V .

Note 2: Two tests are performed with $V+ = +15\text{V}$, $V-$ changed from -10V to -15V ; $V- = -15\text{V}$, $V+$ changed from 10V to 15V .