National Semiconductor

PRELIMINARY
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DP80253
TROPIC II™ and DP80255 TROPIC II-SI™ Very High Performance Token Ring Protocol Interface Controller and System Interface for MicroChannel®

General Description

The DP80253 Token Ring Protocol Interface Controller II (TROPIC II) is a microCMOS VLSI device designed for high performance implementations of IEEE 802.5 Token-Ring LAN interface adapters.

The TROPIC II chip provides the functions needed to establish a Medium Access Control (MAC) layer connection to a Token Ring LAN. It operates at both 4 Mbps and 16 Mbps at full media speed and handles all MAC layer processing without involvement from the attached Host processor.

The TROPIC II has a proprietary parallel bus interface which must be connected to a DP80255 TROPIC II-System Interface device (TROPIC II-SI) that provides the MicroChannel host interface.

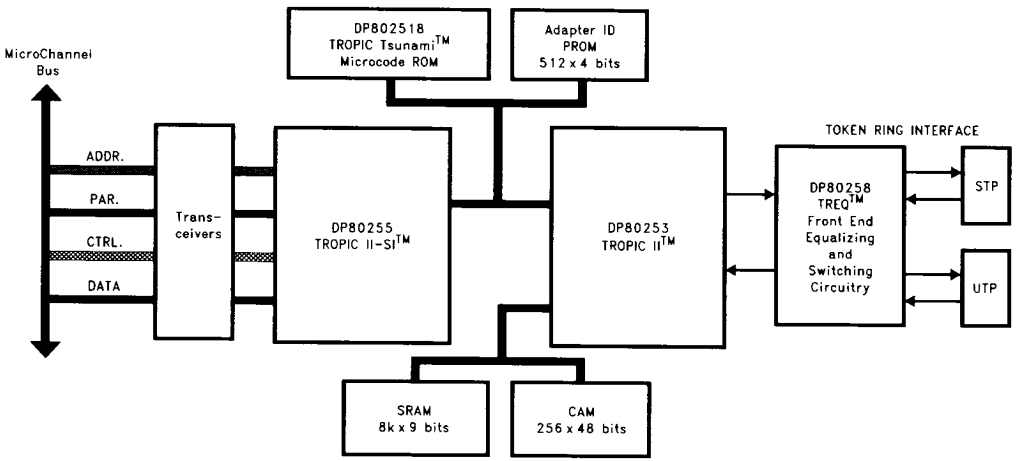
TROPIC II provides full IEEE 802.5 compatibility for MAC protocol handling, and is IBM 802.5 certified. Logical Link Control (LLC) packet processing is performed by the host system software.

Network performance exceeds current IEEE 802.5 Jitter requirements.

Features

- Very high performance (media speed) MicroChannel level B/C bus master Token Ring server/client adapter solution
- Full 32-bit address and data MicroChannel host system interface supports 40 MByte/s streaming mode
- MPU microcode provided for adapter operation
- Improved receive PLL jitter performance
- POS selectable 16/4 Mbps operation
- Multiple group address support
- Single +5V supply required
- CMOS for low power dissipation
- DP80253 TROPIC II is in a 171-pin PGA package
- DP80255 TROPIC II-SI is in a 208-pin PQFP

1.0 System Diagram



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DP80253 TROPIC II and DP80255 TROPIC II-SI Very High Performance Token Ring Protocol Interface Controller and System Interface for MicroChannel

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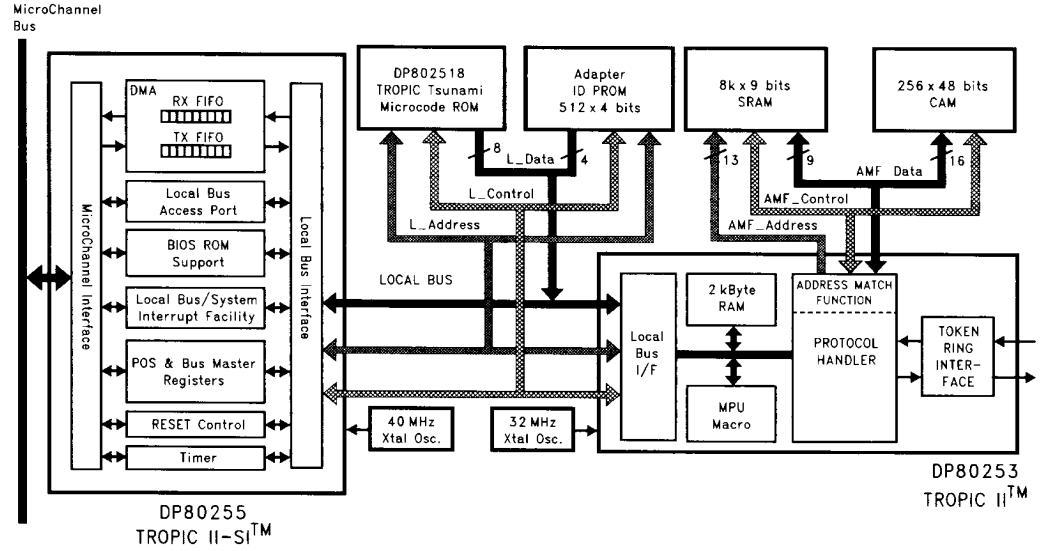

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3.0 Functional Description

3.1 DP80253 TROPIC II

The DP80253 TROPIC II has three interfaces (Token Ring interface, Address Match Function interface and Local Bus interface). These are described below:

3.1.1 Token Ring Interface

The TROPIC II has an improved front end design which, when used in conjunction with the DP80258 TREQ™ Token Ring Equalization device and the approved magnetics, will provide a full 4 Mbps and 16 Mbps Token Ring interface with superior analog characteristics to other older Token Ring products.

It is not possible to use the DP8025 TROPIC™ discrete analog front end design with the DP80253 TROPIC II: there are special pre-amplifiers designed into the DP80258 TREQ device and also separate equalization circuits for Unshielded Twisted Pair (UTP–100Ω) and Shielded Twisted Pair (STP–150Ω) cable and at both 4 Mbps and 16 Mbps operation (a total of four equalizers).

The receive phase locked loop (RXPLL) in the TROPIC II has been designed to have "pseudo constant gain". This greatly improves its jitter performance over other designs whose gain varies with received data pattern.

Selection of 4 Mbps or 16 Mbps ring speeds and STP or UTP cable selection is by MicroChannel POS register bits in the TROPIC II-SI. No external hardware jumpers are necessary.

Packets are received from the incoming data stream as follows: serial data is recovered from the incoming encoded data stream by the RXPLL in the Front End macro of the TROPIC II, the serial data is de-serialized and passed on to the Parallel Receive Channel function for address match checking and passing onto the MAC or LLC data streams.

Packets for transmission are prioritized by the TROPIC II in the Parallel Transmit Channel, converted to serial data and transmitted at the next free token. Transmit packet prioritization is performed in hardware in order to increase performance—previous designs did the prioritization in software.

3.1.2 Address Match Function Interface

As packets are received and deserialized, they are checked to see if the destination address matches the address stored in the TROPIC II, the broadcast address (all 1's) or one of a number of multicast (or "group") addresses. Packets are stored either in local memory or system memory as a result.

The TROPIC II has an external Address Match Function (AMF) interface that must have a 256k x 48-bit Content Addressable Memory (CAM) and an 8k x 9-bit SRAM connected to it in order for the node to function correctly.

The CAM on the AMF interface is used to store up to 256 different (freely chosen) group/multicast addresses. Full 48-bit comparisons are performed on these addresses. Note that addresses stored in the CAM can only be multicast addresses; the TROPIC II will not allow individual addresses to be written to the CAM.

3.0 Functional Description (Continued)

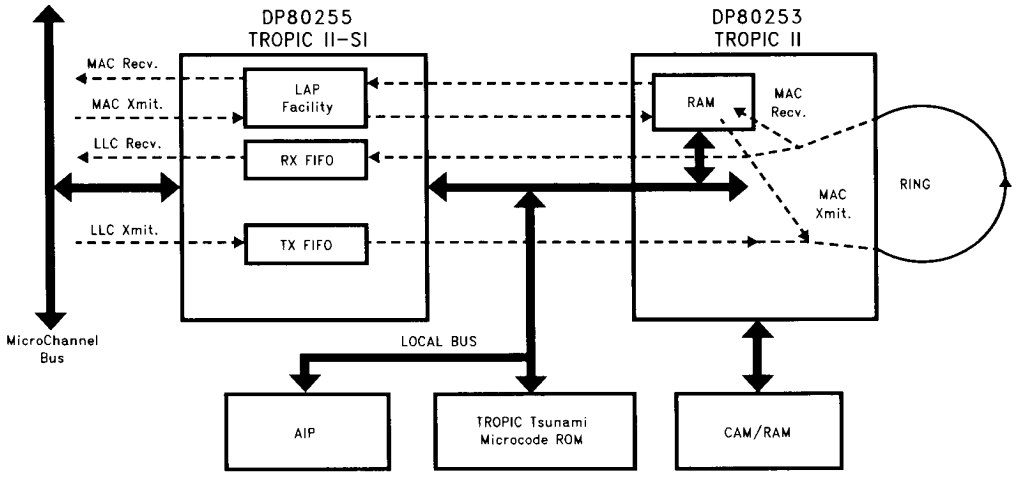

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FIGURE 1. Transmit and Receive Packet Dataflow

The SRAM on the AME interface is used to store up to 6 groups of 4k contiguous group/multicast addresses. The TROPIC II compares the received packet's destination address with the partial addresses held in the SRAM to decide if it is within any of the six 4k blocks.

Packets that have an address match are received into the TROPIC II's receive FIFO's. MAC frames are buffered into the TROPIC II's internal RAM and LLC frames are forwarded across the local bus interface to the DP80255 TROPIC II-SI. Packet data flow is illustrated in *Figure 1*.

The DP80253 TROPIC II device effectively has a 64 byte receive FIFO and a 32 byte transmit FIFO. These FIFOs are necessary to buffer traffic from local bus latency and internal switching delays.

3.1.3 Local Bus Interface

The TROPIC II's local bus interface connects the DP80253 TROPIC II to the DP80255 TROPIC II-SI systems interface device. The TROPIC II's microprocessor unit (MPU) runs microcode from an external EPROM connected to the local bus. An Adapter Information PROM (bipolar PROM 74S571) is also connected to the local bus to hold parameter information such as the Token Ring physical address and card configuration details.

Microcode fetches from the DP802518 TROPIC Tsunami™ microcode ROM are interlaced with Token Ring traffic transfers and special protocol specific information transfers on the local bus. Because the TROPIC II's internal 2 kbyte RAM is architecturally on the local bus, read and write accesses to it will be seen externally.

Certain technical details of the local bus and protocol specific information transfers on it are proprietary information and will not be disclosed. Enough functional and timing information is presented for the user to correctly hook up the microcode ROM and AIP devices to the local bus and connect the TROPIC II to the TROPIC II-SI.

3.2 DP80255 TROPIC II-SI

The DP80255 TROPIC II-SI only has two physical interfaces (Local Bus interface and MicroChannel Host interface) but performs several important functions internally. Both the interfaces and the internal functions are described below:

3.2.1 MicroChannel Interface

The TROPIC II-SI supports level B and C MicroChannel attachment. It has full 32-bit data and 32-bit address paths with optional address and data parity checking. Full 32-bit addressing is one of the most important features of the TROPIC II chipset since it allows dramatically increased server cache sizes: restricted cache size is possibly the most severe bottleneck to achieving very high server performance.

3.0 Functional Description (Continued)

TROPIC II-SI supports 16-bit and 32-bit 200 ns (min) basic non-streaming mode transfers and 16-bit or 32-bit 100 ns (min) streaming mode transfers when enabled.

Any MicroChannel bus arbitration level may be selected (although there are no hardware restrictions, users should check their systems design restrictions). Fairness is supported, but can be disabled if required. In addition to fairness, a programmable bus preempt timeout function can be used to restrict bus burst size if required.

As a bus slave, the TROPIC II-SI only supports level B 16-bit transfers.

TROPIC II-SI has four Host system interrupt lines that can be connected to four interrupt levels on the MicroChannel bus as desired.

The TROPIC II-SI supports synchronous channel check.

For many of the MicroChannel signals, 24 mA drivers are integrated into the TROPIC II-SI.

3.2.2 Local Bus Interface

The local bus interface connects the TROPIC II-SI to the TROPIC II and provides a conduit for LLC and MAC data transfer, register access, and PROM and RAM access.

Since the local bus interface is proprietary (as previously described), detail is limited to minimum necessary to correctly hook up the TROPIC II chipset.

3.2.3 Transmit FIFO, Receive FIFO and DMA

As a MicroChannel bus master, LLC packet traffic to and from the TROPIC II-SI and the Host memory passes through the TXFIFO and RXFIFO. Each of the FIFOs is 256 bytes long. The FIFO threshold for transmit and receive can be independently set to 32, 64 or 128 bytes. The transmit and receive channels can operate in full duplex.

LLC Packets for transmission are described by a Transmit Descriptor in Host memory (one packet per descriptor). Packets can be made up of a number of fragments (each called a Transmit Buffer). Transmit data buffers in Host memory are chained by pointers, so fragments can be non-contiguous. The minimum fragment size is 0 bytes and the maximum 18 kbytes—zero length fragments are ignored and do not take up Host bus bandwidth. Up to 255 fragments in each transmit descriptor are allowed. Transmit descriptors must be WORD aligned. Transmit buffers can be aligned to any byte boundary. Generally, Host system software drivers will operate the Transmit Buffers as a circular queue.

LLC Receive data can be scattered throughout the receive buffers available (more than one buffer per receive packet is allowed). Receive buffers can be aligned to any byte boundary. The TROPIC II-SI fills in a Receive Descriptor (for each LLC packet received) that describes where the packet is, how long it is, its status, etc. Receive Descriptors must be WORD aligned. The scattering and gathering of LLC packet data is automatic. The precise operation of the DMA and the receive and transmit buffers is discussed in Section 10.

3.2.4 Local Bus Access Port

The Local Bus Access Port (LAP) is used to pass control block associated parameters and data between the adapter and the Host.

MAC traffic is transmitted and received using the LAP facility via the TROPIC II's internal 2 kbyte RAM (see *Figure 1*).

Software use of the LAP facility is discussed in Section 10.

The LAP facility is used by writing the address of the local bus location to the LAP facility's port address registers, then the data transfer can be executed from the LAP's data "port" register.

All Host accesses to the local bus are controlled by the TROPIC II-SI. The LAP disallows illegal accesses as even seemingly innocuous reads to some locations could result in catastrophic node failure. LAP access violations are flagged as error interrupts. LAP read access violations always return a value of zero.

3.2.5 BIOS ROM Support

The TROPIC II-SI will support up to 16 kbytes of BIOS ROM. The BIOS ROM can be enabled/disabled and located anywhere in the region from xC0000 to xDC000 in Host system memory using POS register bits. The BIOS ROM can be used to contain Remote Program Load (RPL) instructions for remote boot of a diskless workstation from a server. Since the TROPIC II chipset is intended for high performance server adapter cards, RPL code is not included in the microcode EPROM.

3.2.6 Local Bus and System Interrupts

Local and system interrupt status registers are used to flag both hardware interrupt conditions and software command passing conditions between the Host system and the TROPIC II's CPU/microcode. TROPIC II can generate interrupts on one of four selectable Host system interrupt levels. A single interrupt signal line is used on the local bus interface.

3.2.7 POS and Bus Master Registers

TROPIC II-SI has registers that are used to control operations and provide status information to the Host system.

Programmable Option Select (POS) registers are provided to contain the MicroChannel Adapter ID, Basic Configuration and Bus Master configuration information. The Bus Master POS registers are used to configure the MicroChannel parameters such as arbitration level, etc.

Separate Bus Master status and control registers are used for receive and transmit of LLC traffic. These locate the transmit and receive buffers in Host memory, the current buffer, receive and transmit status, etc.

3.2.8 Reset Control

In the TROPIC II chipset there are two types of reset: hard (hardware) reset and soft (software) reset.

Hard reset occurs as a result of the MicroChannel signal CHRESET going true. The hard reset state is held for as long as the CHRESET signal is true.

3.0 Functional Description (Continued)

Soft reset occurs when the soft reset bit in the Basic Control Register (BCR) is set. The soft reset state is held until the soft reset bit in the BCR is cleared.

The precise action of these resets is described in Section 8.

3.2.9 Timer

A general purpose timer is available for use by the Host system software. The timer can be set to generate ticks in 10 ms intervals from 10 ms to 2550 ms. It generates a "timer expired" interrupt upon each timer expiry.

The timer accuracy is the same as the tolerance of the 40 MHz crystal oscillator connected to the TROPIC II-SI except for the first decrement after a Timer Value is written, when the decrement time error will be $+1$ ms/-2 ms.

The timer is only intended to be used as a general purpose wake-up timer for software purposes.

4.0 Host Hardware Interface

Details of the external drivers and circuitry needed to interface the TROPIC II to the MicroChannel bus are given in this section.

Without the use of external POS ID circuitry, the TROPIC II-SI responds to POS ID 8FAxh which belongs exclusively to IBM. Users need to obtain their own POS ID and add external POS ID logic. Complete details of the external POS ID circuitry are given in Application Note ANxxx "*A High Performance MicroChannel Token Ring Adapter Using the TROPIC II Chipset*".

A block diagram to show the principle of the external POS ID circuitry is shown in *Figure 2* below. A GAL decodes MicroChannel setup read accesses to the POS ID bytes, intercepts the data from the TROPIC II-SI device (by disabling a bus transceiver) and enables a hardwired value onto the bus instead. The TROPIC II-SI provides all the bus timing for these accesses.

The rest of the TROPIC II-SI's MicroChannel bus interface is straightforward and is shown in *Figure 3*. It consists of simple data transceivers and drivers or straight "one to one" connections. Although the diagram shows 74F245 transceivers, users can achieve a substantial board space saving by replacing these with 74FR16245 16-bit transceiver devices.

The TROPIC II-SI provides several MicroChannel attachment options. The primary method of determining the attachment type is by the use of the -BE0/Level C signal, but also by the way some of the interface signals are connected. The block diagram in *Figure 3* shows the connections for the automatic **Level B/Level C** attachment—most high performance server adapters will be of this type. The different attachment types are:

Level B (16-bit)—TROPIC II-SI operates as a level B bus master. The attachment is the same as in *Figure 3*, except all the signals associated with 32-bit MicroChannel are left unconnected.

Level C (32-bit)—TROPIC II-SI operates as a level C bus master. The attachment is the same as in *Figure 3* except that MicroChannel pin A81 should be connected to the adapter's $+5$V power plane.

Level B/Level C—TROPIC II-SI automatically senses the level of the slot into which it is inserted. This is the option shown in *Figure 3*. Note that the only connection to MicroChannel pin A81 is to the 3K9 resistor attached to the -BE0/Level C pin—MicroChannel pin A81 should not be connected to the adapter's $+5$V power plane.

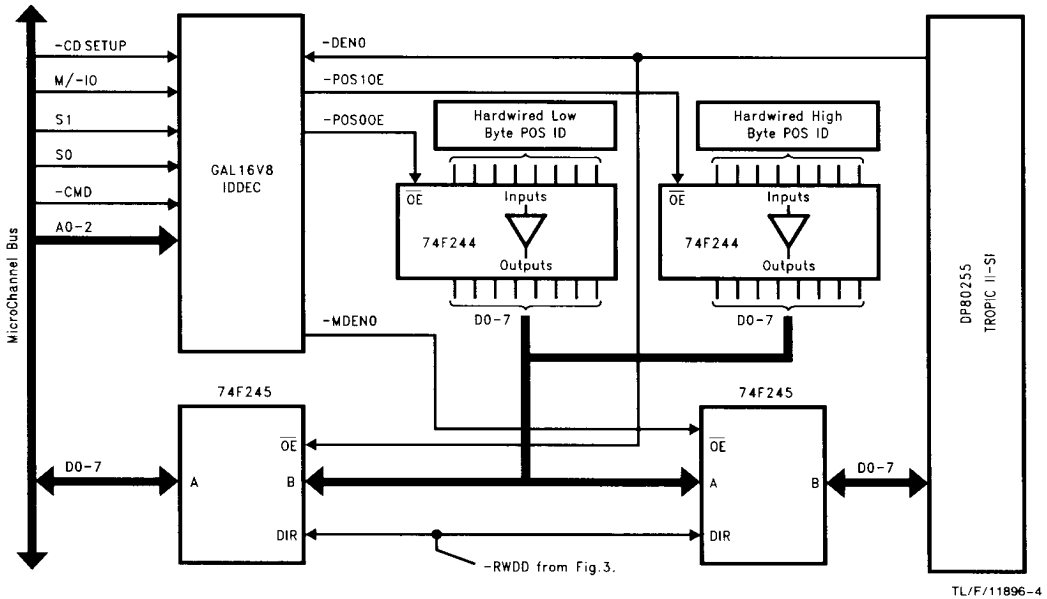

FIGURE 2. Required External POS ID Circuitry

4.0 Host Hardware Interface (Continued)

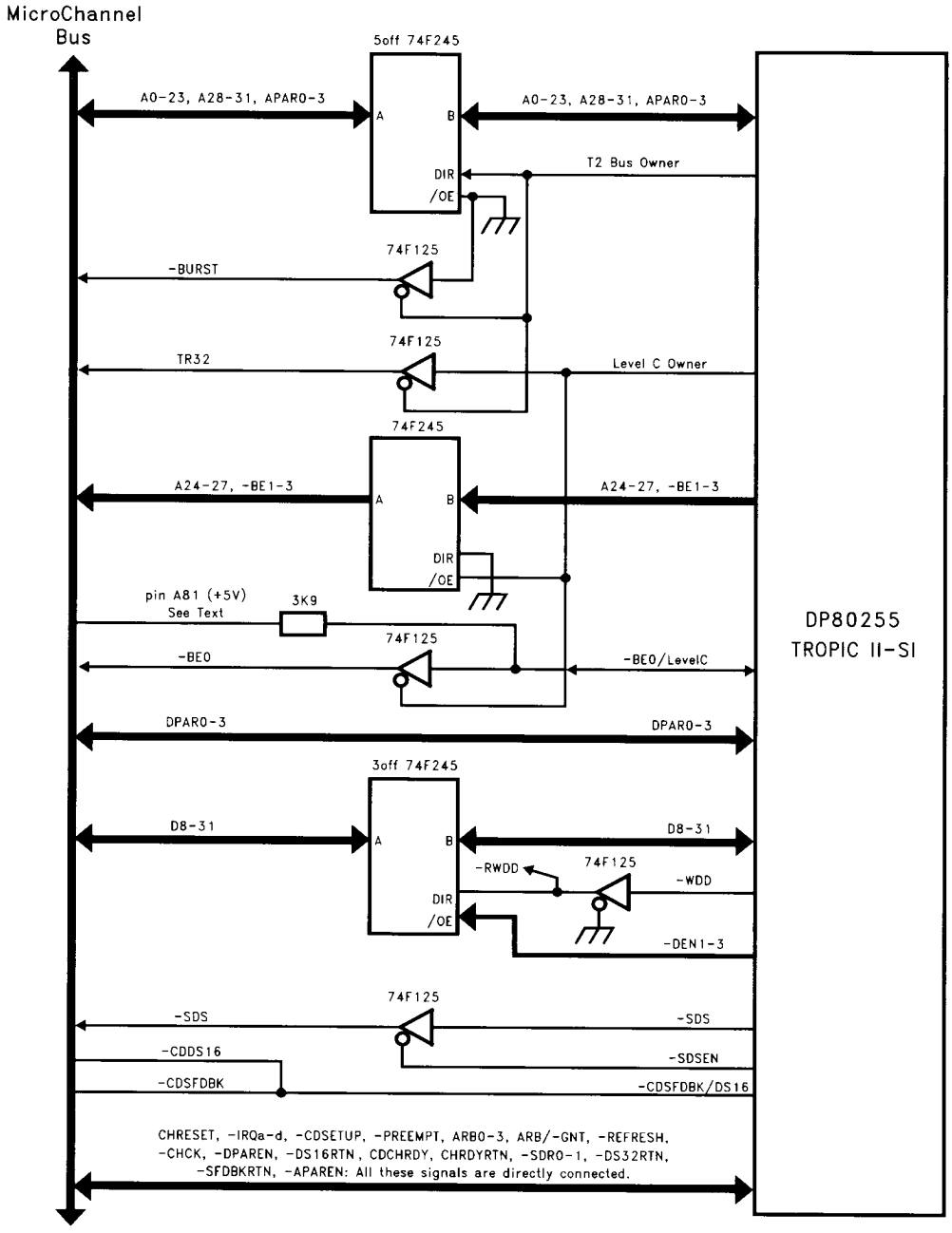

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FIGURE 3. TROPIC II-SI MicroChannel Bus Connection—Block Diagram

5.0 Local Bus Hardware Interface

The local bus hardware consists of the DP802518 TROPIC Tsunami microcode ROM, the Adapter Information PROM (AIP), a little glue logic and an alphabet's worth of "one to one" connected signals between the TROPIC II and the TROPIC II-SI.

5.1 MICROCODE ROM

The TROPIC Tsunami Microcode ROM is a 64 kbyte ROM with licensed Token Ring microcode programmed into it. No timing is given for the device since none is required in order to connect it up correctly.

The local address bus L__A0 to 15 connects directly to the ROM address pins A0 to A15 respectively and the eight ROM outputs O0 to O7 connect directly to the local data bus L__D0 to 7 respectively.

The local bus output enable L__OE connects directly to the output enable of the ROM. The ROM chip select is a buffered version of the microcode ROM chip select signal from the TROPIC II (-MROM).

5.2 ADAPTER INFORMATION PROM

The AIP is a standard 74S571 512k x 4-bit bipolar PROM that contains the adapter card's Token Ring MAC address plus other adapter specific configuration information.

The contents of the AIP are discussed briefly in Section 10. Full details are given in the document ANxxx "*MicroChannel Programmers Guide for the TROPIC II Chipset*".

The local address bus L__A0 to 8 connects directly to the AIP address pins A0 to A8 respectively and the four AIP outputs O0 to O3 connect directly to the local data bus L__D0 to 3 respectively.

The AIP enable (/G) signal is formed from the OR of the local bus output enable L__OE and a buffered version of the AIP chipselect signal from the TROPIC II (-AIP).

Again, since no timing information is needed to successfully connect up the AIP, none is given.

5.3 TROPIC II/TROPIC II-SI CONNECTIONS

All the information needed to connect the TROPIC II to the TROPIC II-SI is given in the block diagram shown in *Figure 4* below. There are 26 signals that must be joined between the TROPIC II and the TROPIC II-SI. One of these, L__M, is driven by a 74F125 buffer device from the C8M signal out of the TROPIC II.

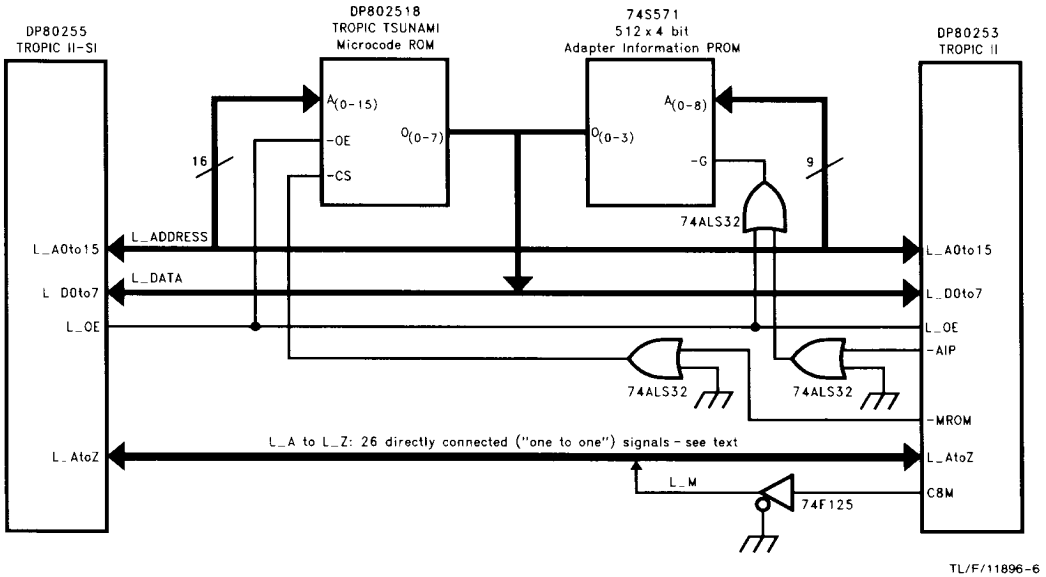

FIGURE 4. Local Bus Hardware Interface—Block Diagram

6.0 Address Match Function Hardware Interface

TROPIC II's Address Match Function (AMF) has its own bus interface to connect external storage devices. The TROPIC Tsunami microcode expects there to be an 8k by 9-bit SRAM (45 ns access time) and a single AM99C10A 256k x 48-bit CAM connected to this bus as shown in the block diagram in *Figure 5* below. These components are not optional.

6.1 SRAM INTERFACE

A 9-bit wide SRAM is required to perform the function of storing the information for up to six groups of 4k contiguous multicast (group) addresses for destination address comparison with the incoming Token Ring data stream. The RAM is used in conjunction with internal TROPIC II registers to perform this function. Details of this are given in Section 9.

The hardware interface to the SRAM is simple. The bus requires that the SRAM have 45 ns access time (address to data valid minimum, e.g. M5M5179P-45).

6.2 CAM INTERFACE

A 256k x 48-bit CAM device is required to hold up to 256 user chosen multicast (group) addresses for destination address comparison by the TROPIC II. Again, the CAM is used in conjunction with internal TROPIC II registers to perform this function.

CAM devices have a multiplexed address and data bus; all CAM activity is performed as a series of "locked" accessed to the device. The TROPIC II in conjunction with its microcode perform all the necessary sequencing and timing needed by the CAM automatically.

The CAM_D/-C signal from the TROPIC II tells the CAM if the current access is Data or Command. A 74F125 driver is required to re-drive the CAM chipselect signal AMF_CAM. The FULL and MATCH flag outputs are not required by the TROPIC II and are left unconnected.

The lower 9 bits of the CAM's address/data bus is shared with the SRAM's 9 bits of data. TROPIC II handles all the timing for this bus.

7.0 Token Ring Interface

This section will be added in the next revision of this data sheet. It will include details of the new high performance front end design using the DP80258 Token Ring Equalization (TREQ) device and show how to connect up a fully IBM and IEEE802.5 Token Ring compliant interface for both STP and UTP cables.

8.0 Initialization

This section will be added in the next revision of this data sheet. It will show the TROPIC II chipset's reset states and how users can configure the adapter after power up.

9.0 Register Descriptions

This section will be added in the next revision of this data sheet. It will give complete details of all the required registers for software to completely configure an adapter and run it normally.

10.0 Software Interface

This section will be added in the next revision of this data sheet. It will give details of the transmit and receive LLC and MAC frames buffers and how the software should use them.

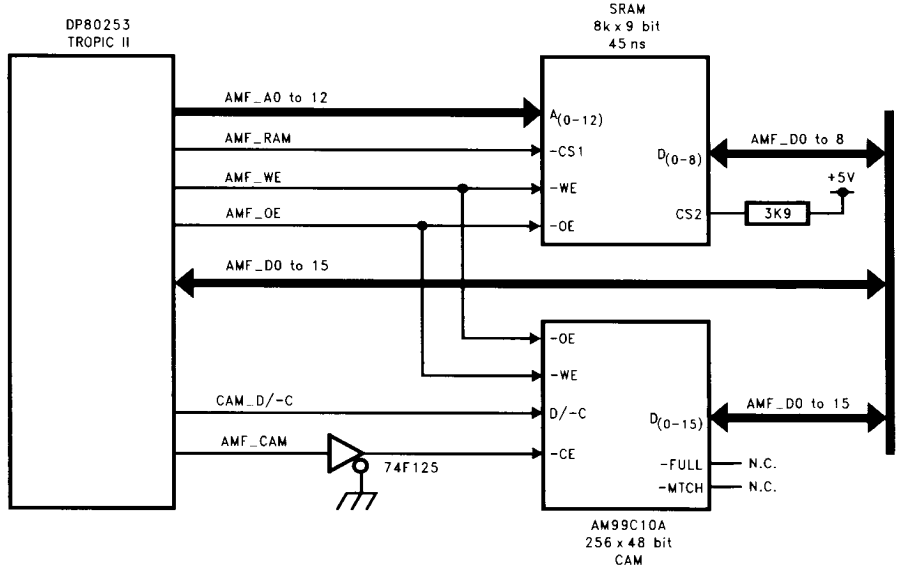

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FIGURE 5. Address Match Function RAM/CAM Interface—Block Diagram

11.0 Pin Descriptions

The pin descriptions for the TROPIC II and TROPIC II-SI are given below.

11.1 DP80253 TROPIC II PIN DESCRIPTION

Pins are grouped into functional families for clarity. Pin types are as follows:

ALI	Analog Input	TTD	TTL Input with internal pull-down resistor
ALO	Analog Output	TSD	TRI-STATE® Driver (CMOS)
TTL	TTL Input	CIO	Combined Input/Output—TTL/TSD
TTU	TTL Input with internal pull-up resistor	CIU	CIO with internal pull-up resistor

Pin Name	Pin No.	Type	Description
TOKEN RING INTERFACE PINS			
UTP/-STP	N03	TSD	**UTP/STP** MEDIUM SELECT OUTPUT: Used to drive transistor switches for UTP/STP changeover relays. UTP selected when output is HIGH, STP selected when output is LOW.
STP/-UTP	M04	TSD	**STP/UTP** MEDIUM SELECT OUTPUT: Used to drive DP80258 TREQ medium select input. Inverse of UTP/-STP pin above. STP selected when output is HIGH, UTP selected when output is LOW.
16M+i/p	P01	ALI	**16 M**bps + RECEIVE DIFFERENTIAL DATA **INPUT**: Driven by DP80258 TREQ.
16M−i/p	N01	ALI	**16 M**bps − RECEIVE DIFFERENTIAL DATA **INPUT**: Driven by DP80258 TREQ.
4M+i/p	K02	ALI	**4 M**bps + RECEIVE DIFFERENTIAL DATA **INPUT**: Driven by DP80258 TREQ.
4M−i/p	J01	ALI	**4 M**bps − RECEIVE DIFFERENTIAL DATA **INPUT**: Driven by DP80258 TREQ.
TXD+	F01	ALO	**Transmit** + DIFFERENTIAL DATA OUTPUT: To output filter/transformer circuitry.
TXD−	G01	ALO	**Transmit** − DIFFERENTIAL DATA OUTPUT: To output filter/transformer circuitry.
PhantomA	J02	ALO	**Phantom** DRIVE **A**: This output drives the transmit phantom power circuitry.
PhantomB	H01	ALO	**Phantom** DRIVE **B**: This output drives the transmit phantom power circuitry.
PLLFLTR4	L02	ALO	**4** Mbps **PLL** LOOP **FILTER** OUTPUT: Used to set receive PLL loop response.
PLLFLTR16	L01	ALO	**16** Mbps **PLL** LOOP **FILTER** OUPUT: Used to set receive PLL loop response.
PLLGND	M01	ALO	**PLL** LOOP FILTER **GND** RETURN: Used for external PLL loop filter GND return.
CLOCK INPUT			
32 MHz	A07	TTL	**32 MHz** CLOCK INPUT: Must be driven by a 32 MHz ±0.01% signal source with a worst case duty cycle ratio of 40%/60%.
NO CONNECT PINS			
NC	A09, B01, B08, C01, C14, D01, D02, E02, E14, F02, F03, F12, F13, F14, G02, G04, G13, G14, H11, H12, H13, H14, J10, J11, J12, J13, J14, K14, L05, M05, N04, P03, P04, P10		
POWER SUPPLY PINS			
Analog Power Pins			
AV_{CC}	K03, L03, H02		
AGND	H03, K04, M02		
Digital Power Pins			
V_{CC}	C07, D06, E06, E08, F04, J03, L06, L08, M06		
GND	B06, C06, D07, E04, E07, H04, H10, J04, L07, L10, M07, M08		

11.0 Pin Descriptions (Continued)

11.1 DP80253 TROPIC II PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
LOCAL BUS INTERFACE			
Local Address Bus			
L_A0	B05	CIO	LOCAL ADDRESS BUS **A0**
L_A1	B07	CIO	LOCAL ADDRESS BUS **A1**
L_A2	A08	CIO	LOCAL ADDRESS BUS **A2**
L_A3	C02	CIO	LOCAL ADDRESS BUS **A3**
L_A4	E03	CIO	LOCAL ADDRESS BUS **A4**
L_A5	C03	CIO	LOCAL ADDRESS BUS **A5**
L_A6	A06	CIO	LOCAL ADDRESS BUS **A6**
L_A7	C04	CIO	LOCAL ADDRESS BUS **A7**
L_A8	D04	CIO	LOCAL ADDRESS BUS **A8**
L_A9	A03	CIO	LOCAL ADDRESS BUS **A9**
L_A10	A02	CIO	LOCAL ADDRESS BUS **A10**
L_A11	B02	CIO	LOCAL ADDRESS BUS **A11**
L_A12	D03	CIO	LOCAL ADDRESS BUS **A12**
L_A13	A01	CIO	LOCAL ADDRESS BUS **A13**
L_A14	A06	CIO	LOCAL ADDRESS BUS **A14**
L_A15	A05	CIO	LOCAL ADDRESS BUS **A15**
Local Data Bus			
L_D0	B11	CIU	LOCAL DATA BUS **D0**
L_D1	C09	CIU	LOCAL DATA BUS **D1**
L_D2	A11	CIU	LOCAL DATA BUS **D2**
L_D3	C10	CIU	LOCAL DATA BUS **D3**
L_D4	A12	CIU	LOCAL DATA BUS **D4**
L_D5	E09	CIU	LOCAL DATA BUS **D5**
L_D6	D09	CIU	LOCAL DATA BUS **D6**
L_D7	B12	CIU	LOCAL DATA BUS **D7**
-MROM	E12	CIO	**M**ICROCODE **ROM** SELECT SIGNAL: Chipselect for the DP802518 TROPIC Tsunami microcode ROM.
-AIP	G10	CIO	**A**DAPTER **I**NFORMATION **P**ROM SELECT SIGNAL: Chipselect for the AIP device.
-L_OE	A14	CIU	**L**OCAL BUS **O**UTPUT **E**NABLE: Output enable signal for local bus slaves.
C8M	E13	TSD	**8 M**Hz **C**LOCK OUTPUT: Must be re-driven—see *Figure 4*, Section 5.

11.0 Pin Descriptions (Continued)

11.1 DP80253 TROPIC II PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
LOCAL BUS INTERFACE (Continued)			
One to one connections between DP80253 TROPIC II and DP80255 TROPIC II-SI			
L_A	C08	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **A**
L_B	C05	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **B**
L_C	B04	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **C**
L_D	D08	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **D**
L_E	B13	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **E**
L_F	C13	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **F**
L_G	B14	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **G**
L_H	B10	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **H**
L_I	B09	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **I**
L_J	D12	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **J**
L_K	A04	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **K**
L_L	D05	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **L**
L_M	G11	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **M**
L_N	C12	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **N**
L_O	D13	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **O**
L_P	A13	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **P**
L_Q	A10	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **Q**
L_R	E10	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **R**
L_S	E05	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **S**
L_T	F11	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **T**
L_U	D11	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **U**
L_V	F10	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **V**
L_W	D10	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **W**
L_X	D14	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **X**
L_Y	C11	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **Y**
L_Z	E11	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **Z**
MISCELLANEOUS PINS			
PD330	G12	TTD	**Pull** this signal **Down** with a **330Ω** resistor to GND.
PU330	G03	TTU	**Pull** this signal **Up** with a **330Ω** resistor to V_{CC}.
PWROFF	E01	TTD	Connect this signal to GND.
Rext	K01	ALO	Connect a 4k99 1% **R**esistor from this pin to GND.
PO	L04	ALI	NC
PI	M03	ALI	Connect this signal to V_{CC}.
NO	N02	ALI	NC
NI	P02	ALI	Connect this signal to GND.

11.0 Pin Descriptions (Continued)

11.1 DP80253 TROPIC II PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
ADDRESS MATCH FUNCTION INTERFACE			
AMF Address Bus			
AMF_A0	N05	TSD	**AMF** ADDRESS **A0**
AMF_A1	L13	TSD	**AMF** ADDRESS **A1**
AMF_A2	P05	TSD	**AMF** ADDRESS **A2**
AMF_A3	M14	TSD	**AMF** ADDRESS **A3**
AMF_A4	L12	TSD	**AMF** ADDRESS **A4**
AMF_A5	N06	TSD	**AMF** ADDRESS **A5**
AMF_A6	L11	TSD	**AMF** ADDRESS **A6**
AMF_A7	M12	TSD	**AMF** ADDRESS **A7**
AMF_A8	M13	TSD	**AMF** ADDRESS **A8**
AMF_A9	N14	TSD	**AMF** ADDRESS **A9**
AMF_A10	M11	TSD	**AMF** ADDRESS **A10**
AMF_A11	L09	TSD	**AMF** ADDRESS **A11**
AMF_A12	N13	TSD	**AMF** ADDRESS **A12**
AMF Data Bus			
AMF_D0	M10	CIO	**AMF** DATA **D0**
AMF_D1	P14	CIO	**AMF** DATA **D1**
AMF_D2	P13	CIO	**AMF** DATA **D2**
AMF_D3	P06	CIO	**AMF** DATA **D3**
AMF_D4	M09	CIO	**AMF** DATA **D4**
AMF_D5	N12	CIO	**AMF** DATA **D5**
AMF_D6	N11	CIO	**AMF** DATA **D6**
AMF_D7	N10	CIO	**AMF** DATA **D7**
AMF_D8	N08	CIO	**AMF** DATA **D8**
AMF_D9	P11	CIO	**AMF** DATA **D9**
AMF_D10	N09	CIO	**AMF** DATA **D10**
AMF_D11	P12	CIO	**AMF** DATA **D11**
AMF_D12	P09	CIO	**AMF** DATA **D12**
AMF_D13	N07	CIO	**AMF** DATA **D13**
AMF_D14	P08	CIO	**AMF** DATA **D14**
AMF_D15	P07	CIO	**AMF** DATA **D15**
-AMF_RAM	K10	TSD	**AMF SRAM** CHIPSELECT: LOW for SRAM read and write accesses only.
-AMF_CAM	K13	TSD	**AMF CAM** CHIPSELECT: LOW for CAM read and write accesses only.
-AMF_OE	K12	TSD	**AMF OUTPUT ENABLE**: Chip selected device outputs onto AMF DATA bus when this signal is LOW.
-AMF_WE	L14	TSD	**AMF WRITE ENABLE**: LOW for write accesses, HIGH for read accesses.
CAM_D/-C	K11	TSD	**CAM DATA/CONTROL** SIGNAL: Data access when HIGH, Control access when LOW.

11.0 Pin Descriptions (Continued)

11.2 DP80255 TROPIC II-SI PIN DESCRIPTION

Pins are grouped into functional families for clarity. Pin types are as follows:

OD	24 mA Open Drain driver	TTL	TTL input
TSL	6 mA TRI-STATE driver	TTU	TTL input with internal pull-up resistor
TSH	24 mA TRI-STATE driver	TTD	TTL input with internal pull-down resistor
BIL	Combination TSL/TTL	BIH	Combination TSH/TTL
BLU	BIL with internal pull-up resistor	BHU	BIH with internal pull-up resistor
BLD	BIL with internal pull-down resistor	TSU	TSL with internal pull-up resistor
ODU	OD with internal pull-up resistor		

Pin Name	Pin No.	Type	Description
MICROCHANNEL BUS MASTER ARBITRATION PINS			
-ARB0	67	BIH	MICROCHANNEL **ARB**ITRATION LEVEL BIT **0**
-ARB1	71	BIH	MICROCHANNEL **ARB**ITRATION LEVEL BIT **1**
-ARB2	73	BIH	MICROCHANNEL **ARB**ITRATION LEVEL BIT **2**
-ARB3	75	BIH	MICROCHANNEL **ARB**ITRATION LEVEL BIT **3**
ARB/-GNT	108	TTL	**ARB**ITRATE/**GRANT**: HIGH when arbitration is in progress, goes LOW if TROPIC II-SI wins the arbitration process.
-PREEMPT	77	BIH	**PREEMPT**: Driven LOW when ARB/-GNT is LOW, deactivates within a specified time after TROPIC II-SI becomes bus master. It is received if fairness is being observed (set by a bit in a POS register).
MICROCHANNEL ADDRESS BUS PINS			
A0	36	BIL	MICROCHANNEL ADDRESS BUS **A0**
A1	40	BIL	MICROCHANNEL ADDRESS BUS **A1**
A2	41	BIL	MICROCHANNEL ADDRESS BUS **A2**
A3	45	BIL	MICROCHANNEL ADDRESS BUS **A3**
A4	47	BIL	MICROCHANNEL ADDRESS BUS **A4**
A5	70	BIL	MICROCHANNEL ADDRESS BUS **A5**
A6	74	BIL	MICROCHANNEL ADDRESS BUS **A6**
A7	81	BIL	MICROCHANNEL ADDRESS BUS **A7**
A8	82	BIL	MICROCHANNEL ADDRESS BUS **A8**
A9	91	BIL	MICROCHANNEL ADDRESS BUS **A9**
A10	92	BIL	MICROCHANNEL ADDRESS BUS **A10**
A11	96	BIL	MICROCHANNEL ADDRESS BUS **A11**
A12	26	BIL	MICROCHANNEL ADDRESS BUS **A12**
A13	30	BIL	MICROCHANNEL ADDRESS BUS **A13**
A14	34	BIL	MICROCHANNEL ADDRESS BUS **A14**
A15	48	BIL	MICROCHANNEL ADDRESS BUS **A15**
A16	50	BIL	MICROCHANNEL ADDRESS BUS **A16**
A17	52	BIL	MICROCHANNEL ADDRESS BUS **A17**
A18	63	BIL	MICROCHANNEL ADDRESS BUS **A18**

11.0 Pin Descriptions (Continued)

11.2 DP80255 TROPIC II-SI PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
MICROCHANNEL ADDRESS BUS PINS (Continued)			
A19	66	BIL	MICROCHANNEL ADDRESS BUS **A19**
A20	68	BIL	MICROCHANNEL ADDRESS BUS **A20**
A21	83	BIL	MICROCHANNEL ADDRESS BUS **A21**
A22	86	BIL	MICROCHANNEL ADDRESS BUS **A22**
A23	89	BIL	MICROCHANNEL ADDRESS BUS **A23**
A24	8	BIL	MICROCHANNEL ADDRESS BUS **A24**
A25	189	BIL	MICROCHANNEL ADDRESS BUS **A25**
A26	176	BIL	MICROCHANNEL ADDRESS BUS **A26**
A27	173	BIL	MICROCHANNEL ADDRESS BUS **A27**
A28	172	BIL	MICROCHANNEL ADDRESS BUS **A28**
A29	171	BIL	MICROCHANNEL ADDRESS BUS **A29**
A30	170	BIL	MICROCHANNEL ADDRESS BUS **A30**
A31	169	BIL	MICROCHANNEL ADDRESS BUS **A31**
MICROCHANNEL ADDRESS BUS ASSOCIATED PINS			
-ADL	78	BHU	**AD**DRESS **L**ATCH SIGNAL: Used to latch the MicroChannel address bits.
-APAREN	196	BHU	**A**DDRESS **PAR**ITY **EN**ABLE: Used to enable address bus parity checking.
APAR0	188	BIH	**A**DDRESS BUS **PAR**ITY BIT **0**: Parity for address bits A0–A7.
APAR1	181	BIH	**A**DDRESS BUS **PAR**ITY BIT **1**: Parity for address bits A8–A15.
APAR2	177	BIH	**A**DDRESS BUS **PAR**ITY BIT **2**: Parity for address bits A16–A23.
APAR3	175	BIH	**A**DDRESS BUS **PAR**ITY BIT **3**: Parity for address bits A24–A31.
-CDSETUP	106	TTL	**CARD SETUP**: When this signal is LOW at the same time M/-IO is LOW, the TROPIC II-SI's POS registers are accessed.
-CDSFDBK /DS16	42	TSH	**CARD S**ELECTED **FEEDBACK/D**ATA **SIZE 16** BITS: Driven LOW for memory cycles where the address on the bus falls within the ROM region, and for I/O cycles where the address on the bus falls within the TROPIC II-SI's I/O region. It is driven HIGH for Card Set Up cycles.
MADE24	100	BIL	**MADE24**: Used to qualify ROM region address decodes.
M/-IO	24	BLU	**M**EMORY/INPUT-**O**UTPUT: Distinguishes the type of access.
-SFDBKRTN	197	TTU	**S**ELECTED **FEEDBACK RETURN**: indicates a valid address is being accessed.

11.0 Pin Descriptions (Continued)

11.2 DP80255 TROPIC II-SI PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
MICROCHANNEL DATA BUS PINS			
D0	99	BIH	MICROCHANNEL DATA BUS **D0**
D1	97	BIH	MICROCHANNEL DATA BUS **D1**
D2	95	BIH	MICROCHANNEL DATA BUS **D2**
D3	93	BIH	MICROCHANNEL DATA BUS **D3**
D4	90	BIH	MICROCHANNEL DATA BUS **D4**
D5	88	BIH	MICROCHANNEL DATA BUS **D5**
D6	85	BIH	MICROCHANNEL DATA BUS **D6**
D7	84	BIH	MICROCHANNEL DATA BUS **D7**
D8	80	BIH	MICROCHANNEL DATA BUS **D8**
D9	33	BIH	MICROCHANNEL DATA BUS **D9**
D10	32	BIH	MICROCHANNEL DATA BUS **D10**
D11	31	BIH	MICROCHANNEL DATA BUS **D11**
D12	29	BIH	MICROCHANNEL DATA BUS **D12**
D13	28	BIH	MICROCHANNEL DATA BUS **D13**
D14	25	BIH	MICROCHANNEL DATA BUS **D14**
D15	23	BIH	MICROCHANNEL DATA BUS **D15**
D16	19	BIH	MICROCHANNEL DATA BUS **D16**
D17	17	BIH	MICROCHANNEL DATA BUS **D17**
D18	16	BIH	MICROCHANNEL DATA BUS **D18**
D19	12	BIH	MICROCHANNEL DATA BUS **D19**
D20	11	BIH	MICROCHANNEL DATA BUS **D20**
D21	5	BIH	MICROCHANNEL DATA BUS **D21**
D22	3	BIH	MICROCHANNEL DATA BUS **D22**
D23	2	BIH	MICROCHANNEL DATA BUS **D23**
D24	199	BIH	MICROCHANNEL DATA BUS **D24**
D25	195	BIH	MICROCHANNEL DATA BUS **D25**
D26	192	BIH	MICROCHANNEL DATA BUS **D26**
D27	190	BIH	MICROCHANNEL DATA BUS **D27**
D28	187	BIH	MICROCHANNEL DATA BUS **D28**
D29	186	BIH	MICROCHANNEL DATA BUS **D29**
D30	185	BIH	MICROCHANNEL DATA BUS **D30**
D31	183	BIH	MICROCHANNEL DATA BUS **D31**

11.0 Pin Descriptions (Continued)

11.2 DP80255 TROPIC II-SI PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
MICROCHANNEL DATA BUS ASSOCIATED PINS			
BE0/Level C	15	BLD	**BYTE ENABLE 0/LEVEL C** ATTACHMENT DETECT: Indicates byte D0–D7 is valid.
BE1	13	TSU	**BYTE ENABLE 1**: Indicates byte D8–D15 is valid.
BE2	10	TSU	**BYTE ENABLE 2**: Indicates byte D16–D23 is valid.
BE3	7	TSU	**BYTE ENABLE 3**: Indicates byte D24–D31 is valid.
CDCHRDY	54	TSL	**CARD CHANNEL READY**: Used to indicate access cycle completion.
CHRDYRTN	206	TTU	**CHANNEL READY RETURN**: Monitored by bus masters, this signal indicates that slaves need more time to complete the normal cycle in progress. If in streaming mode, it is used to "pace" the bus master who uses it to wait the new data.
-CMD	59	BHU	**COMMAND**: Used to indicate times when data is valid.
-DPAREN	65	BHU	**DATA BUS PARITY ENABLE**: Indicates data parity checking is being done.
DPAR0	64	BIH	**DATA BUS PARITY BIT 0**: Parity bit for data byte D0–D7.
DPAR1	21	BIH	**DATA BUS PARITY BIT 1**: Parity bit for data byte D8–D15.
DPAR2	201	BIH	**DATA BUS PARITY BIT 2**: Parity bit for data byte D16–D23.
DPAR3	193	BIH	**DATA BUS PARITY BIT 3**: Parity bit for data byte D24–31.
-DS16RTN	110	TTU	**DATA SIZE 16 RETURN**: Indicates the slave's transfer data size capability.
-DS32RTN	148	TTU	**DATA SIZE 32 RETURN**: Indicates the slave's transfer data size capability.
-SBHE	20	BIL	**SYSTEM HIGH BYTE ENABLE**: Indicates that the high byte is valid.
-SDS	205	ODU	**STREAMING DATA STROBE**: Indicates to slaves when data is valid.
-SDR(0)	113	TTU	**STREAMING DATA REQUEST (0)**: Indicates that slave can do streaming mode.
-SDR(1)	123	TTU	**STREAMING DATA REQUEST (1)**: Indicates that slave can do streaming mode.
-S0	62	BHU	**STATUS BIT 0**: Indicates access type. If S0 is LOW and S1 is HIGH, a write is taking place. If S0 is HIGH and S1 is LOW, a read is taking place. No other combination is possible.
-S1	60	BHU	**STATUS BIT 1**: See -S0 description above.
MICROCHANNEL INTERRUPT SIGNAL PINS			
-IRQa	37	OD	**INTERRUPT REQUEST LINE a**: Connect to chosen MicroChannel interrupt level.
-IRQb	39	OD	**INTERRUPT REQUEST LINE b**: Connect to chosen MicroChannel interrupt level.
-IRQc	49	OD	**INTERRUPT REQUEST LINE c**: Connect to chosen MicroChannel interrupt level.
-IRQd	51	OD	**INTERRUPT REQUEST LINE d**: Connect to chosen MicroChannel interrupt level.
MICROCHANNEL MISCELLANEOUS PINS			
-CHCK	44	BIH	
CHRESET	112	TTL	
-REFRESH	121	TTL	

11.0 Pin Descriptions (Continued)

11.2 DP80255 TROPIC II-SI PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
MICROCHANNEL BUS TRANSCEIVER CONTROL PINS			
-T2 Bus Owner	55	TSL	TROPIC **II**-SI is the current **bus owner**.
-Level C Owner	4	TSL	TROPIC II-SI is a **level C** bus **owner**.
-SDSEN	204	TSL	**SDS EN**ABLE signal for re-drive of -SDS.
-WDD	207	TSL	**W**RITE **D**ATA **D**IRECTION signal for data transceivers (needs re-drive).
-DEN0	56	TSL	**D**ATA BYTE**0 EN**ABLE SIGNAL: Enables D0–D7's data transceiver.
-DEN1	57	TSL	**D**ATA BYTE**1 EN**ABLE SIGNAL: Enables D8–D15's data transceiver.
-DEN2	202	TSL	**D**ATA BYTE**2 EN**ABLE SIGNAL: Enables D16–23's data transceiver.
-DEN3	198	TSL	**D**ATA BYTE**3 EN**ABLE SIGNAL: Enables D24–D31's data transceiver.
LOCAL BUS INTERFACE PINS			
Local Data Bus			
L_D0	143	BIL	**L**OCAL DATA BUS **D0**
L_D1	160	BIL	**L**OCAL DATA BUS **D1**
L_D2	161	BIL	**L**OCAL DATA BUS **D2**
L_D3	162	BIL	**L**OCAL DATA BUS **D3**
L_D4	164	BIL	**L**OCAL DATA BUS **D4**
L_D5	165	BIL	**L**OCAL DATA BUS **D5**
L_D6	167	BIL	**L**OCAL DATA BUS **D6**
L_D7	168	BIL	**L**OCAL DATA BUS **D7**
Local Address Bus			
L_A0	155	BIL	**L**OCAL ADDRESS BUS **A0**
L_A1	152	BIL	**L**OCAL ADDRESS BUS **A1**
L_A2	150	BIL	**L**OCAL ADDRESS BUS **A2**
L_A3	137	BIL	**L**OCAL ADDRESS BUS **A3**
L_A4	134	BIL	**L**OCAL ADDRESS BUS **A4**
L_A5	118	TTL	**L**OCAL ADDRESS BUS **A5**
L_OE	131	BIL	**L**OCAL BUS **O**UTPUT **EN**ABLE: Output enable signal for local bus slaves.
One to one connections between DP80253 TROPIC II and DP80255 TROPIC II-SI			
L_A	149	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **A**
L_B	102	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **B**
L_C	158	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **C**
L_D	126	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **D**
L_E	146	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **E**
L_F	109	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **F**
L_G	127	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **G**
L_H	129	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **H**
L_I	103	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **I**
L_J	159	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **J**
L_K	115	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **K**

11.0 Pin Descriptions (Continued)

11.2 DP80255 TROPIC II-SI PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Type	Description
LOCAL BUS INTERFACE PINS (Continued)			
L__L	104	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **L**
L__M	116	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **M**
L__N	107	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **N**
L__O	147	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **O**
L__P	136	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **P**
L__Q	119	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **Q**
L__R	156	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **R**
L__S	120	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **S**
L__T	154	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **T**
L__U	135	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **U**
L__V	141	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **V**
L__W	138	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **W**
L__X	139	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **X**
L__Y	133	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **Y**
L__Z	145	—	TROPIC II/TROPIC II-SI INTERCONNECT SIGNAL **Z**
NO CONNECT PINS			
NC	124, 125, 128, 144, 178, 180		
CLOCK INPUT			
40 MHz	179	TTU	**40 MHz** CLOCK INPUT: Must be driven by a 40 MHz signal source with a worst case duty cycle ration of 45%/55% and a minimum rise time of 5 ns.
MISCELLANEOUS PINS			
PD330	157	TTL	**Pull** this signal **Down** with a **330**Ω resistor to GND.
POWER SUPPLY PINS:			
V_{CC}	9, 18, 27, 43, 61, 72, 79, 98, 114, 130, 142, 151, 166, 182, 191, 200		
GND	1, 6, 14, 22, 35, 38, 46, 53, 58, 69, 76, 87, 94, 101, 105, 111, 117, 122, 132, 140, 153, 163, 174, 184, 194, 203, 208		

12.0 DC and AC Specifications

This section will be added in the next revision of this datasheet.

12.1 DC ELECTRICAL CHARACTERISTICS

12.2 AC ELECTRICAL SPECIFICATIONS

13.0 Connection Diagrams

13.1 DP80253 TROPIC II CONNECTION DIAGRAM

Beveled Edge

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	L_OE	L_G	N.C.	L_X	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	-AMF_WE	AMF_A3	AMF_A9	AMF_D1
13	L_P	L_E	L_F	L_O	C8M	N.C.	N.C.	N.C.	N.C.	-AMF_CAM	AMF_A1	AMF_A8	AMF_A12	AMF_D2
12	L_D4	L_D7	L_N	L_J	-MROM	N.C.	PD330	N.C.	N.C.	-AMF_OE	AMF_A4	AMF_A7	AMF_D5	AMF_D11
11	LD_2	LD_0	L_Y	L_U	L_Z	L_T	L_M	N.C.	N.C.	CAM_D/C	AMF_A6	AMF_A10	AMF_D6	AMF_D9
10	L_Q	L_H	L_D3	L_W	L_R	L_V	-AIP	GND	N.C.	-AMF_RAM	GND	AMF_D0	AMF_D7	N.C.
9	N.C.	L_I	L_D1	L_D6	L_D5						AMF_A11	AMF_D4	AMF_D10	AMF_D12
8	L_A2	N.C.	L_A	L_D	VCC						VCC	GND	AMF_D8	AMF_D14
7	32MHz	L_A1	VCC	GND	GND						GND	GND	AMF_D13	AMF_D15
6	L_A14	GND	GND	VCC	VCC						VCC	VCC	AMF_A5	AMF_D3
5	L_A15	L_A0	L_B	L_L	L_S						N.C.	N.C.	AMF_A0	AMF_A2
4	L_K	L_C	L_A7	L_A8	GND	VCC	N.C.	GND	GND	AGND	PO	STP/-UTP	N.C.	N.C.
3	L_A9	L_A6	L_A5	L_A12	L_A4	N.C.	PU330	AGND	VCC	AVCC	AVCC	PI	UTP/-STP	N.C.
2	L_A10	L_A11	L_A3	N.C.	N.C.	N.C.	N.C.	AVCC	PhantomA	4M+i/p	PLLFLTR4	AGND	NO	NI
1	L_A13	N.C.	N.C.	N.C.	PWROFF	TXD+	TXD-	PhantomB	4M-i/p	Rext	PLLFLTR16	PLLGND	16M-i/p	16M+i/p

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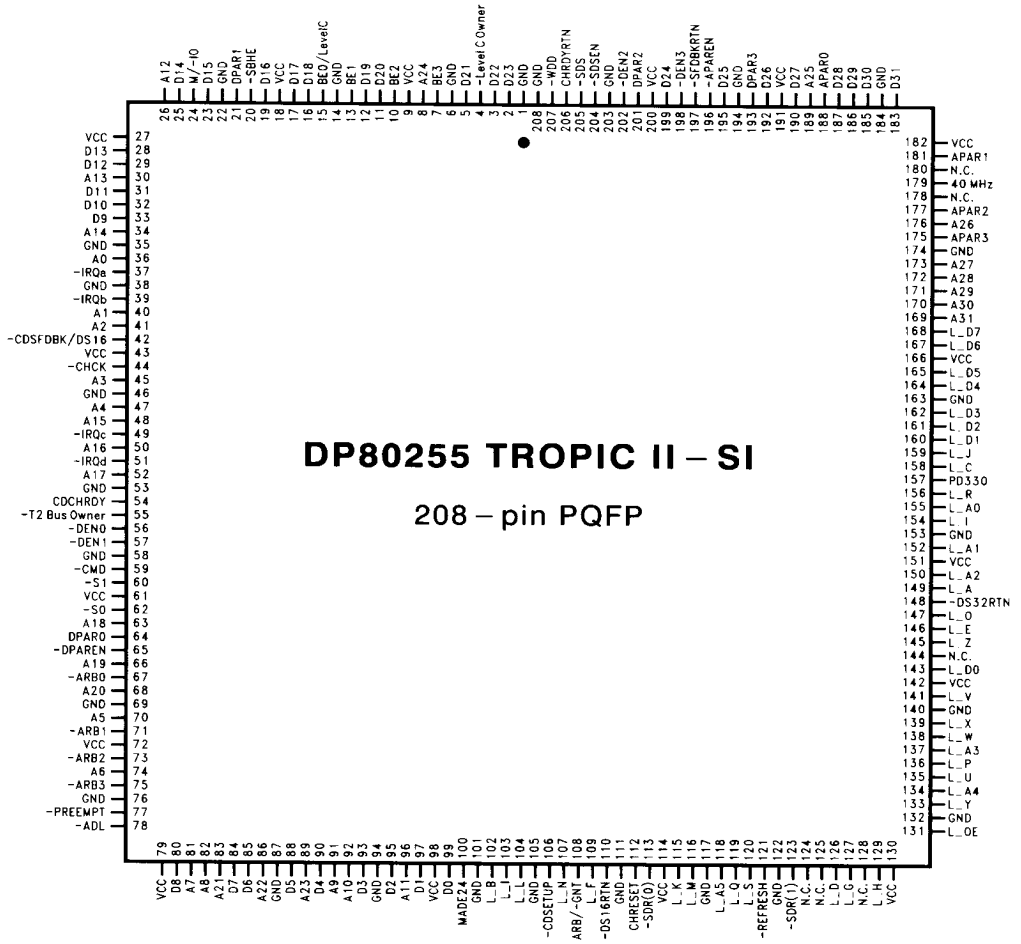
Viewed from the Pin Side

13.0 Connection Diagrams (Continued)

13.2 DP80255 TROPIC II-SI CONNECTION DIAGRAM



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208-Pin PQFP

14.0 Physical Dimensions

Lit. # 102850-001

Physical dimension information will be added to the next version of this datasheet.

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